TPS65135 Single-Inductor, Multiple-Output Regulator

1 Features

- Single-Inductor, Multiple-Output Topology
- 2.5-V to 5.5-V Input Voltage Range
- 750-mW Output Power at V_I = 2.9 V
- Positive Output Voltages Up to 6 V
- Negative Output Voltage Down to –7 V
- 1% Output Voltage Accuracy
- Up to 50% Output Current Mismatch Allowed
- Excellent Line Regulation
- Advanced Power-Save Mode for Light-Load Efficiency
- Low-Noise Operation
- Out-of-Audio Mode
- Short-Circuit Protection
- Thermal Shutdown
- 3-mm × 3-mm Thin QFN Package

2 Applications

- AMOLED Display Power Supplies
- LCD Power Supplies
- Split-Rail Power Supplies for Op-Amps, Data Converters, Data Interfaces, etc.

3 Description

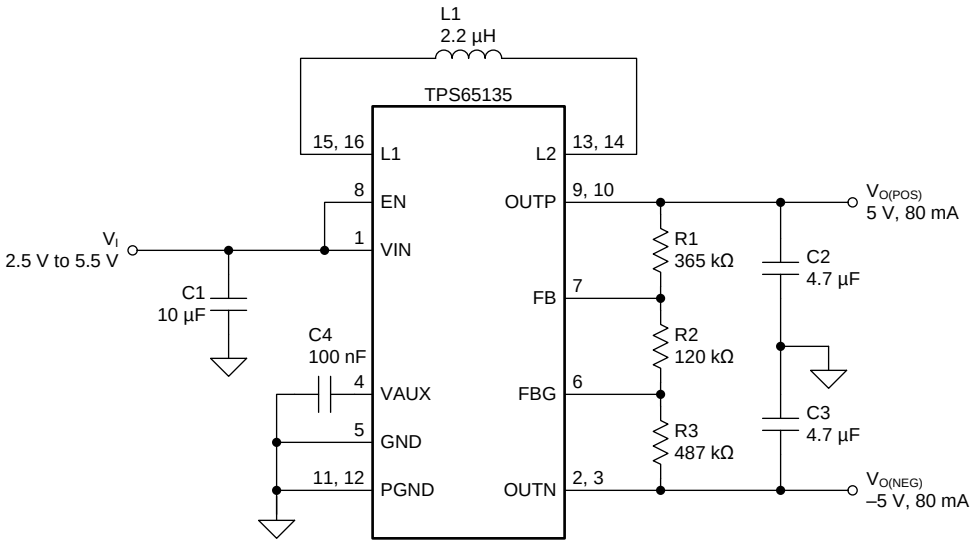
The TPS65135 device is a high-efficiency split-rail power supply. Thanks to its single-inductor, multiple-output (SIMO) topology, the converter uses very few external components. The device operates with a buck-boost topology and generates positive and negative output voltages above or below the input supply voltage. The SIMO topology achieves excellent line and load regulation, which is necessary, for example, to avoid disturbance of a mobile phone display as a result of input voltage variations that occur during transmit periods in mobile communication systems. The device can also be used as a general-purpose split-rail supply as long as the output current mismatch between the rails is less than 50%.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS65135	WQFN (16)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (June 2015) to Revision C — **Page**

- Changed L2 pin numbers From: 1 and 14 To: 13 and 14 in the *Pin Functions* table ... 3
- Changed PGND pin numbers From: 11 and 11 To: 11 and 12 in the *Pin Functions* table ... 3

Changes from Revision A (November 2011) to Revision B — **Page**

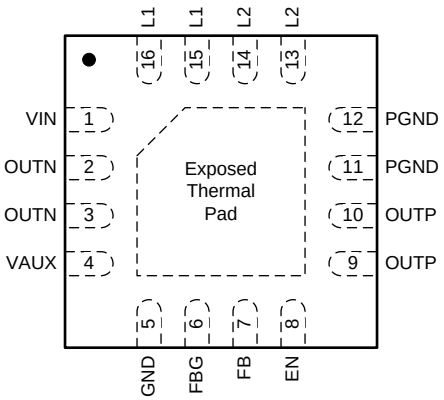
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Moved output current mismatch to Recommended Operating Conditions ... 4
- Moved maximum output power to Recommended Operating Conditions ... 4

Changes from Original (November 2011) to Revision A — **Page**

- Changed the UVLO threshould max value for V_{IN} falling From: 2 V To 2.1 V ... 5

5 Pin Configuration and Functions

RTE Package
16-Pin WQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	8	I	Input pin to enable the device. Pulling this pin high enables the device. This pin has an internal 500-kΩ pull-down resistor.
FB	7	I	Feedback regulation point for the positive output voltage rail
FBG	6	I	Feedback regulation point for the negative output voltage rail
GND	5	–	Analog ground
L1	15	I/O	Inductor terminal
	16		
L2	13	I/O	Inductor terminal
	14		
OUTN	2	O	Negative output
	3		
OUTP	9	O	Positive output
	10		
PGND	11	–	Power ground
	12		
VAUX	4	I/O	Reference voltage output. This pin requires a 100-nF capacitor for stability.
VIN	1	I	Input supply
Exposed thermal pad	—	–	Connect this pad to ground

6 Specifications

6.1 Absolute Maximum Ratings (1)(2)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Voltage	VIN, EN, VAUX, FB, OUTP, L2	–0.3	7	V
	L1, OUTN	–8	7	V
	FBG	–0.3	0.3	V
Operating junction temperature, T_J		–40	150	°C
Operating ambient temperature, T_A		–40	85	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to ground.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	
		Machine model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
V_I	Input voltage range	2.5		5.5	V
$I_{O(POS)}$ / $\lvert I_{O(NEG)} \rvert$	Output current mismatch	0.5		2	
P_O	Output power (V_I = 2.9 V, $V_{O(POS)} - V_{O(NEG)} \le$ 10 V)			750	mW
L	Inductor (1)	1	2.2	4.7	µH
$C_{(IN)}$	Input Capacitor (1)	4.7	10		µF
$C_{O(POS)}$, $C_{O(NEG)}$	Output Capacitors (1)	4.7	10	20	µF
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

(1) Please refer to *Application Information* for further information

6.4 Thermal Information

THERMAL METRIC (1)		TPS65135 RTE (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	44.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	42	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	4.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	16.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	0.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	16.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

V_I = 3.7 V, $V_{(EN)}$ = V_I, $V_{O(POS)}$ = 5 V, $V_{O(NEG)}$ = –5 V, T_A = –40°C to 85°C; typical values are at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_I	Input voltage range		2.5		5.5	V
$I_{I(standby)}$	Quiescent current	EN = H; measured into VIN pin		7		mA
	Shutdown current	EN = L; measured into VIN pin		0.1	2	µA
UNDERVOLTAGE LOCKOUT						
	Input threshold voltage (VIN) (undervoltage lockout)	V_I rising		2	2.3	V
		V_I falling		1.8	2.1	V
THERMAL SHUTDOWN						
	Thermal shutdown junction temperature			140		°C
	Thermal shutdown hysteresis			5		°C
ENABLE						
	High-level input voltage (EN)	V_I = 2.5 V to 5.5 V	1.2			V
	Low-level input voltage (EN)	V_I = 2.5 V to 5.5 V			0.4	V
$R_{(EN)}$	Pull-down resistor (EN)		200	500	900	kΩ
OUTPUT						
$V_{O(POS)}$	Positive output voltage range		3		6	V
	Threshold voltage (OUTP) (overvoltage protection)	$I_{O(POS)}$ = 10 mA	6.1	7		V
$V_{O(NEG)}$	Negative output voltage range		–7		–2.5	V
	Threshold voltage (OUTN) (overvoltage protection)	$I_{O(NEG)}$ = –10 mA		–7.6	-7.1	V
V_{ref1}	Positive output reference voltage		–1%	1.24	+1%	V
V_{ref2}	Negative output reference voltage		–10	0	10	mV
	MOSFET on-state resistance (Q1)	$I_{D(Q1)}$ = 100 mA		250		mΩ
	MOSFET on-state resistance (Q2)	$I_{D(Q2)}$ = 100 mA		200		mΩ
	MOSFET on-state resistance (Q3)	$I_{D(Q3)}$ = 100 mA		500		mΩ
	MOSFET on-state resistance (Q4)	$I_{D(Q4)}$ = 100 mA		300		mΩ
$I_{D(Q2)}$max	Q2 switch current limit	V_I = 3.7 V	0.9	1.2	1.6	A
		V_I = 2.5 V	1	1.5	1.9	

6.6 Typical Characteristics

V_I= 3.7 V and T_A = 25°C unless otherwise noted

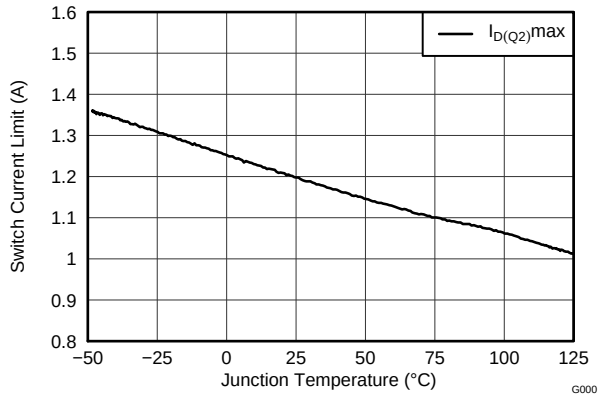


Figure 1. Switch Current Limit vs Temperature

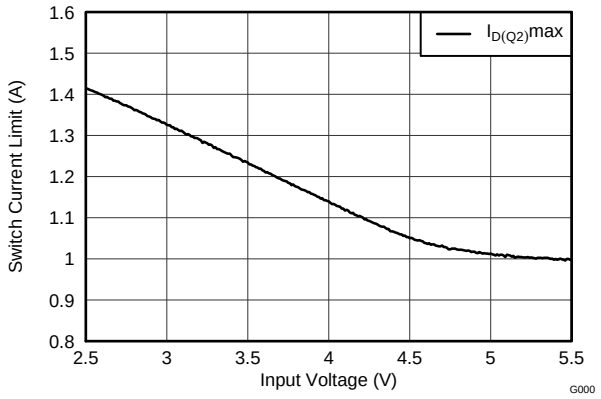


Figure 2. Switch Current Limit vs Input Supply Voltage

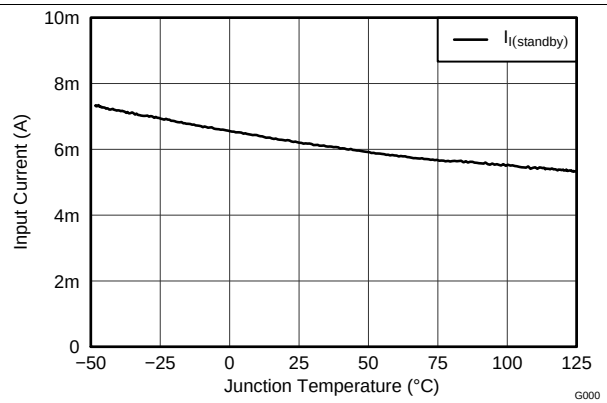


Figure 3. Input Supply Current vs Temperature

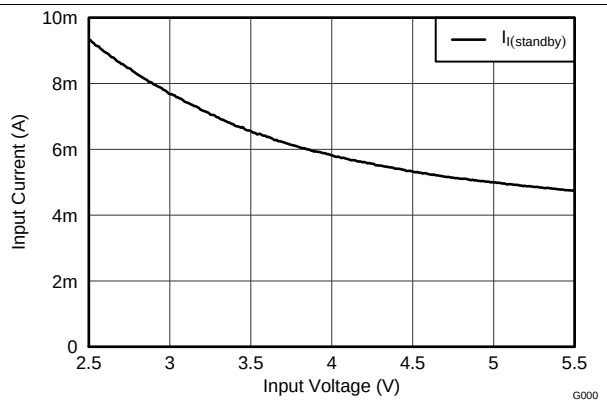


Figure 4. Input Supply Current vs Input Supply Voltage

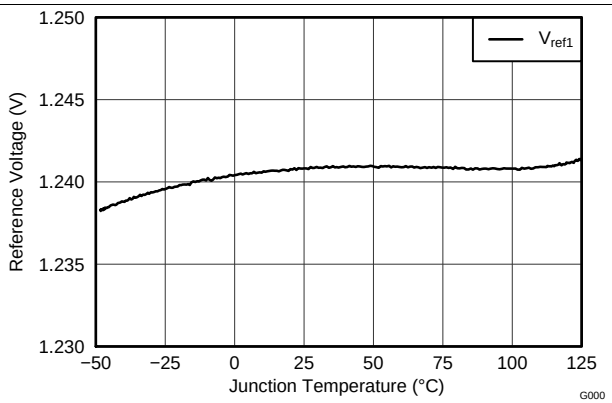


Figure 5. Reference Voltage V_{ref1} vs Temperature

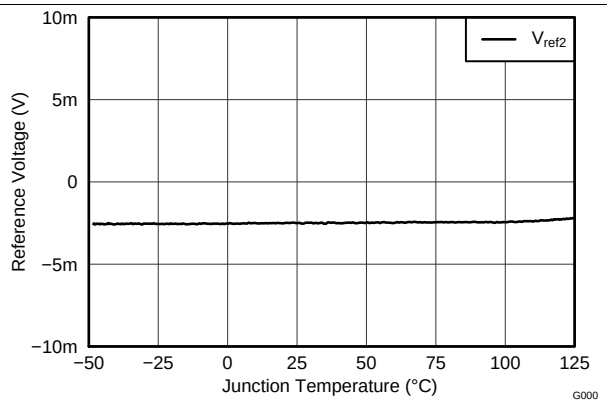


Figure 6. Reference Voltage V_{ref2} vs Temperature

7 Detailed Description

7.1 Overview

The TPS65135 device uses a four-switch buck-boost converter topology to generate one negative and one positive output voltage with a single inductor. The device uses a SIMO topology to achieve excellent line transient response, buck-boost mode for both outputs, and high efficiency over the entire output current range. High efficiency over the entire load-current range is implemented by reducing the converter switching frequency under low load conditions. Out-of-audio mode prevents the switching frequency going below 20 kHz.

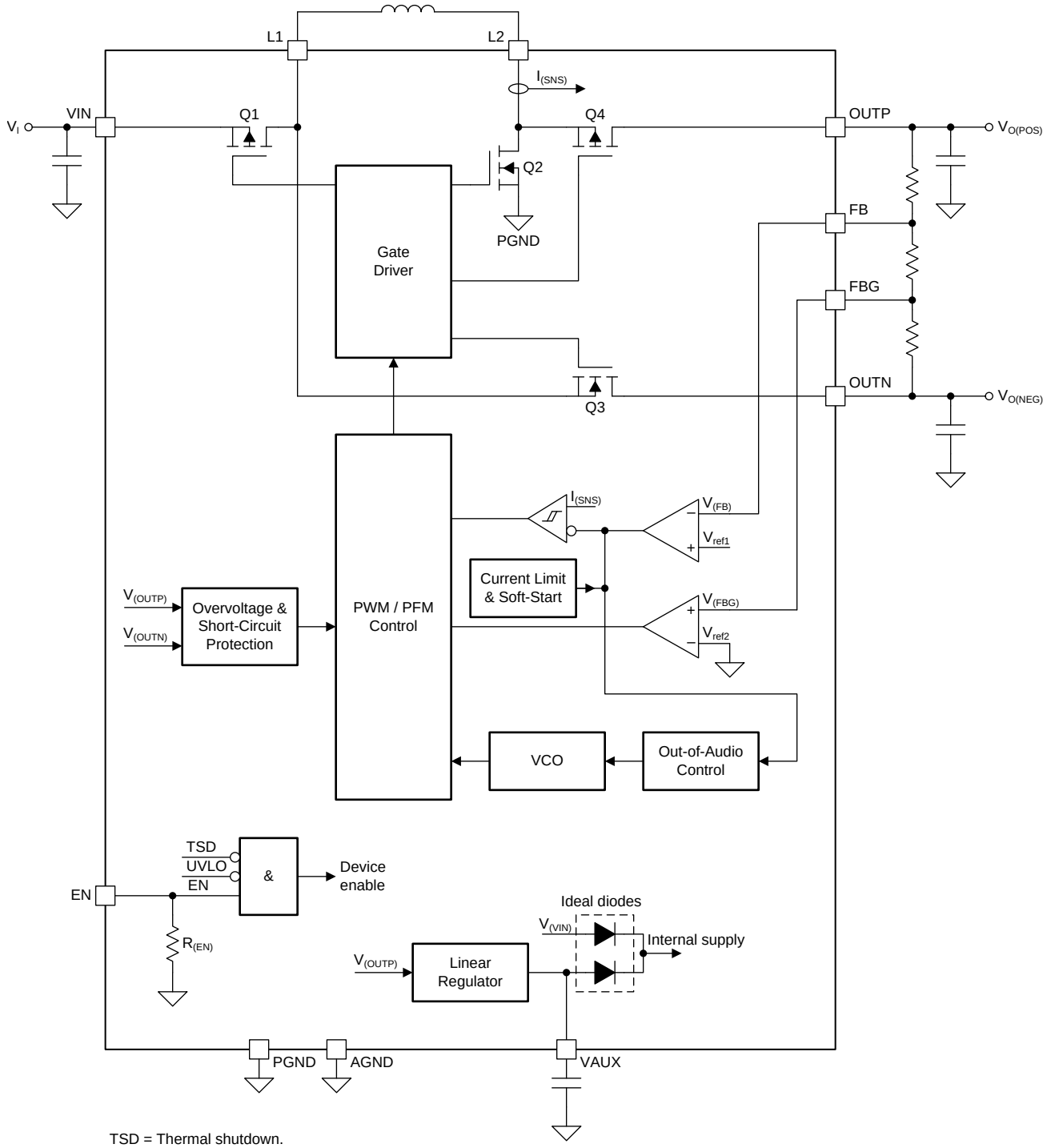
The converter operates with two control loops. One error amplifier controls the positive output voltage $V_{O(POS)}$ so that the FB pin is regulated to 1.24 V. A second error amplifier controls the negative output voltage $V_{O(NEG)}$ so that the FBG pin is regulated to 0 V. An external feedback divider allows both output voltages to be set to the desired value. In principle, the SIMO converter topology operates just like any other buck-boost converter topology, with the difference that the output voltage across the inductor is the sum of the positive and negative output voltages. With this consideration all calculations of the buck-boost converter apply for this topology as well. During the first part of a switching cycle Q1 and Q2 are closed, connecting the inductor from V_I to ground. During the second part of a switching cycle, the inductor discharges to the positive and negative outputs by closing switches Q4 and Q3. Because the inductor is discharged to both of the outputs simultaneously, the output voltages can be higher or lower than the input voltage. The converter operates best when the positive output current $I_{O(POS)}$ is equal to the negative output current $I_{O(NEG)}$, for example, as is the case when driving an AMOLED display. However, asymmetries of up to 50% in load current can be canceled out by the used topology. In such cases, a third part of the switching cycle is implemented, during which either Q3 is turned off and Q1 is turned on (as is the case when $I_{O(POS)} > I_{O(NEG)}$) or Q4 is turned off and Q2 is turned on (as is the case when $I_{O(NEG)} > I_{O(POS)}$) (see Table 1).

During light loads the converter operates in DCM, using peak-current control and a switching frequ3ency determined by a voltage-controlled oscillator (VCO). At higher load currents the converter operates in CCM with a switching frequency controlled by a fixed off-time. The SIMO regulator topology achieves its best line transient response when operating in DCM.

Table 1. Switch Control

Switching Cycle	Q1	Q2	Q3	Q4	Remark
Part 1	On	On	Off	Off	
Part 2	Off	Off	On	On	
Part 3	On	Off	Off	On	If $I_{O(POS)} > \lvert I_{O(NEG)} \rvert$
	Off	On	On	Off	If $\lvert I_{O(NEG)} \rvert > I_{O(POS)}$

7.2 Functional Block Diagram



TSD = Thermal shutdown.
UVLO = Undervoltage lockout.

7.3 Feature Description

7.3.1 Advanced Power-Save Mode for Light-Load Efficiency

In order to maintain high efficiency over the entire load current range, the converter reduces its switching frequency as the load current decreases. The advanced power-save mode controls the switching frequency using a voltage-controlled oscillator (VCO). The VCO frequency is proportional to the inductor peak current, with a lower frequency limit of 20 kHz; but in typical applications the frequency does not go below 100 kHz. This avoids disturbance of the audio band and minimizes audible noise coming from the ceramic input and output capacitors. By maintaining a controlled switching frequency, potential EMI is minimized. This is especially important when using the device in mobile phones. See Figure 24 for typical switching frequency versus load current. For zero load an internal shunt regulator ensures stable output voltage regulation.

7.3.2 Buck-Boost Mode Operation

Buck-boost mode operation allows the input voltage to be higher or lower than the output voltage. This mode allows the use of batteries and supply voltages that are above the positive output voltage.

7.3.3 Inherently Good Line-Transient Regulation

The SIMO regulator achieves inherently good line-transient response when operating in discontinuous conduction mode (DCM), as shown in Figure 14 and Figure 15. In DCM, the current delivered to the output is determined by the peak value and slope of the inductor current. This is illustrated in Figure 7, where the average output current, shown by the shaded area, is the same for different input voltages. Because the converter uses peak-current-mode control, the peak current is fixed as long as the load current is fixed. The falling slope of the inductor current is given by the difference between the positive and negative output voltages and the inductor value; it is independent of the input voltage. As a result, any change in input voltage changes the converter duty cycle but not the peak value or slope of the inductor current when discharging. The average output current, given by the area A (Figure 7), therefore remains constant over any input voltage variation. Entering continuous conduction mode (CCM) linearly decreases the line-transient performance; however, the line-transient response in CCM is still as good as any standard current-mode switching converter.

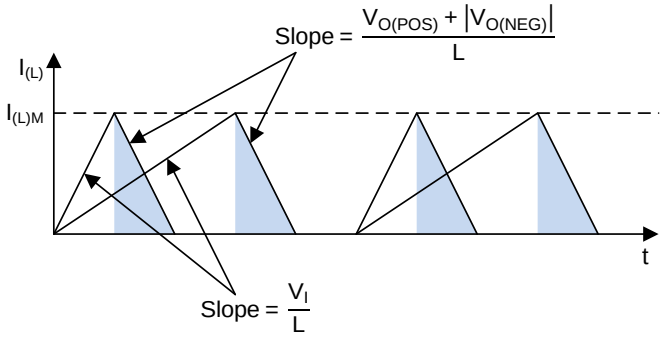


Figure 7. Inherently Good Line-Transient Regulation

The following formulas describe the operation of the TPS65135 device when operating in CCM with equal positive and negative output currents. The converter always sees the sum V_O of the magnitude of the positive and negative output voltages, as given by

$$V_O = V_{O(POS)} + |V_{O(NEG)}| \quad (1)$$

where

- $V_{O(POS)}$ is the positive output voltage
- and $V_{O(NEG)}$ is the negative output voltage.

The converter duty cycle is calculated using the efficiency estimation from datasheet curves or from real application measurements. A value of 70% for the efficiency η is a good starting assumption for most applications.

Feature Description (continued)

$$D = \frac{V_O}{\eta V_I + V_O}$$

where

- D is the duty cycle of Q2
- and η is the converter efficiency. (2)

Now the output current for entering CCM can be calculated. The switching frequency can be obtained from the data sheet graphs. A frequency of 1.5 MHz is a good assumption for these calculations.

$$I_{O(CCM)} = \frac{V_O(1-D)^2}{2fL}$$

where

- $I_{O(CCM)}$ is the value of output current at which continuous conduction starts;
- f is the converter switching frequency;
- and L is the inductance connected between the L1 and L2 pins. (3)

The inductor ripple current when operating in CCM can also be calculated

$$I_{(L)(PP)} = \frac{DV_I}{fL}$$

where

- $I_{(L)(PP)}$ is the peak-to-peak (that is, ripple) inductor current. (4)

Finally, the converter switch peak current can be calculated

$$I_{(L)M} = \frac{I_O}{1-D} + \frac{I_{(L)(PP)}}{2}$$

where

- $I_{(L)M}$ is the peak (that is, maximum) inductor current. (5)

7.3.4 Overvoltage Protection

The device monitors the positive and negative output voltages and reduces the current limit when either (or both) of the output voltages exceeds its overvoltage protection threshold. The positive output voltage is clamped to 7 V and the negative output voltage to –7.6 V.

7.3.5 Short-Circuit Protection

Both outputs are protected against short circuits either to ground or to the other output. The device's switching frequency and current limit are reduced in case of a short circuit.

7.3.6 Soft-Start Operation

The device increases the current limit during soft-start operation to avoid high inrush currents during start up. The current limit typically ramps up to its maximum value within 100 µs.

Feature Description (continued)

7.3.7 Output-Current Mismatch

The device operates best when the current of the positive output is similar to the current of the negative output. However, the device is able to regulate an output current mismatch of up to 50% (See Figure 26 for typically allowed currents, only 50% mismatch is specified). If the output-current mismatch becomes much larger one of the outputs goes out of regulation and finally the device shuts down. In case of zero load of one output the other output can support up to 5 mA. The device automatically recovers when the mismatch is reduced. The formula below can be used to calculate the maximum supported current mismatch.

$$0.5 \leq \left| \frac{I_{O(POS)}}{I_{O(NEG)}} \right| \leq 2 \quad (6)$$

7.3.8 Setting the Output Voltages

The output voltages are set by the three feedback resistors R1, R2, and R3 (Figure 8). R1 and R2 set the positive output voltage $V_{O(POS)}$ and R2 and R3 set the negative output voltage $V_{O(NEG)}$. To reduce the circuit's sensitivity to noise, it is recommended to choose R2 so that a current of at least 10 µA flows through the feedback resistors. Equation 7 can be used to calculate a suitable value for R2.

$$R2 = \frac{V_{ref1}}{I_{(R2)}} = \frac{1.24\ V}{10\ \mu A} = 124\ k\Omega \quad (7)$$

The positive output voltage $V_{O(POS)}$ is given by

$$V_{O(POS)} = V_{ref1}\left(1 + \frac{R1}{R2}\right) \quad (8)$$

The negative output voltage $V_{O(NEG)}$ is given by

$$V_{O(NEG)} = -V_{ref1}\left(\frac{R3}{R2}\right) \quad (9)$$

7.4 Device Functional Modes

7.4.1 Operation with 2.5 V ≤ V_I ≤ 5.5 V

The recommended input supply voltage is 2.5 V to 5.5 V. Within this range the device operates normally and achieves its specified performance.

7.4.2 Operation with V_I < 2.5 V

The recommended minimum input supply voltage is 2.5 V. The device continues to operate with input supply voltages lower than 2.5 V, however, its performance is not specified. The device does not operate with input supply voltages below the UVLO threshold.

7.4.3 Operation with V_I > 5.5 V

The recommended maximum input supply voltage is 5.5 V. As long as the absolute maximum voltage is not exceeded, the device will not be damaged by input supply voltages greater than 5.5 V, however, its performance is not specified.

Device Functional Modes (continued)

7.4.4 Operation with EN

When EN = L the device is disabled and switching is inhibited. When EN = H the device is enabled and its start-up sequence begins. If the EN pin is left floating an internal 500-kΩ resistor pulls this pin to ground.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS65135 device can be used to generate spilt-rail supplies from input supply voltages in the range 2.5 V to 5.5 V and has been optimized for use with 3.3-V rails of single-cell Li-ion batteries. It can generate positive output voltages up to 6 V and negative voltages down to –7 V with buck-boost action (i.e. the input supply voltage may be above or below the positive output voltage), as long as the output current mis-match is 50% or less. Both outputs are controlled by the EN pin: a high logic level enables both outputs, and a low logic level disables them. An integrated UVLO function disables the device when the input supply voltage is too low for proper operation.

8.2 Typical Application

Figure 8 shows a typical application for a ±5-V AMOLED display supply.

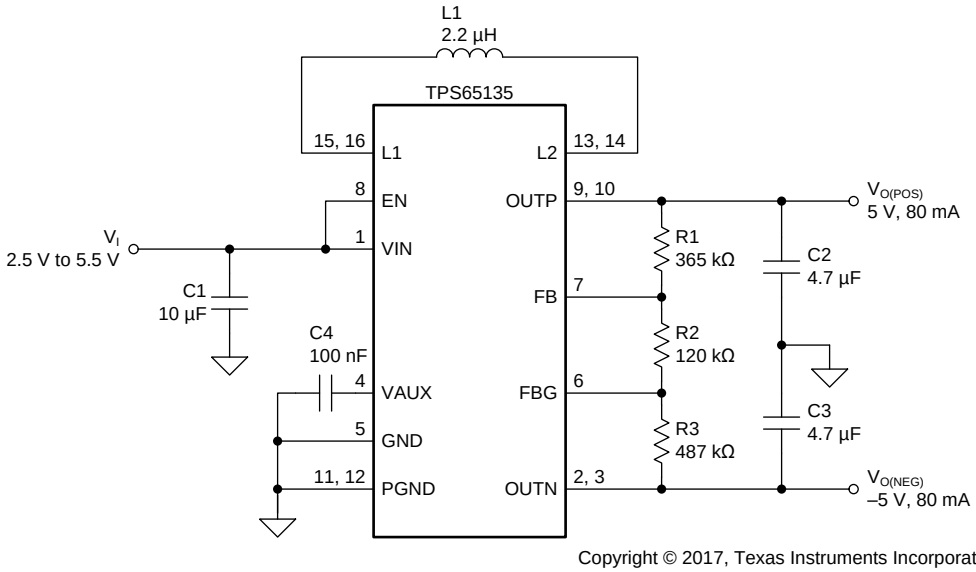


Figure 8. Standard Application ±5-V Supply

8.2.1 Design Requirements

Table 2 shows the design requirements for a ±5-V AMOLED supply application used as an example to illustrate the design process.

Typical Application (continued)

Table 2. Design Parameters

PARAMETER	SYMBOL	EXAMPLE VALUE
Input Supply Voltage Range	V_I	2.5 V to 5.5 V
Positive Output Voltage	$V_{O(POS)}$	5 V
Negative Output Voltage	$V_{O(NEG)}$	–5 V
Maximum Positive Output Current	$I_{O(POS)}$ max	80 mA
Maximum Negative Output Current	$I_{O(NEG)}$ max	–80 mA

8.2.2 Detailed Design Procedure

8.2.2.1 Choosing a Suitable Inductor

The TPS65135 device is internally compensated and operates best with a 2.2-µH inductor. For this type of converter, selection of the inductor is a key element in the design process because it has a big impact on the efficiency, the line and load transient response, and the maximum output current the device is able to deliver. Because the inductor ripple current is fairly large in the SIMO topology, the inductor core losses largely determine converter efficiency. As a result, an inductor with a relatively large dc winding resistance (DCR) but low core losses can often achieve higher converter efficiencies than other inductors with lower DCR but higher core losses.

As previously described, the converter's line transient response is highest when the converter operates in DCM, and since larger inductor values cause the converter to enter CCM operation at lower load currents, smaller inductor values give the best line transient response. The formula to calculate the output current at which the converter enters CCM operation is shown in Equation 3. The inductors listed in Table 3 achieve a good overall converter efficiency while having a low height. The first two TOKO inductors achieve the highest efficiency (almost identical) followed by the LPS3008. The best compromise between efficiency and inductor size is given by the XFL2006 inductor. The inductor saturation current should typically be 1 A or higher, however, if the output current required by the application is low, inductors with smaller saturation current ratings may be considered.

Table 3. Inductor Selection

INDUCTOR VALUE	COMPONENT SUPPLIER	DIMENSIONS in mm	I_{sat} / DCR
2.2 µH	TOKO DFE252010C	2.5 x 2 x 1	1.9 A / 130 mΩ
	TOKO DFE252012C	2.5 x 2 x 1.2	2.2 A / 90 mΩ
	Coilcraft XFL2006-222	2 × 1.9 × 0.6	0.8 A / 278 mΩ
	Coilcraft LPS3008-222	3 × 3 × 0.8	1.1 A / 175 mΩ
	Samsung CIG2MW2R2NNE	2 × 1.6 × 1	1.2 A / 110 mΩ
	TOKO FDSE0312-2R2	3.3 × 3.3 × 1.2	1.2 A / 160 mΩ
	ABCO LPF3010T-2R2	2.8 × 2.8 × 1	1.0 A / 100 mΩ
	Maruwa CXFU0208-2R2	2.65 × 2.65 × 0.8	0.85 A / 185 mΩ

8.2.2.2 Choosing Suitable Input and Output Capacitors

The TPS65135 device typically requires a 10-µF ceramic input capacitor. Larger values can be used to lower the input voltage ripple. Table 4 lists capacitors suitable for use on the TPS65135 input.

Table 4. Input Capacitor Selection

CAPACITOR	COMPONENT SUPPLIER	SIZE
10 µF / 6.3V	Murata GRM188R60J106ME84D	0603
10 µF / 6.3 V	Taiyo Yuden JMK107BJ106	0603

A 4.7-µF output capacitor is generally sufficient for most applications, but larger values can be used as well for improved load- and line-transient response at higher load currents. The capacitors of Table 5 have been found to work well with the TPS65135 device.

Table 5. Output Capacitor Selection

CAPACITOR	COMPONENT SUPPLIER	SIZE
10 µF / 6.3 V	Murata GRM188R60J106ME84D	0603
4.7 µF / 10 V	Taiyo Yuden LMK107BJ475	0603
10 µF / 6.3 V	Taiyo Yuden JMK107BJ106	0603

8.2.2.3 Choosing Suitable Feedback Resistors

Equation 7 can be used to calculate a suitable value for R2, so that the recommended current of ≈10 µA flows through the feedback resistors.

The value of R1 can be calculated by rearranging Equation 7, so that

$$R1 = R2\left(\frac{V_{O(POS)}}{V_{ref1}} - 1\right) \tag{10}$$

Inserting R2 = 120 kΩ, V_{ref1} = 1.24 V and $V_{O(POS)}$ = 5 V into Equation 10, we get

$$R1 = 120\ k\Omega\left(\frac{5\ V}{1.24\ V} - 1\right) = 363.9\ k\Omega \tag{11}$$

The closest 1%-tolerance standard value is 365 kΩ, which will generate a nominal output voltage of 5.012 V.

The value of R3 can be calculated by rearranging Equation 9, so that

$$R3 = R2\left(\frac{\left|V_{O(NEG)}\right|}{V_{ref1}}\right) \tag{12}$$

Inserting R2 = 120 kΩ, V_{ref1} = 1.24 V and $V_{O(NEG)}$ = –5 V into Equation 12, we get

$$R3 = 120\ k\Omega\left(\frac{5\ V}{1.24\ V}\right) = 483.9\ k\Omega \tag{13}$$

The closest 1%-tolerance standard value is 487 kΩ, which will generate a nominal output voltage of –5.032 V.

8.2.2.4 Measurement Circuit

The following application curves were obtained using the circuit shown in Figure 9 and the external components listed in Table 6.

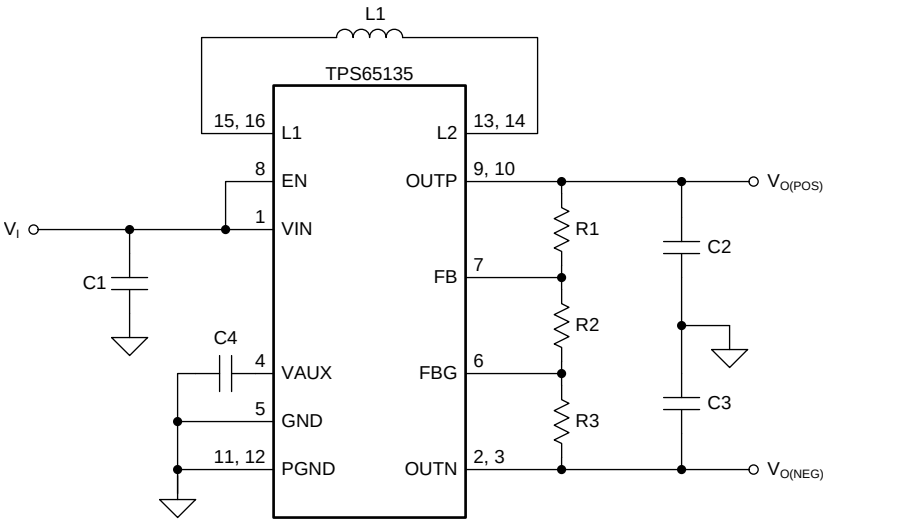


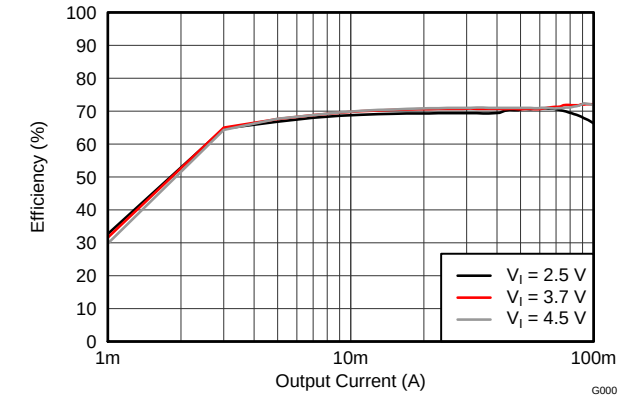
Figure 9. Measurement Circuit

Table 6. Component List

Reference	Description	Manufacturer and Part Number
C1, C2, C3	10 μF, 6.3 V, 0603, X5R, ceramic	Murata, GRM188R60J106ME84D
C4	100 nF, 10 V, 0603, X7R, ceramic	Murata, GRM188R71H104KA93D
L1	2.2 μH, 2.2 A, 90 mΩ, 2.5 mm × 2.0 mm × 1.2 mm	Toko, 1239AS-H-2R2M
R1	Depending on the output voltage, 1%, (all measurements with ±5 V output voltage uses 365 kΩ)	
R2	Depending on the output voltage, 1%, (all measurements with ±5 V output voltage uses 120 kΩ)	
R3	Depending on the output voltage, 1%, (all measurements with ±5 V output voltage uses 487 kΩ)	
U1	TPS65135RTE	Texas Instruments

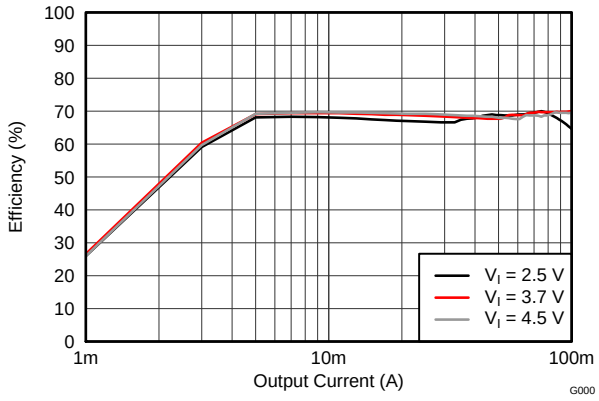
8.2.3 Application Curves

In the following curves V_I = 3.7 V, $V_{O(POS)}$ = 5 V, $V_{O(NEG)}$ = –5 V unless otherwise noted. Where the symbol I_O is used, it implies that $I_{O(POS)} = |I_{O(NEG)}|$. All measurements at T_A = 25°C unless otherwise noted.



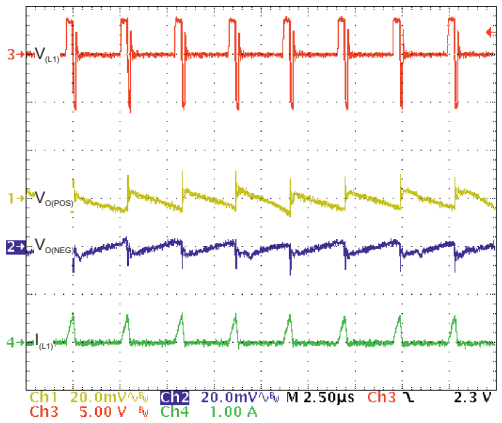
L1 = 2.2 µH

Figure 10. Efficiency vs Load Current



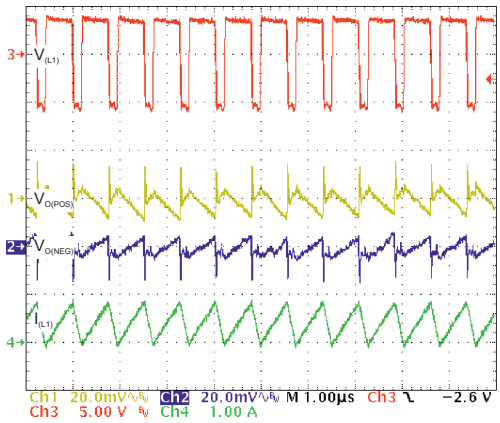
L1 = 4.7 µH

Figure 11. Efficiency vs Load Current



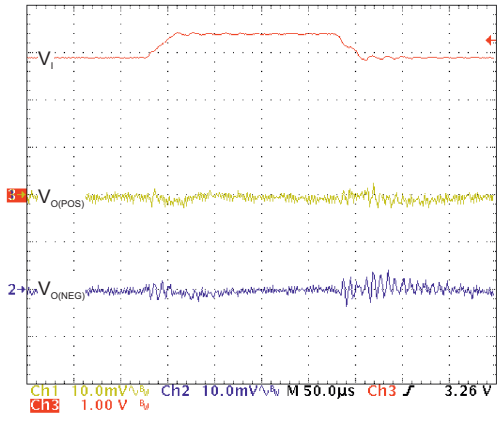
I_O = 10 mA

Figure 12. Operation at Light Load Current (DCM)



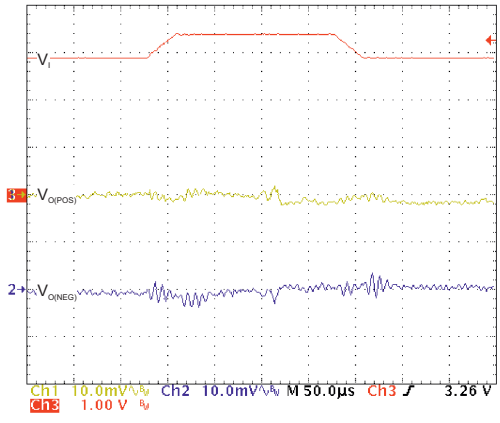
I_O = 80 mA

Figure 13. Operation at High Load Current (CCM)



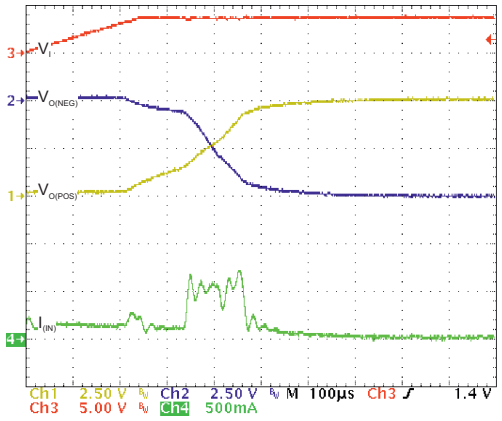
I_O = 10 mA V_I = 2.9 V, 3.4 V

Figure 14. Line Transient Response



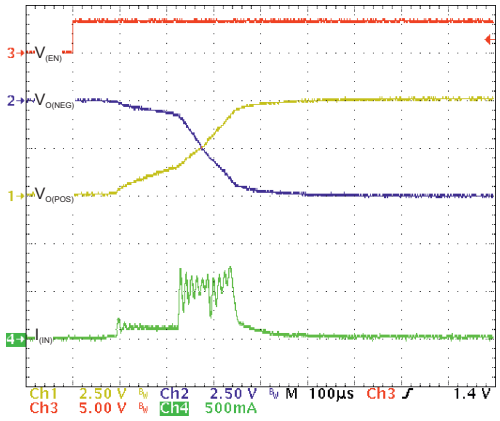
I_O = 50 mA V_I = 2.9 V, 3.4 V

Figure 15. Line Transient Response



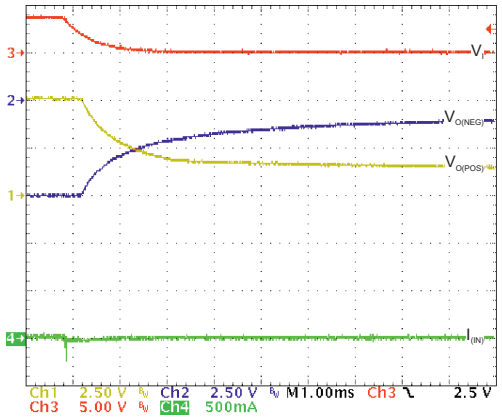
I_O = 0 mA

Figure 16. Start Up (V_I Rising)



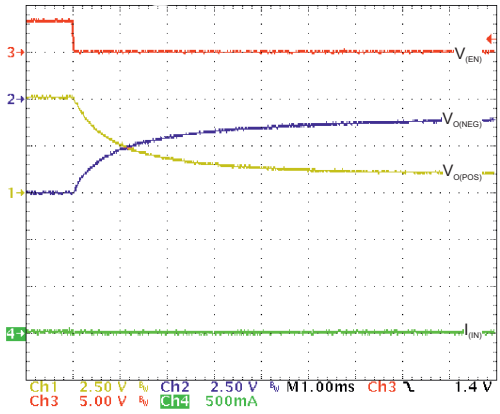
I_O = 0 mA

Figure 17. Start Up ($V_{(EN)}$ Rising)



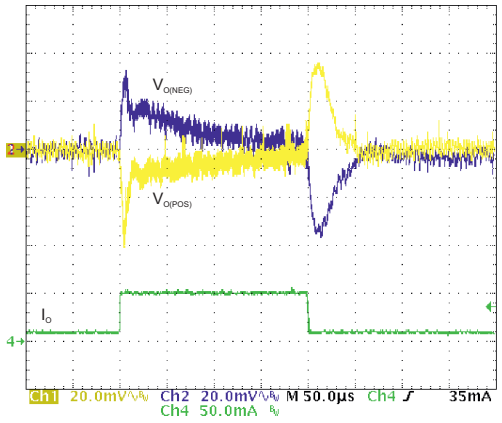
I_O = 0 mA

Figure 18. Shut Down – (V_I Falling)



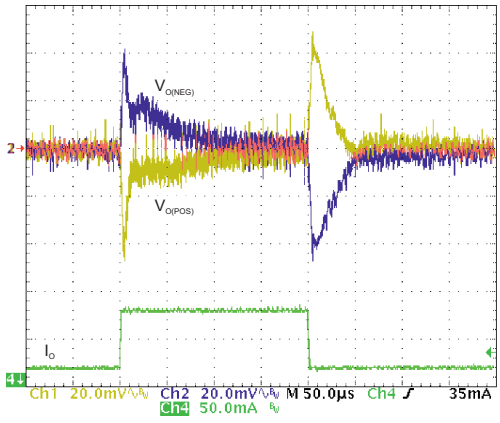
I_O = 0 mA

Figure 19. Shut Down ($V_{(EN)}$ Falling)



I_O = 10 mA, 50 mA

Figure 20. Load Transient Response



I_O = 20 mA, 80 mA

Figure 21. Load Transient Response

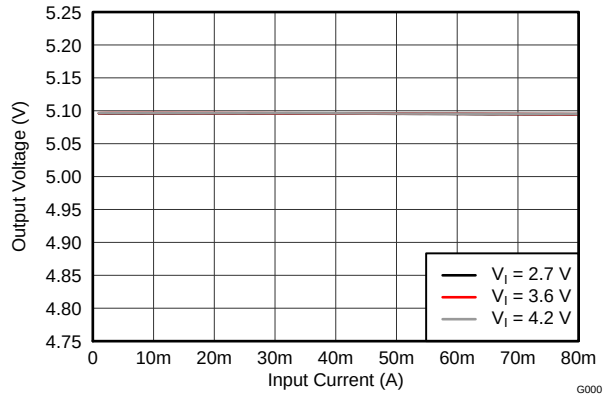


Figure 22. Positive Output Load Regulation

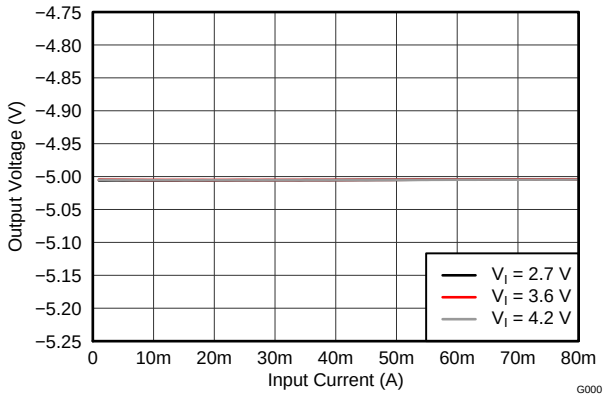


Figure 23. Negative Output Load Regulation

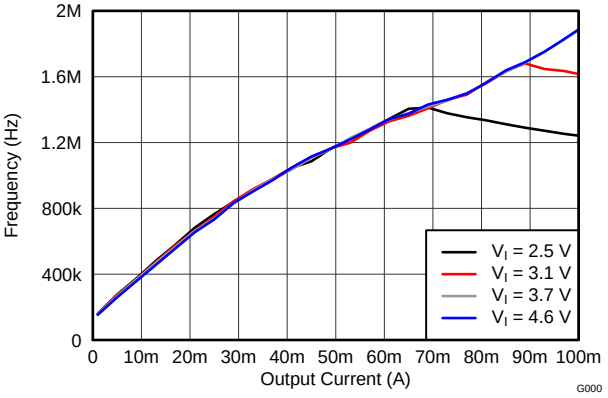


Figure 24. Switching Frequency vs Load Current

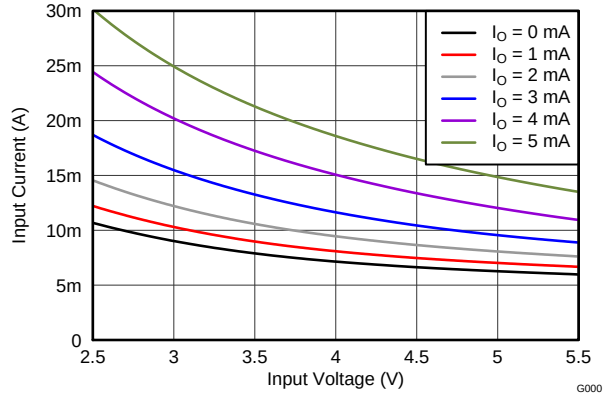


Figure 25. Input Current vs Input Voltage

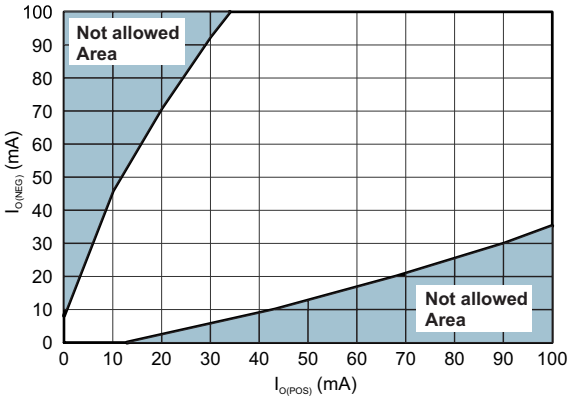


Figure 26. Output Current Mismatch

9 Power Supply Recommendations

The TPS65135 device is designed to operate from an input supply voltage in the range 2.5 V to 5.5 V. If the input supply is located more than a few centimeters from the device additional bulk capacitance may be required. The 10-μF shown in the schematics in this data sheet are typical for this function.

10 Layout

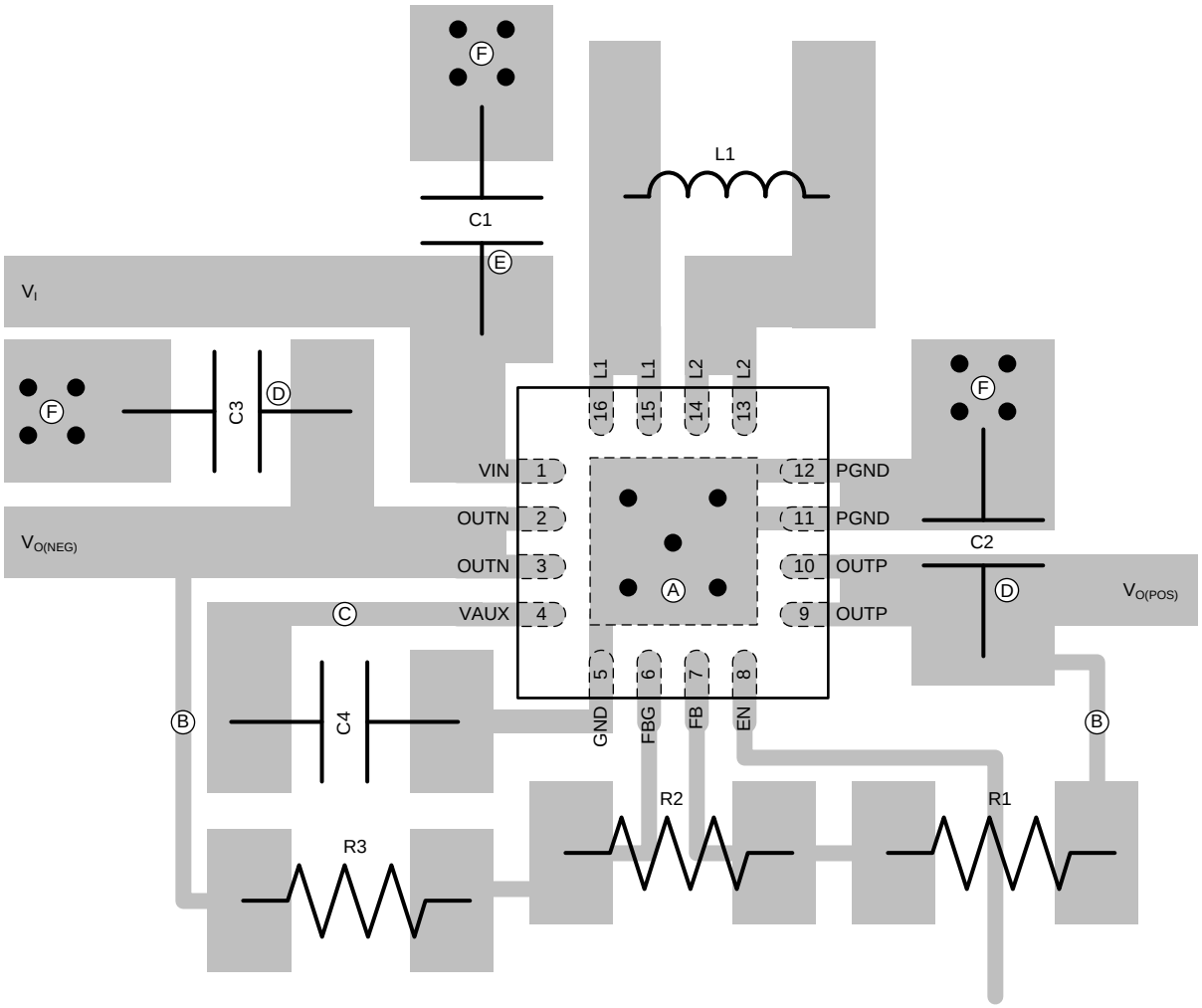
10.1 Layout Guidelines

No PCB layout is perfect, and compromises are always necessary. However, the basic principles listed below (in order of importance) go a long way to achieving the full performance of the TPS65135 device.

- If possible, route discontinuous switching currents on the top layer, using short, wide traces to minimize stray inductance and resistance. For the TPS65135 device, the current flowing into the VIN, L1, L2, VPOS, VNEG and PGND pins is discontinuous. In the example layout below, vias are used to connect discontinuous return currents to the ground plane, as it is considered a slightly better approach with this device than forcing all currents to flow on the top layer.
- Place C1 and C4 as close as possible to the VIN and AVIN pins respectively.
- Place C2 and C3 as close as possible to the VPOS and VNEG pins respectively.
- Place L1 as close as possible to the L1 and L2 pins.
- Use a copper pour (preferably on layer 2) as a thermal spreader and connect it to the exposed thermal pad using the maximum number of thermal vias (see packaging information for more information on the recommended thermal vias).
- The copper pour described above can be used as a ground plane if it is not possible to route power ground signals on the top layer.

10.2 Layout Example

Figure 27 shows an example PCB layout based on the above principles.



Ⓐ Multiple vias used to connect thermal pad to copper pour on bottom or inner layer to conduct heat away and minimize loop area.

Ⓑ Output voltages sensed directly at output capacitors. Sensing traces kept separate from high-current-carrying traces.

Ⓒ C4 placed close to VAUX and GND pins. Traces connecting to C4 do not need to be especially wide, because they do not conduct high current.

Ⓓ C2 and C3 placed close to OUTP and OUTN pins and connected with wide traces to minimize parasitic inductance.

Ⓔ C1 placed close to VIN pin and connected with very wide traces to minimize parasitic inductance.

Ⓕ PGND connected to copper pour ground plane on bottom or inner layer to minimize loop area.

Figure 27. PCB Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

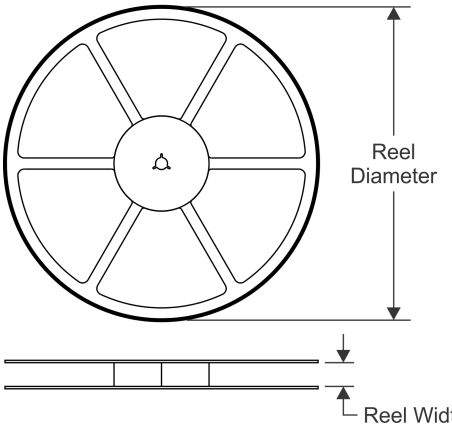
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

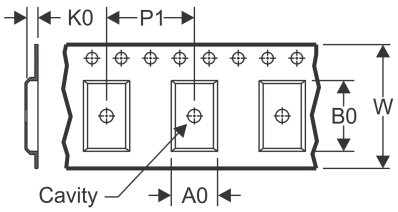
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

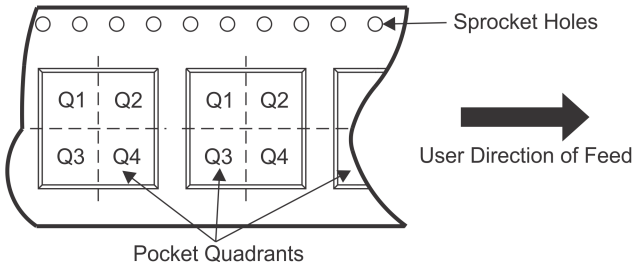


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

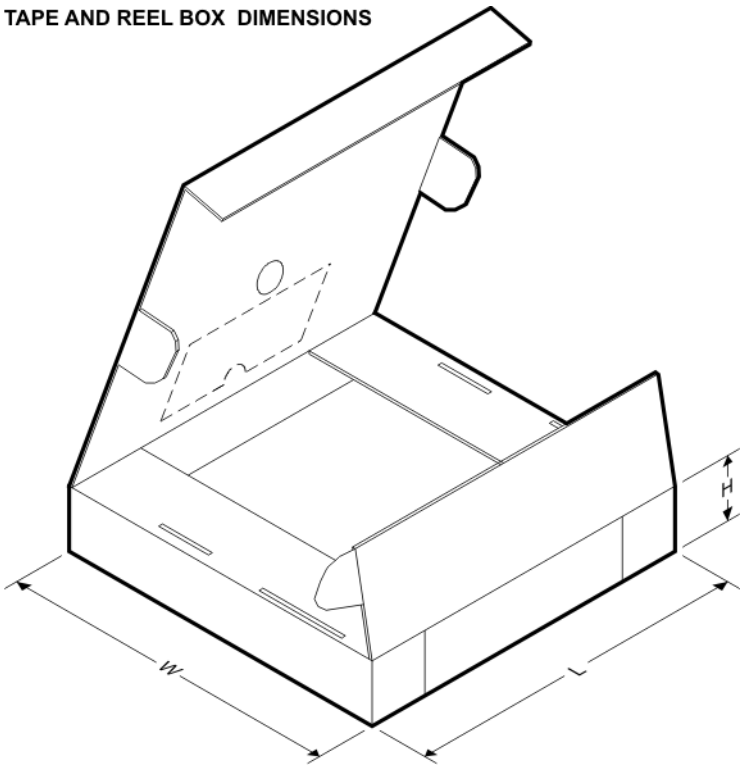
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65135RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

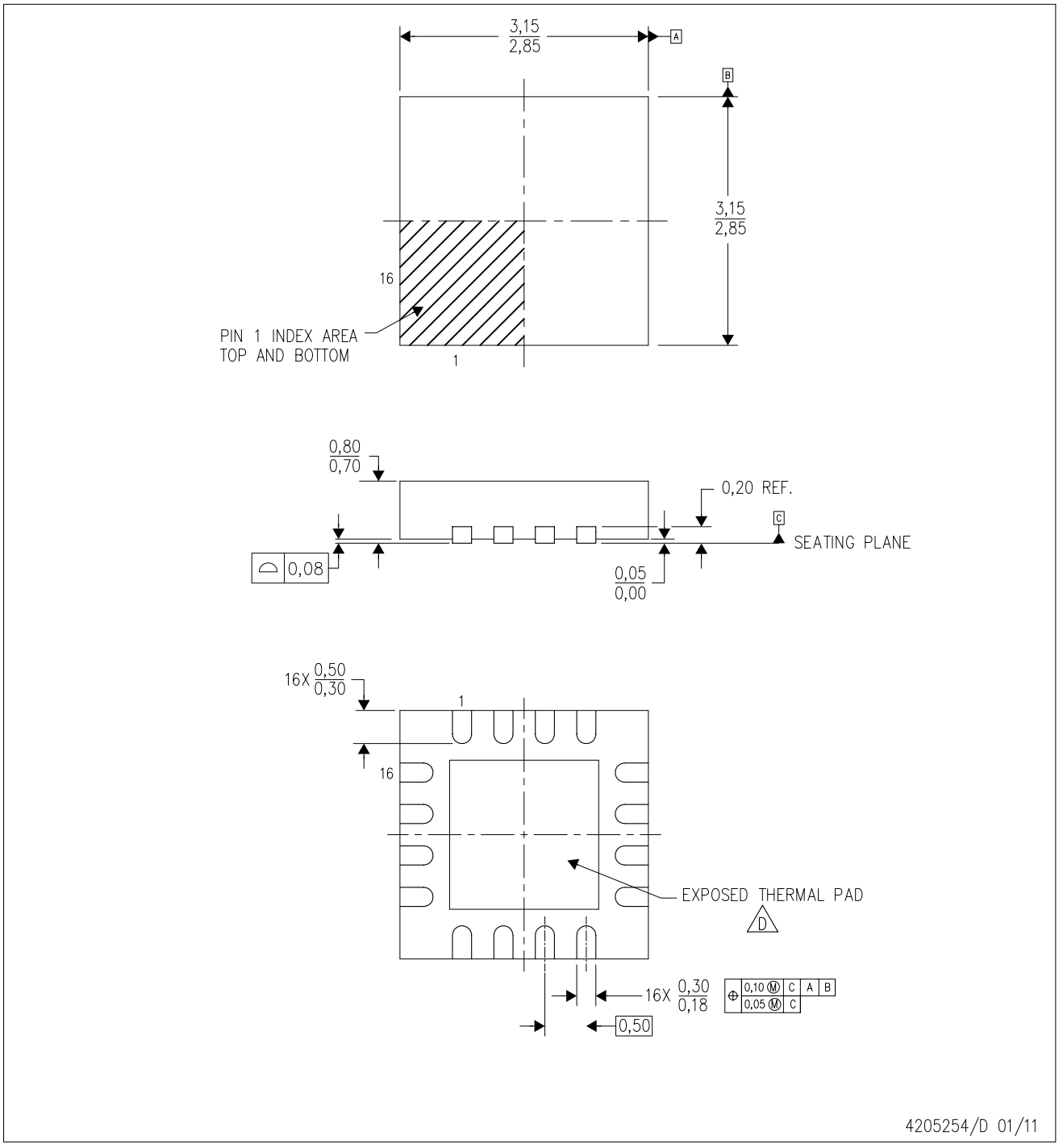
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65135RTER	WQFN	RTE	16	3000	367.0	367.0	35.0

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

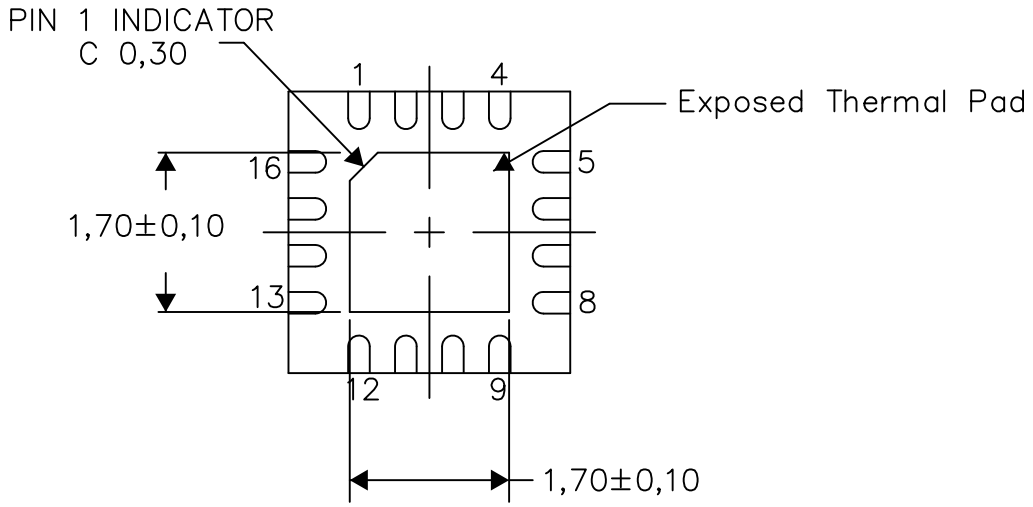
RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



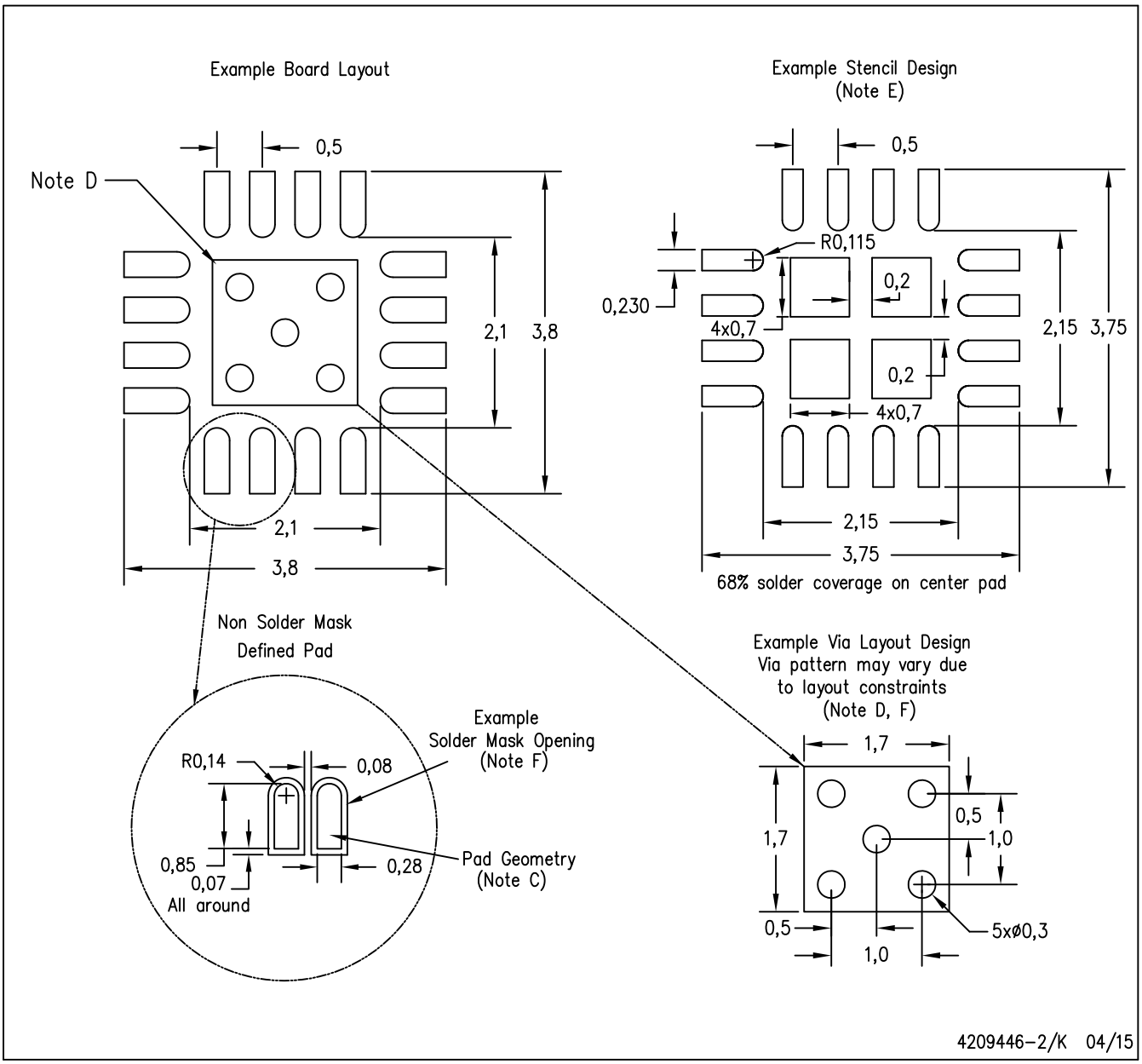
Bottom View

Exposed Thermal Pad Dimensions

4206446–3/U 08/15

NOTE: A. All linear dimensions are in millimeters

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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