TPS65217x Single-Chip PMIC for Battery-Powered Systems

1 Features

- ***CHARGER and POWER PATH***
  - 2-A Output Current on Power Path
  - Linear Charger; 700-mA Maximum Charge Current
  - 20-V Tolerant USB and AC Inputs
  - Thermal Regulation, Safety Timers
  - Temperature Sense Input
- ***STEP-DOWN CONVERTER (DCDC1, -2, -3)***
  - Three Step-Down Converter With Integrated Switching FETs
  - 2.25-MHz Fixed Frequency Operation
  - Power-Save Mode at Light Load Current
  - Output Voltage Accuracy in PWM Mode ±2%
  - 100% Duty Cycle for Lowest Dropout
  - Typical 15-µA Quiescent per Converter
  - Passive Discharge to Ground When Disabled
- ***LDOs (LDO1, -2)***
  - Two Adjustable LDOs
  - LDO2 Can Be Configured to Track DCDC3
  - Typical 15-µA Quiescent Current
- ***LOAD SWITCHES (LDO3, -4)***
  - Two Independent Load Switches That Can Be Configured as LDOs
- ***WLED DRIVER***
  - Internally Generated PWM for Dimming Control
  - 38-V Open-LED Protection
  - Supports Two Strings of Up To 10 LEDs at 25 mA Each
  - Internal Low-Side Current Sinks
- ***PROTECTION***
  - Undervoltage Lockout and Battery Fault Comparator
  - Always-On Push-Button Monitor
  - Hardware Reset Pin
  - Password Protected I^2C Registers
- ***INTERFACE***
  - I^2C Interface (Address 0x24)
  - Password Protected I^2C Registers

2 Applications

- AM335x ARM® Cortex™-A8 Microprocessors
- Portable Navigation Systems
- Tablet Computing
- 5-V Industrial Equipment

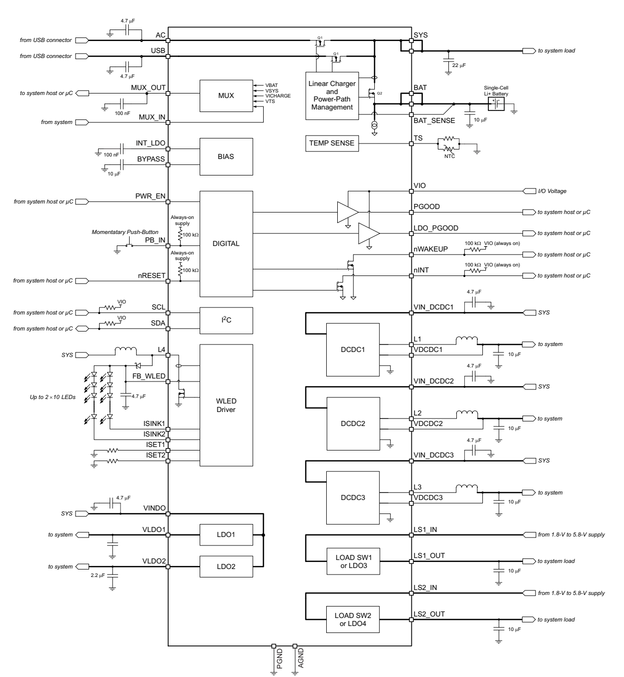
3 Description

The TPS65217 is a single-chip power management IC specifically designed to support applications in portable and 5-V non-portable applications. It provides a linear battery charger for single-cell Li-ion and Li-polymer batteries, dual-input power path, three step-down converters, four LDOs, and a high-efficiency boost converter to power two strings of up to 10 LEDs each. The system can be supplied by any combination of USB port, 5-V ac adaptor, or Li-Ion battery. The device is characterized across a –40°C to 105°C temperature range which makes it suitable for industrial applications. Three high-efficiency 2.25-MHz step-down converters can providing the core voltage, memory, and I/O voltage for a system.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS65217A	VQFN (48)	6.00 mm x 6.00 mm
TPS65217B		
TPS65217C		
TPS65217D		

(1) For all available packages, see the orderable addendum at the end of the datasheet.



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4 Revision History

Changes from Revision G (January 2015) to Revision H — **Page**

- Added a Reference Design button to the top of the first page 1
- Revised Figure 4 20
- Reversed STROBE 14 and STROBE 15 in the second paragraph of Special Strobes (STROBE 14 and 15) 22
- Changed PFMENx bit value required to force PWM operation at light loads from 0 to 1 34
- Changed text in RESET paragraph 38
- Changed Figure 20 39
- Added a row to Table 36 78
- *Added Receiving Notification...* and *Community Resources* sections 83

Changes from Revision F (April 2013) to Revision G — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

5 Description (continued)

These step-down converters enter a low-power mode at light load for maximum efficiency across the widest possible range of load currents. For low-noise applications the devices can be forced into fixed-frequency PWM using the I^2C interface. The step-down converters allow the use of small inductors and capacitors to achieve a small solution size.

LDO1 and LDO2 can support system-standby mode. In SLEEP state, output current is limited to 1 mA to reduce quiescent current whereas in normal operation they can support up to 100 mA each. LDO3 and LDO4 can be configured to support up to 400 mA each and can be configured as load switches instead of regulators. All four LDOs have a wide input voltage range that allows them to be supplied either from one of the dc-dc converters or directly from the system voltage node.

By default only LDO1 is always ON but any rail can be configured to remain up in SLEEP state. Especially the dc-dc converters can remain up in a low-power PFM mode to support system suspend mode.

The TPS65217 offers configurable power-up and power-down sequencing and several housekeeping functions such as power-good output, pushbutton monitor, hardware reset function and temperature sensor to protect the battery.

For details on specific applications please see our application note SLVU551.

The TPS65217 comes in a 48-pin leadless package (6-mm x 6-mm QFN) with a 0.4-mm pitch.

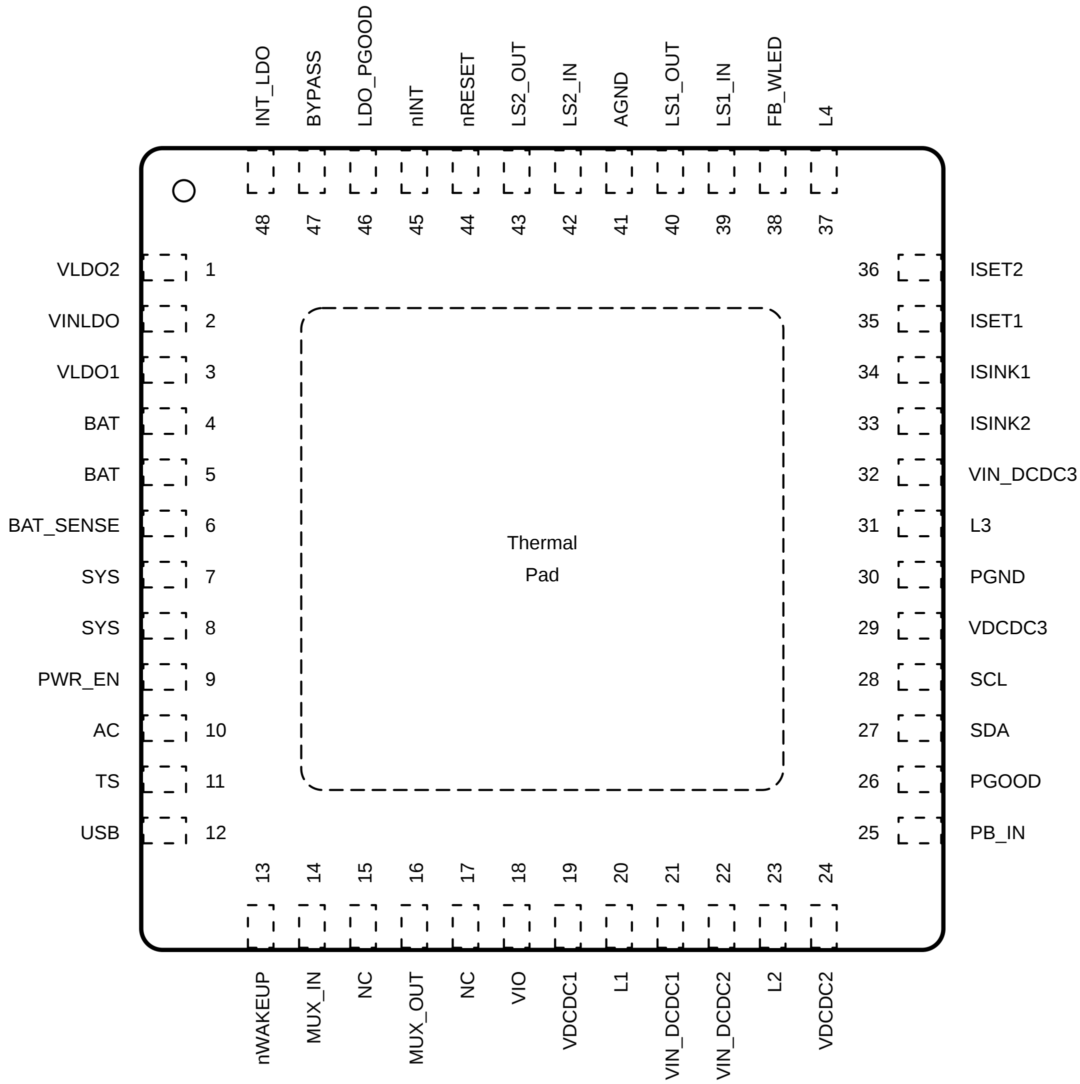
6 Device Comparison Table(1)

	TPS65217A (Targeted at AM335x - ZCE)		TPS65217B (Targeted at AM335x - ZCZ)		TPS65217C (Targeted at AM335x - ZCZ)		TPS65217D (Targeted at AM335x - ZCZ)	
	VOLTAGE (V)	SEQUENCE (STROBE)	VOLTAGE (V)	SEQUENCE (STROBE)	VOLTAGE (V)	SEQUENCE (STROBE)	VOLTAGE (V)	SEQUENCE (STROBE)
DCDC1	1.8	1	1.8	1	1.5	1	1.35	1
DCDC2	3.3	2	1.1	5	1.1	5	1.1	5
DCDC3	1.1	3	1.1	5	1.1	5	1.1	5
LDO1(1)	1.8	15	1.8	15	1.8	15	1.8	15
LDO2	3.3	2	3.3	2	3.3	3	3.3	3
LS1 or LDO3	Load switch	1	3.3 (LDO, 200 mA)	3	1.8 (LDO, 400 mA)	2	1.8 (LDO, 400 mA)	2
LS2 or LDO4	Load switch	4	3.3 (LDO, 200 mA)	4	3.3 (LDO, 400 mA)	4	3.3 (LDO, 400 mA)	4

(1) See *RESET* in *Modes of Operation* for more information.
(1) Strobe 15 (LDO1) is the first rail to be enabled in a sequence, followed by strobe 1-7. See *Wake-Up and Power-Up Sequencing* for details.

7 Pin Configuration and Functions

RSL Package
48-Pin VQFN With Exposed Thermal Pad
Top View



NC – No internal connection

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AC	10	I	AC adapter input to power path. Connect to an external dc supply.
AGND	41	—	Analog GND, connect to PGND (PowerPad)
BAT	4, 5	I/O	Battery charger output. Connect to battery.
BAT_SENSE	6	I	Battery voltage sense input, connect to BAT directly at the battery terminal.
BYPASS	47	O	Internal bias voltage (2.25 V). It is not recommended to connect any external load to this pin.
FB_WLED	38	I	Feedback pin for WLED boost converter. Also connected to the Anode of the WLED strings.
INT_LDO	48	O	Internal bias voltage (2.3 V). It is not recommended to connect any external load to this pin.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
ISET1	35	I	Low-level WLED current set. Connect a resistor to ground to set the WLED low-current level.
ISET2	36	I	High-level WLED current set. Connect a resistor to ground to set the WLED high-current level.
ISINK1	34	I	Input to the WLED current SINK1. Connect to the cathode of the WLED string. Current through SINK1 equals current through ISINK2. If only one WLED string is used, short ISINK1 and ISINK2 together.
ISINK2	33	I	Input to the WLED current SINK2. Connect to the cathode of the WLED string. Current through SINK1 equals current through ISINK2. If only one WLED string is used, short ISINK1 and ISINK2 together.
L1	20	O	Switch pin for DCDC1. Connect to inductor.
L2	23	O	Switch pin for DCDC2. Connect to inductor.
L3	31	O	Switch pin for DCDC3. Connect to Inductor.
L4	37	O	Switch pin of the WLED boost converter. Connected to Inductor.
LDO_PGOOD	46	O	LDO power good (LDO1 and LDO2 only, push-pull output). Pulled low when either LDO1 or LDO2 is out of regulation.
LS1_IN	39	I	Input voltage pin for load switch 1 or LDO3
LS1_OUT	40	O	Output voltage pin for load switch 1 or LDO3
LS2_IN	42	I	Input voltage pin for load switch 2 or LDO4
LS2_OUT	43	O	Output voltage pin for load switch 2 or LDO4
MUX_IN	14	O	Input to analog multiplexer
MUX_OUT	16	O	Output pin of analog multiplexer
NC	15, 17		Not used
nINT	45	O	Interrupt output (active-low, open-drain). Pin is pulled low if an interrupt bit is set. The output goes high after the bit causing the interrupt in register INT has been read. The interrupt sources can be masked in register INT, so no interrupt is generated when the corresponding interrupt bit is set.
nRESET	44	I	Reset pin (active-low). Pulling this pin low causes the PMIC to shut down, and after 1s to power up in its default state.
nWAKEUP	13	O	Signal to host to indicate a power on event (active-low, open-drain output)
PB_IN	25	I	Push-button monitor input. Typically connected to a momentary switch to ground (active-low).
PGND	30		Power ground. Connect to ground plane.
PGOOD	26	O	Power-good output (push-pull output). Pulled low when any of the power rails are out of regulation. Behavior is register programmable.
PWR_EN	9	I	Enable input for DCDC1, DCDC2, DCDC3 converters and LDO1, LDO2, LDO3, LDO4. Pull this pin high to start the power-up sequence.
SCL	28	I	Clock input for the I^2C interface
SDA	27	I/O	Data line for the I^2C interface
SYS	7, 8	O	System voltage pin and output of the power path. All voltage regulators are typically powered from this output.
TS	11	I	Temperature sense input. Connect to NTC thermistor to sense battery temperature. Works with 10k and 100k thermistors. See charger section for details.
USB	12	I	USB voltage input to power path. Connect to external voltage from a USB port.
VDCDC1	19	I	DCDC1 output and feedback voltage-sense input
VDCDC2	24	I	DCDC2 output and feedback voltage-sense input
VDCDC3	29	I	DCDC3 output and feedback voltage-sense input
VINLDO	2	I	Input voltage for LDO1 and LDO2
VIN_DCDC1	21	I	Input voltage for DCDC1. Must be connected to SYS pin.
VIN_DCDC2	22	I	Input voltage for DCDC2. Must be connected to SYS pin.
VIN_DCDC3	32	I	Input voltage for DCDC3. Must be connected to SYS pin.

Pin Functions (continued)

PIN NAME	PIN NO.	I/O	DESCRIPTION
VIO	18	I	Output-high supply for output buffers
VLDO1	3	O	Output voltage of LDO1
VLDO2	1	O	Output voltage of LDO2
Thermal pad	—	—	Power ground connection for the PMU. Connect to GND

8 Specifications

8.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) (1)(2)

			MIN	MAX	UNIT
	Supply voltage (with respect to PGND)	BAT	–0.3	7	V
		USB, AC	–0.3	20	
	Input/output voltage (with respect to PGND)	All pins unless specified separately	–0.3	7	V
		ISINK	–0.3	20	
		L4, FB_WLED	–0.3	44	
	Absolute voltage difference between SYS and any VIN_DCDCx pin or SYS and VINLDO		0.3	0.3	V
	Terminal current	SYS, USB, BAT	3000	3000	mA
	Source or Sink current	PGOOD, LDO_PGOOD	6	6	mA
	Sink current	nWAKEUP, nINT	2	2	mA
T_J	Operating junction temperature		125	125	°C
T_A	Operating ambient temperature		–40	105	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, USB, AC	4.3		5.8	V
Supply voltage, BAT	2.75		5.5	V
Input current from AC			2.5	A
Input current from USB			1.3	A
Battery current			2	A
Input voltage range for DCDC1, DCDC2, and DCDC3	2.7		5.8	V
Input voltage range for LDO1, LDO2	1.8		5.8	V
Input voltage range for LS1 or LDO3, LS2 or LDO4 configured as LDOs	2.7		5.8	V
Input voltage range for LS1 or LDO3, LS2 or LDO4 configured as load switches	1.8		5.8	V
Output voltage range for LDO1	1		3.3	V

Recommended Operating Conditions (continued)

over operating ambient temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Output voltage range for LDO2		0.9		3.3	V
Output voltage range for LS1 or LDO3, LS2 or LDO4		1.8		3.3	V
Output current DCDC1		0		1.2	A
Output current DCDC2		0		1.2	A
Output current DCDC3		0		1.2	A
Output current LDO1, LDO2		0		100	mA
Output current LS1 or LDO3, LS2 or LDO4 configured as LDOs	TPS65217A	0		200	mA
	TPS65217B	0		200	
	TPS65217C	0		400	
	TPS65217D	0		400	
Output current LS1 or LDO, LS2 or LDO4 configured as load switches		0		200	mA

8.4 Thermal Information

THERMAL METRIC(1)		TPS65217 RSL (VQFN) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	16.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

8.5 Electrical Characteristics

V_{BAT} = 3.6 V ±5%, T_J = 27ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT VOLTAGE AND CURRENTS							
V_{BAT}	Battery input voltage range	USB or AC supply connected		0		5.5	V
		USB and AC not connected		2.75		5.5	
V_{AC}	AC adapter input voltage range	Valid range for charging		4.3		5.8	V
V_{USB}	USB input voltage range	Valid range for charging		4.3		5.8	V
V_{UVLO}	Undervoltage lockout	Measured in respect to V_{BAT}; supply falling; V_{AC} = V_{USB} = 0 V	UVLO[1:0] = 00		2.73		V
			UVLO[1:0] = 01		2.89		
			UVLO[1:0] = 10		3.18		
			UVLO[1:0] = 11		3.3		
	Accuracy			–2%		2%	
	Deglitch time(1)			4		6	ms
V_{OFFSET}	AC and USB UVLO offset	V_{BAT} < V_{UVLO}; Device shuts down when V_{AC}, V_{USB} drop below V_{UVLO} + V_{OFFSET}			200		mV
I_{OFF}	OFF current, Total current into VSYS, VINDCDCx, VINLDO	All rails disabled, T_A = 27°C			6		µA
I_{SLEEP}	Sleep current, Total current into VSYS, VINDCDCx, VINLDO	LDO1 and LDO2 enabled, no load. All other rails disabled. V_{SYS} = 4 V, T_A = 0.105°C			80	106	µA
POWER PATH AC AND USB DETECTION LIMITS							

(1) Not tested in production

Electrical Characteristics (continued)

V_{BAT} = 3.6 V ±5%, T_J = 27ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IN(DT)}$	AC and USB voltage-detection threshold	$V_{BAT} > V_{UVLO}$, AC and USB valid when $V_{AC-USB} – V_{BAT} > V_{IN(DT)}$	190			mV
		$V_{BAT} < V_{UVLO}$, AC and USB valid when $V_{AC-USB} > V_{IN(DT)}$	4.3			V
$V_{IN(NDT)}$	AC and USB voltage-removal detection threshold	$V_{BAT} > V_{UVLO}$, AC and USB invalid when $V_{AC/USB} – V_{BAT} < V_{IN(DT)}$			125	mV
		$V_{BAT} < V_{UVLO}$, AC and USB invalid when $V_{AC-USB} < V_{IN(DT)}$		V_{UVLO} + V_{OFFSET}		V
t_{RISE}	V_{AC}, V_{USB} rise time	Voltage rising from 100 mV to 4.5 V. If rise time is exceeded, device may not power up.			50	ms
$t_{DG(DT)}$	Power detected deglitch[(1)]	AC or USB voltage increasing		22.5		ms
$V_{IN(OVP)}$	Input overvoltage detection threshold	USB and AC input	5.8	6	6.4	V
POWER PATH TIMING						
$t_{SW(PSEL)}$	Switching from AC to USB[(1)]				150	µs
POWER PATH MOSFET CHARACTERISTICS						
$V_{DO, AC}$	AC input switch dropout voltage	IAC[1:0] = 11 (2.5 A), I_{SYS} = 1 A		150		mV
$V_{DO, USB}$	USB input switch dropout voltage	IUSB[1:0] = 01 (500 mA), I_{SYS} = 500 mA		100		mV
		IUSB[1:0] = 10 (1300 mA), I_{SYS} = 800 mA		160		
$V_{DO, BAT}$	Battery switch dropout voltage	V_{BAT} = 3 V, I_{BAT} = 1 A		60		mV

Electrical Characteristics (continued)

V_{BAT} = 3.6 V ±5%, T_J = 27ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER PATH INPUT CURRENT LIMITS						
I_{ACLMT}	Input current limit; AC pin	IAC[1:0] = 00	90		130	mA
		IAC[1:0] = 01	480		580	
		IAC[1:0] = 10	1000	1500		
		IAC[1:0] = 11	2000	2500		
I_{USBLMT}	Input current limit; USB pin	IUSB[1:0] = 00	90		100	mA
		IUSB[1:0] = 01	460		500	
		IUSB[1:0] = 10	1000	1300		
		IUSB[1:0] = 11	1500	1800		
I_{BAT}	Battery load current(1)				2	A
POWER PATH BATTERY SUPPLEMENT DETECTION						
V_{BSUP}	Battery supplement threshold	V_{SYS} ≤ V_{BAT} – VBSUP1, V_{SYS} falling IUSB[1:0] = 10		40		mV
	Hysteresis	V_{SYS} rising		20		
POWER PATH BATTERY PROTECTION						
$V_{BAT(SC)}$	BAT pin short-circuit detection threshold		1.3	1.5	1.7	V
$I_{BAT(SC)}$	Source current for BAT pin short-circuit detection			7.5		mA
INPUT BASED DYNAMIC POWER MANAGEMENT						
V_{DPPM}	Threshold at which DPPM loop is enabled	I^2C selectable	3.5		4.25	V
BATTERY CHARGER						
V_{OREG}	Battery charger voltage	I^2C selectable	4.1		4.25	V
	Accuracy		–2%		1%	
V_{LOWV}	Precharge to fast-charge transition threshold	VPRECHG = 0		2.9		V
		VPRECHG = 1		2.5		
$t_{DGL1(LOWV)}$	Deglitch time on precharge to fast-charge transition(1)			25		ms
$t_{DGL2(LOWV)}$	Deglitch time on fast-charge to precharge transition(1)			25		ms
I_{CHG}	Battery fast charge current range V_{OREG} > V_{BAT} > V_{LOWV}, V_{IN} = V_{USB} = 5 V	ICHRG[1:0] = 00		300		mA
		ICHRG[1:0] = 01		400		
		ICHRG[1:0] = 10	450	500	550	
		ICHRG[1:0] = 11		700		
I_{PRECHG}	Precharge current	ICHRG[1:0] = 00		30		mA
		ICHRG[1:0] = 01		40		
		ICHRG[1:0] = 10	25	50	75	
		ICHRG[1:0] = 11		70		
I_{TERM}	Charge current value for termination detection threshold (fraction of I_{CHG})	TERMIF[1:0] = 00		2.5%		
		TERMIF[1:0] = 01	3%	7.5%	10%	
		TERMIF[1:0] = 10		15%		
		TERMIF[1:0] = 11		18%		
$t_{DGL(TERM)}$	Deglitch time, termination detected(1)			125		ms
V_{RCH}	Recharge detection threshold	Voltage below V_{OREG}	150	100	70	mV
$t_{DGL(RCH)}$	Deglitch time, recharge threshold detected(1)			125		ms
$I_{BAT(DET)}$	Sink current for battery detection	T_J = 27°C	3	7.5	10	mA
t_{DET}	Battery detection timer. $I_{BAT(DET)}$ is pulled from the battery for t_{DET}. If BAT voltage remains above V_{RCH} threshold the battery is connected.(1)	V_{BAT} < $V_{RCH;}$		250		ms
t_{CHG}	Charge safety timer(1)	Safety timer range, thermal and DPPM not active, selectable by I^2C	4		8	h

Electrical Characteristics (continued)

V_{BAT} = 3.6 V ±5%, T_J = 27ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PRECHG}	Precharge timer(1)	Pre charge timer, thermal and DPPM loops not active, selectable by I^2C	PCHRGT = 0		30	60	min
			PCHRGT = 1		60		min
BATTERY NTC MONITOR							
t_{THON}	Thermistor power on time at charger off, sampling mode on				10		ms
t_{THOFF}	Thermistor power sampling period at charger off, sampling mode on				1		s
R_{NTC_PULL}	Pullup resistor from thermistor to Internal LDO . I2C selectable	NTC_TYPE = 1 (10-kΩ NTC)			7.35		kΩ
		NTC_TYPE = 0 (100-kΩ NTC)			60.5		kΩ
	Accuracy	T_A = 27°C		–3%		3%	
V_{LTF}	Low-temperature failure threshold	Temperature falling			1660		mV
		Temperature rising			1610		mV
V_{HTF}	High-temperature failure threshold	Temperature falling	TRANGE = 0		910		mV
		Temperature rising	TRANGE = 0		860		mV
		Temperature falling	TRANGE = 1		667		mV
		Temperature rising	TRANGE = 1		622		mV
V_{DET}	Thermistor detection threshold			1750		1850	mV
t_{BATDET}	Thermistor not detected. Battery not present deglitch(1)				26		ms
THERMAL REGULATION							
$T_{J(REG)}$	Temperature regulation limit, temperature at which charge current is reduced			111		123	°C
DCDC1 (BUCK)							
V_{IN}	Input voltage range	VIN_DCDC1 pin		2.7		V_{SYS}	V
$I_{Q,SLEEP}$	Quiescent current in SLEEP mode	No load, V_{SYS} = 4 V, T_A = 25°C			30		µA
V_{OUT}	Output voltage range	External resistor divider (XADJ1 = 1)		0.6		V_{IN}	V
		I^2C selectable in 25-mV steps (XADJ1 = 0)		0.9		1.8(2)	V
	DC output voltage accuracy	V_{IN} = V_{OUT} + 0.3 V to 5.8 V; 0 mA ≤ I_{OUT} ≤ 1.2 A		–2%		3%	
	Power-save mode (PSM) ripple voltage	I_{OUT} = 1 mA, PFM mode L = 2.2 µH, C_{OUT} = 20 µF			40		mV_{pp}
I_{OUT}	Output current range			0		1.2	A
$r_{DS(on)}$	High-side MOSFET on-resistance	V_{IN} = 2.7 V			170		mΩ
	Low-side MOSFET on-resistance	V_{IN} = 2.7 V			120		mΩ
I_{LEAK}	High-side MOSFET leakage current	V_{IN} = 5.8 V				2	µA
	Low-side MOSFET leakage current	V_{DS} = 5.8 V				1	µA
I_{LIMIT}	Current limit (high- and low-side MOSFET).	2.7 V < V_{IN} < 5.8 V			1.6		A
f_{SW}	Switching frequency			1.95	2.25	2.55	MHz
V_{FB}	Feedback voltage	XADJ = 1			600		mV
t_{SS}	Soft-start time	Time to ramp V_{OUT} from 5% to 95%, no load			750		µs
R_{DIS}	Internal discharge resistor at L1(3)				250		Ω
L	Inductor			1.5	2.2		µH
C_{OUT}	Output capacitor	Ceramic		10	22		µF
	ESR of output capacitor				20		mΩ

(2) Contact factory for 3.3-V option.
(3) Can be factory disabled.

Electrical Characteristics (continued)

V_{BAT} = 3.6 V ±5%, T_J = 27ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DCDC2 (BUCK)						
V_{IN}	Input voltage range	VIN_DCDC2 pin	2.7		V_{SYS}	V
$I_{Q,SLEEP}$	Quiescent current in SLEEP mode	No load, V_{SYS} = 4 V, T_A = 25°C		30		µA
V_{OUT}	Output voltage range	External resistor divider (XADJ2 = 1)	0.6		V_{IN}	V
		I^2C selectable in 25-mV steps (XADJ2 = 0)	0.9		3.3	
	DC output voltage accuracy	V_{IN} = V_{OUT} + 0.3 V to 5.8 V; 0 mA ≤ I_{OUT} ≤ 1.2 A	–2%		3%	
	Power-save mode (PSM) ripple voltage	I_{OUT} = 1 mA, PFM mode L = 2.2 µH, C_{OUT} = 20 µF		40		mV_{pp}
I_{OUT}	Output current range		0		1.2	A
$r_{DS(on)}$	High-side MOSFET on-resistance	V_{IN} = 2.7 V		170		mΩ
	Low-side MOSFET on-resistance	V_{IN} = 2.7 V		120		
I_{LEAK}	High-side MOSFET leakage current	V_{IN} = 5.8 V			2	µA
	Low-side MOSFET leakage current	V_{DS} = 5.8 V			1	
I_{LIMIT}	Current limit (high and low side MOSFET).	2.7 V < V_{IN} < 5.8 V		1.6		A
f_{SW}	Switching frequency		1.95	2.25	2.55	MHz
V_{FB}	Feedback voltage	XADJ = 1		600		mV
t_{SS}	Soft-start time	Time to ramp V_{OUT} from 5% to 95%, no load		750		µs
R_{DIS}	Internal discharge resistor at L2			250		Ω
L	Inductor		1.5	2.2		µH
C_{OUT}	Output capacitor	Ceramic	10	22		µF
	ESR of output capacitor			20		mΩ
DCDC3 (BUCK)						
V_{IN}	Input voltage range	VIN_DCDC3 pin	2.7		V_{SYS}	V
$I_{Q,SLEEP}$	Quiescent current in SLEEP mode	No load, V_{SYS} = 4 V, T_A = 25°C		30		µA
V_{OUT}	Output voltage range	External resistor divider (XADJ3 = 1)	0.6		V_{IN}	V
		I^2C selectable in 25-mV steps (XADJ3 = 0)	0.9		1.5(2)	
	DC output voltage accuracy	V_{IN} = V_{OUT} + 0.3 V to 5.8 V; 0 mA ≤ I_{OUT} ≤ 1.2 A	–2%		3%	
	Power save mode (PSM) ripple voltage	I_{OUT} = 1 mA, PFM mode L = 2.2 µH, C_{OUT} = 20 µF		40		mV_{pp}
I_{OUT}	Output current range		0		1.2	A
$r_{DS(on)}$	High-side MOSFET on-resistance	V_{IN} = 2.7 V		170		mΩ
	Low side MOSFET on-resistance	V_{IN} = 2.7 V		120		
I_{LEAK}	High-side MOSFET leakage current	V_{IN} = 5.8 V			2	µA
	Low-side MOSFET leakage current	V_{DS} = 5.8 V			1	
I_{LIMIT}	Current limit (high- and low-side MOSFET).	2.7 V < V_{IN} < 5.8 V		1.6		A
f_{SW}	Switching frequency		1.95	2.25	2.55	MHz
V_{FB}	Feedback voltage	XADJ = 1		600		mV
t_{SS}	Soft-start time	Time to ramp V_{OUT} from 5% to 95%, no load		750		µs
R_{DIS}	Internal discharge resistor at L1, L2			250		Ω
L	Inductor		1.5	2.2		µH
C_{OUT}	Output capacitor	Ceramic	10	22		µF
	ESR of output capacitor			20		mΩ

Electrical Characteristics (continued)

V_{BAT} = 3.6 V ±5%, T_J = 27ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LDO1, LDO2						
V_{IN}	Input voltage range		1.8		5.8	V
$I_{Q,SLEEP}$	Quiescent current in SLEEP mode	No load, V_{SYS} = 4 V, T_A = 25°C		5		µA
V_{OUT}	Output voltage range	LDO1, I^2C selectable	1		3.3	V
		LDO2, I^2C selectable	0.9		3.3	
	DC output voltage accuracy	I_{OUT} = 10 mA, V_{IN} > V_{OUT} + 200 mV, V_{OUT} > 0.9 V	–2%		2%	
	Line regulation	V_{IN} = 2.7 V - 5.5 V, V_{OUT} = 1.2 V, I_{OUT} = 100 mA	–1%		1%	
	Load regulation	I_{OUT} = 1 mA - 100 mA, V_{OUT} = 1.2 V, V_{IN} = 3.3 V	–1%		1%	
		I_{OUT} = 0 mA - 1 mA, V_{OUT} = 1.2 V, V_{IN} = 3.3 V	–2.5%		2.5%	
I_{OUT}	Output current range	Sleep state	0		1	mA
		Active state	0		100	
I_{SC}	Short circuit current limit	Output shorted to GND	100	250		mA
V_{DO}	Dropout voltage	I_{OUT} = 100 mA, V_{IN} = 3.3 V			200	mV
R_{DIS}	Internal discharge resistor at output			430		Ω
C_{OUT}	Output capacitor	Ceramic		2.2		µF
	ESR of output capacitor			20		mΩ
LS1 OR LDO3, AND LS2 OR LDO4, CONFIGURED AS LDOs						
V_{IN}	Input voltage range		2.7		5.8	V
$I_{Q,SLEEP}$	Quiescent current in SLEEP mode	No load, V_{SYS} = 4 V, T_A = 25°C		30		µA
V_{OUT}	Output voltage range	LS1LDO3 = 1, LS2LDO4 =1 I^2C selectable	1.5		3.3	V
	DC output voltage accuracy	I_{OUT} = 10 mA, V_{IN} > V_{OUT} + 200 mV, V_{OUT} > 1.8 V	–2%		2%	
	Line regulation	V_{IN} = 2.7 V - 5.5 V, V_{OUT} = 1.8 V, I_{OUT} = 200 mA	–1%		1%	
	Load regulation	I_{OUT} = 1 mA - 200 mA, V_{OUT} = 1.8 V, V_{IN} = 3.3 V	–1%		1%	
I_{OUT}	Output current range	TPS65217A	0		200	mA
		TPS65217B	0		200	
		TPS65217C	0		400	
		TPS65217D	0		400	
I_{SC}	Short-circuit current limit	Output shorted to GND, TPS65217A	200	280		mA
		Output shorted to GND, TPS65217B	200	280		
		Output shorted to GND, TPS65217C	400	480		
		Output shorted to GND, TPS65217D	400	480		
V_{DO}	Dropout voltage	I_{OUT} = 200 mA, V_{IN} = 3.3 V			200	mV
R_{DIS}	Internal discharge resistor at output(3)			375		Ω
C_{OUT}	Output capacitor	Ceramic	8	10	12	µF
	ESR of output capacitor			20		mΩ
LS1 OR LDO3, AND LS2 OR LDO4, CONFIGURED AS LOAD SWITCHES						
V_{IN}	Input voltage range	LS1_VIN, LS2_VIN pins	1.8		5.8	V
$R_{DS(ON)}$	P-channel MOSFET on-resistance	V_{IN} = 1.8 V, over full temperature range		300	650	mΩ
I_{SC}	Short circuit current limit	Output shorted to GND	200	280		mA
R_{DIS}	Internal discharge resistor at output			375		Ω
C_{OUT}	Output capacitor	Ceramic	1	10	12	µF
	ESR of output capacitor			20		mΩ
WLED BOOST						
V_{IN}	Input voltage range		2.7		5.8	V

Electrical Characteristics (continued)

V_{BAT} = 3.6 V ±5%, T_J = 27ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Max output voltage	I_{SINK} = 20 mA	32			V
V_{OVP}	Output overvoltage protection		37	38	39	V
$R_{DS(ON)}$	N-channel MOSFET on-resistance	V_{IN} = 3.6 V		0.6		Ω
I_{LEAK}	N-channel leakage current	V_{DS} = 25 V, T_A = 25°C		2		µA
I_{LIMIT}	N-channel MOSFET current limit			1.6	1.9	A
f_{SW}	Switching frequency			1.125		MHz
I_{INRUSH}	Inrush current on start-up	V_{IN} = 3.6 V, 1% duty cycle setting		1.1		A
		V_{IN} = 3.6 V, 100% duty cycle setting		2.1		
L	Inductor			18		µH
C_{OUT}	Output capacitor	Ceramic		4.7		µF
	ESR of output capacitor			20		mΩ
WLED CURRENT SINK1, SINK2						
$V_{SINK1,2}$	Overvoltage protection threshold at ISINK1, ISINK2 pins				19	V
$V_{DO,\ SINK1,2}$	Current sink drop-out voltage	Measured from ISINK to GND		400		mV
$V_{ISET1,2}$	ISET1, ISET2 pin voltage			1.24		V
$I_{SINK1,2}$	WLED current range (ISINK1, ISINK2)		1		25	mA
	WLED sink current	R_{ISET} = 130.0 kΩ		10		
		R_{ISET} = 86.6 kΩ		15		
		R_{ISET} = 64.9 kΩ		20		
		R_{ISET} = 52.3 kΩ		25		
	DC current set accuracy	I_{SINK} = 5 mA to 25 mA, 100% duty cycle	–5%		5%	
	DC current matching	R_{SET1} = 52.3 kΩ, I_{SINK} = 25 mA, V_{BAT} = 3.6 V, 100% duty cycle	–5%		5%	
		R_{SET1} = 130 kΩ, I_{SINK} = 10 mA, V_{BAT} = 3.6 V, 100% duty cycle	–5%		5%	
f_{PWM}	PWM dimming frequency	FDIM[1:0] = 00		100		Hz
		FDIM[1:0] = 01		200		
		FDIM[1:0] = 10		500		
		FDIM[1:0] = 11		1000		
ANALOG MULTIPLEXER						
g	Gain, VBAT (V_{BAT} / $V_{OUT,MUX}$); VSYS (V_{SYS} / $V_{OUT,MUX}$)			3		V/V
	Gain, VTS (V_{TS} / $V_{OUT,MUX}$); MUX_IN (V_{MUX_IN} / V_{MUX_OUT})			1		
	Gain, $V_{ICHARGE}$ ($V_{OUT,MUX}$ / $V_{ICHARGE}$)	ICHRG[1:0] = 00b		7.575		V/A
		ICHRG[1:0] = 01b		5.625		
		ICHRG[1:0] = 10b		4.5		
		ICHRG[1:0] = 11b		3.214		
V_{OUT}	Buffer headroom (V_{SYS} – V_{MUX_OUT})	V_{SYS} = 3.6 V, MUX[2:0] = 101 (V_{MUX_IN} – V_{MUX_OUT}) / V_{MUX_IN} > 1%		0.7	1	V
R_{OUT}	Output Impedance			180		Ω
I_{LEAK}	Leakage current	MUX[2:0] = 000 (HiZ), V_{MUX} = 2.25 V			1	µA
LOGIC LEVELS AND TIMING CHARACTERISTICS (SCL, SDA, PB_IN, PGOOD, LDO_PGOOD, PWR_EN, nINT, nWAKEUP, nRESET)						
P_{GTH}	PGOOD comparator treshold, All dc-dc converters and LDOs(1)	Output voltage falling, % of set voltage		90%		
		Output voltage rising, % of set voltage		95%		

Electrical Characteristics (continued)

V_{BAT} = 3.6 V ±5%, T_J = 27ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_{GDG}	PGOOD deglitch time	Output voltage falling, DCDC1, DCDC2, DCDC3		2		4	ms
		Output voltage falling, LDO1, LDO2, LDO3, LDO4		1		2	
P_{GDLY}	PGOOD delay time	PGDLY[1:0] = 00			20		ms
		PGDLY[1:0] = 01			100		
		PGDLY[1:0] = 10			200		
		PGDLY[1:0] = 11			400		
t_{HRST}	PB-IN hard-reset-detect time (1)				8		s
t_{DG}	PB_IN pin deglitch time (1)				50		ms
	PWR_EN pin deglitch time (1)				50		
	nRESET pin deglitch time (1)				30		
R_{PULLUP}	PB_IN internl pullup resistor				100		kΩ
	nRESET internl pullup resistor				100		
V_{IH}	High level input voltage PB_IN, SCL, SDA, PWR_EN, nRESET			1.2		V_{IN}	V
V_{IL}	Low level input voltage PB_IN, SCL, SDA, PWR_EN, nRESET			0		0.4	V
I_{BIAS}	Input bias current PB_IN, SCL, SDA				0.01	1	µA
V_{OL}	Output low voltage	nINT, nWAKEUP	I_O = 1 mA			0.3	V
		PGOOD, LDO_PGOOD	I_O = 1 mA			0.3	
V_{OH}	Output high voltage	PGOOD, LDO_PGOOD	I_O = 1 mA	V_{IO} – 0.3			V
I_{LEAK}	Pin leakage current nINT, nWAKEUP	Pin pulled up to 3.3-V supply				0.2	µA
	I^2C slave address				0x24h		
OSCILLATOR							
f_{OSC}	Oscillator frequency				9		MHz
	Frequency accuracy	T_A = –40°C to 105°C		–10%		10%	
OVERTEMPERATURE SHUTDOWN							
T_{OTS}	Overtemperature shutdown	Increasing junction temperature			150		°C
	Hysteresis	Decreasing junction temperature			20		°C

8.6 Timing Requirements

V_{BAT} = 3.6 V ±5%, T_A = 25ºC, C_L = 100 pF (unless otherwise noted)

			MIN	NOM	MAX	UNIT
f_{SCL}	Serial clock frequency		100		400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	SCL = 100 KHz	4			µs
		SCL = 400 KHz	600			ns
t_{LOW}	LOW period of the SCL clock	SCL = 100 KHz	4.7			µs
		SCL = 400 KHz	1.3			
t_{HIGH}	HIGH period of the SCL clock	SCL = 100 KHz	4			µs
		SCL = 400 KHz	600			ns
$t_{SU;STA}$	Set-up time for a repeated START condition	SCL = 100 KHz	4.7			µs
		SCL = 400 KHz	600			ns
$t_{HD;DAT}$	Data hold time	SCL = 100 KHz	0		3.45	µs
		SCL = 400 KHz	0		900	ns
$t_{SU;DAT}$	Data set-up time	SCL = 100 KHz	250			ns
		SCL = 400 KHz	100			
t_r	Rise time of both SDA and SCL signals	SCL = 100 KHz			1000	ns
		SCL = 400 KHz			300	
t_f	Fall time of both SDA and SCL signals	SCL = 100 KHz			300	ns
		SCL = 400 KHz			300	
$t_{SU;STO}$	Set-up time for STOP condition	SCL = 100 KHz	4			µs
		SCL = 400 KHz	600			ns
t_{BUF}	Bus free time between stop and start condition	SCL = 100 KHz	4.7			µs
		SCL = 400 KHz	1.3			
t_{SP}	Pulse duratoin of spikes which mst be suppressed by the input filter	SCL = 100 KHz	NA		NA	
		SCL = 400 KHz	0		50	ns
C_b	Capacitive load for each bus line	SCL = 100 KHz			400	pF
		SCL = 400 KHz			400	

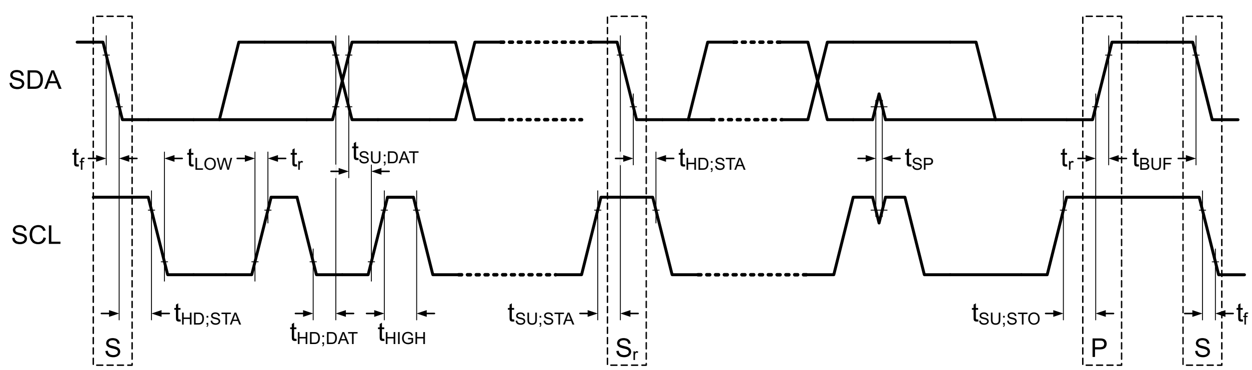


Figure 1. I²C Data Transmission Timing

8.7 Typical Characteristics

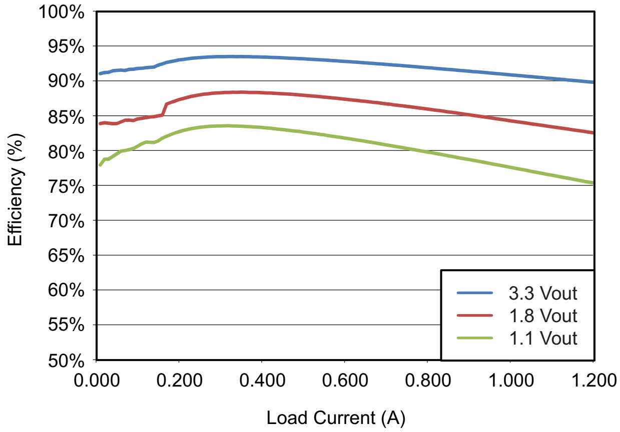


Figure 2. TPS65217 DC-DC Efficiency, 5 V in and an LQM2HPN2R2MG0L Inductor

9 Detailed Description

9.1 Overview

The TPS65217 device provides three step-down converters, two LDOs, two load switches, a linear battery charger, white LED driver, and power path. The system can be supplied by any combination of USB port, 5-V ac adaptor, or Li-ion battery. The device is characterized across a –40°C to 105°C temperature range, making it suitable for portable and non-portable 5-V industrial applications.

The I^2C interface provides comprehensive features for using the TPS65217 device. All rails, load switches, and LDOs can be enabled or disabled. Power-up and power-down sequences can also be programmed through the I^2C interface, as well as overtemperature and overcurrent thresholds. Charging and dimming parameters can also be monitored by the I^2C interface.

The three 2.25-MHz step-down converters can each supply up to 1.2 A of current. The default output voltages for each converter can be adjusted through the I^2C interface. All three converters feature dynamic voltage positioning to reduce the voltage undershoots and overshoots. Typically, the converters work at a fixed-frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents the converters automatically enter power save mode and operate in PFM (Pulse Frequency Modulation); however, for low-noise application the device can be forced into fixed-frequency PWM using the I^2C interface.

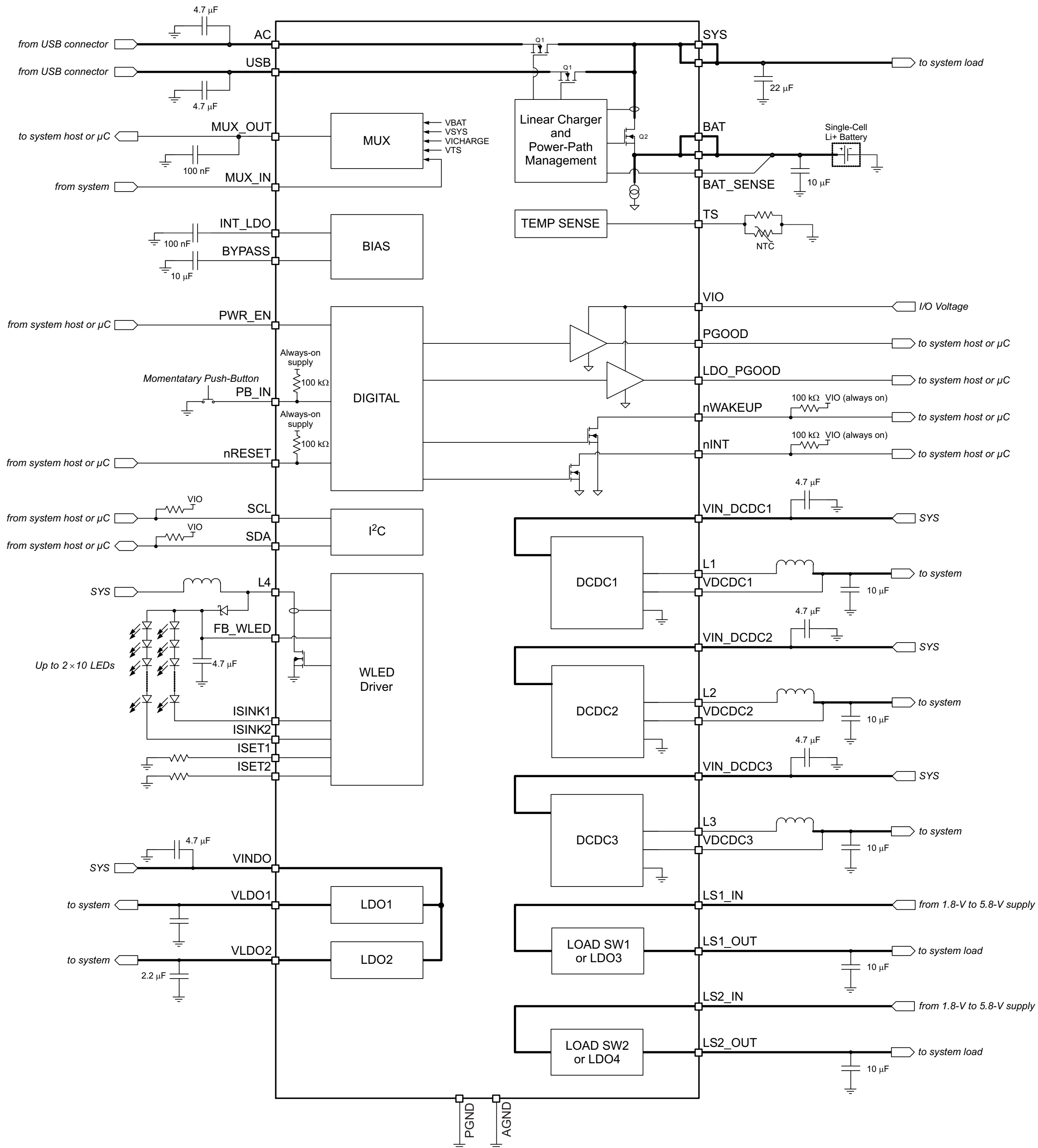
There are two traditional LDOs: LDO1 and LDO2. There are also two load switches, which can also be configured as LDOs: LDO3 and LDO4. LDO1 and LDO2 can support up to 100 mA each, but in SLEEP mode they are limited to 1 mA to reduce quiescent current. LDO3 and LDO4 can support up to 200 mA (TPS65217B), or 400 mA (TPS65217C and -D). LDO1 is always ON, but any rail can be configured to remain up in SLEEP state.

Two power-good logic signals are provided; the main power-good, which monitors DCDC1, DCDC2, DCDC3, LS1 or LDO3, and LS2 or LDO4; if the load switches are configured as LDOs. The main power-good signal can be configured to monitor LDO1 and LDO2. This signal is high in the ACTIVE state, but low in the SLEEP, RESET, and OFF states. The LDO_power-good monitors LDO1, and LDO2; the signal is high in the ACTIVE and SLEEP states, but low in RESET or OFF state. The signals are both pulled low when all the monitored rails are pulled low or when one or more of the monitored rails are enabled and have encountered a fault, typically output short or overcurrent condition.

The highly-efficient boost converter has two current sinks capable of driving two strings of up to 10 LEDs 25 mA each, or a single string of 20 LEDs at 50 mA. Brightness and dimming is supported by an internal PWM signal and I^2C control; both current sources are controlled together and cannot operate independently.

The triple system power path allows for simultaneous and independent charging from the linear battery charger for single-cell Li-ion and Li-Polymer batteries, and powering of the system. The AC input is prioritized over USB as the power source for charging the battery and powering the system. Both these sources are prioritized over the battery for powering the system to reduce the number of charge and discharge cycles on the battery.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Wake-Up and Power-Up Sequencing

The TPS65217 device has a pre-defined power-up–power-down sequence which in a typical application does not require changing. However, it is possible to define custom sequences under I^2C control. The power-up sequence is defined by strobes and delay times. Each output rail is assigned to a strobe to determine the order in which the rails are enabled and the delay times between strobes are selectable in a range from 1 ms to 10 ms.

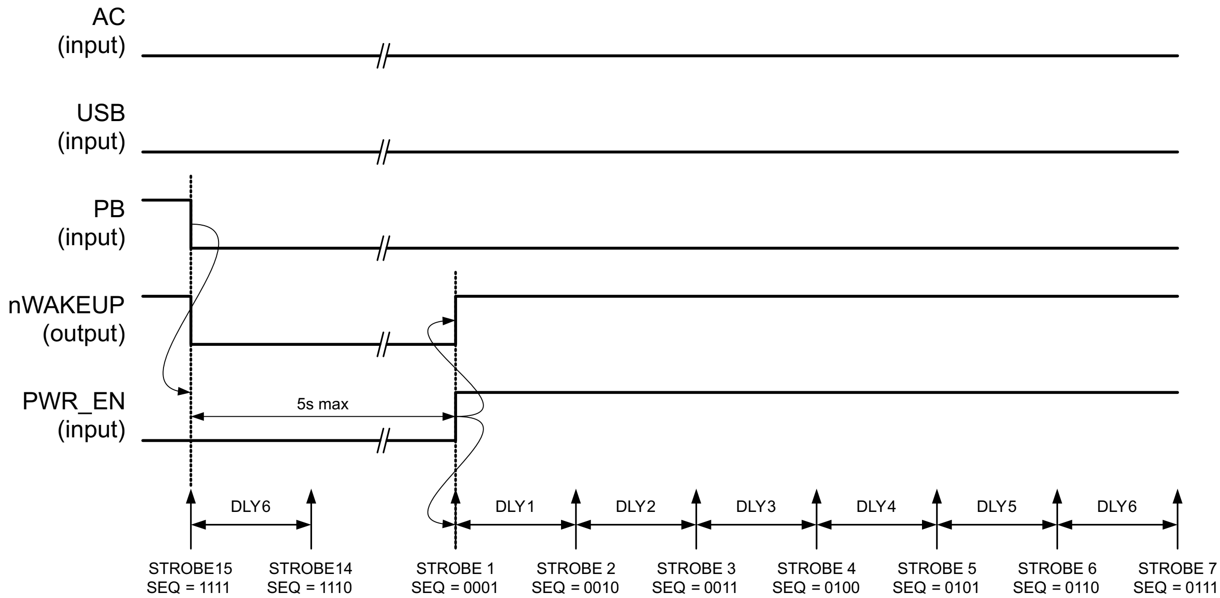
NOTE

Although the user can modify the power-up and power-down sequence through the SEQx registers, those registers are reset to default values when the device enters the SLEEP, OFF or RESET state. In practice this situation means that the power-up sequence is fixed and an other-than-default power-down sequence must be written every time the device is powered up.

Custom power-up and power-down down sequences can be checked out in the ACTIVE mode (PWR_EN pin high) by using the SEQUP and SEQDWN bits. To change the power-up default values, contact the factory.

9.3.1.1 Power-Up Sequencing

When the main power-up sequence is initiated, STROBE1 occurs and any rail assigned to this strobe is enabled. After a delay time of DLY1 STROBE2 occurs and the rail assigned to this strobe is powered up. The sequence continues until all strobes have occurred and all DLYx times have been executed.

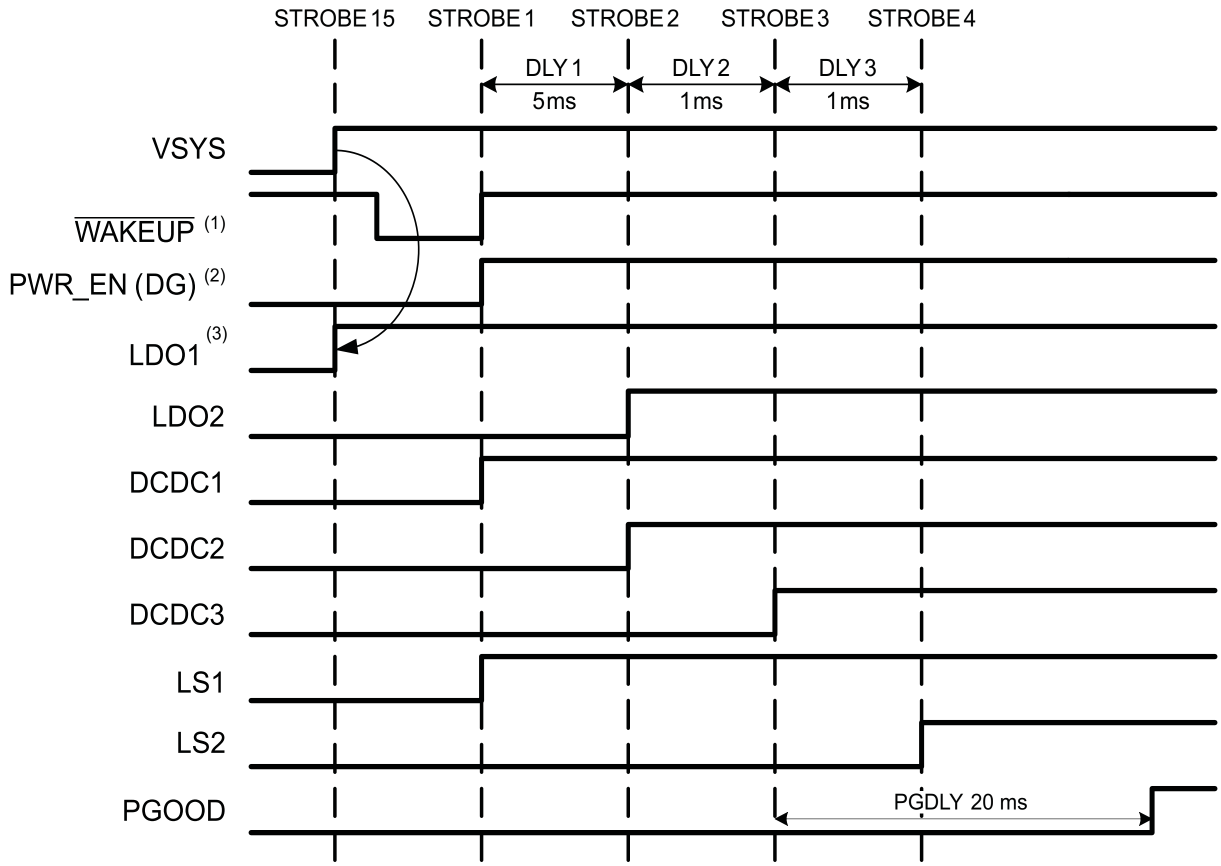


Power-up sequence is defined by strobes and delay times. In this example, push-button low is the power-up event.

Figure 3. Power-Up Sequence

The default power-up sequence can be changed by writing to the SEQ1-6 registers. Strobes are assigned to rails by writing to the SEQ1-4 registers. A rail can be assigned to only one strobe but multiple rails can be assigned to the same strobe. Delays between strobes are defined in registers SEQ5 and SEQ6.

Feature Description (continued)



See SLVU551 for default power-up sequences of the other TPS65217x family members.

Figure 4. Default Power-Up Sequence for the TPS65217A Device

The power up sequence is executed if one of the following events occurs:

From OFF State:

- Push-button is pressed (falling edge on PB_IN) OR
- USB voltage is asserted (rising edge on USB) OR
- AC adaptor is inserted (rising edge on AC) AND
- PWR_EN pin is asserted (pulled high) AND
- Device is not in undervoltage lockout (UVLO) or overtemperature shutdown (OTS).

The PWR_EN pin is level-sensitive (opposed to edge-sensitive), and it makes no difference if the pin is asserted before or after the above power-up events. However, the pin must be asserted within 5 seconds of the power-up event; otherwise, the power-down sequence is triggered and the device enters either OFF state.

From SLEEP State:

- Push-button is pressed (falling edge on PB_IN) OR
- USB voltage is asserted (rising edge on USB) OR
- AC adaptor is inserted (rising edge on AC) AND
- Device is not in undervoltage lockout (UVLO) or overtemperature shutdown (OTS) OR
- PWR_EN pin is asserted (pulled high).

In SLEEP state, the power-up sequence can be triggered by asserting the PWR_EN pin only and the push-button press or AC and USB assertion are not required.

Feature Description (continued)

From ACTIVE State:

The sequencer can be triggered any time by setting the SEQUP bit of the SEQ6 register high. The SEQUP bit is automatically cleared after the sequencer is done.

Rails that are not assigned to a strobe (SEQ = 0000b) are not affected by power-up and power-down sequencing and remain in their current ON or OFF state regardless of the sequencer. Any rail can be enabled or disabled at any time by setting the corresponding enable bit in the ENABLE register with the only exception that the ENABLE register cannot be accessed while the sequencer is active. Enable bits always reflect the current enable state of the rail, that is, the sequencer sets or resets the enable bits for the rails under its control. Also, whenever faults occur that shut-down the power-rails, the corresponding enable bits are reset.

9.3.1.2 Power-Down Sequencing

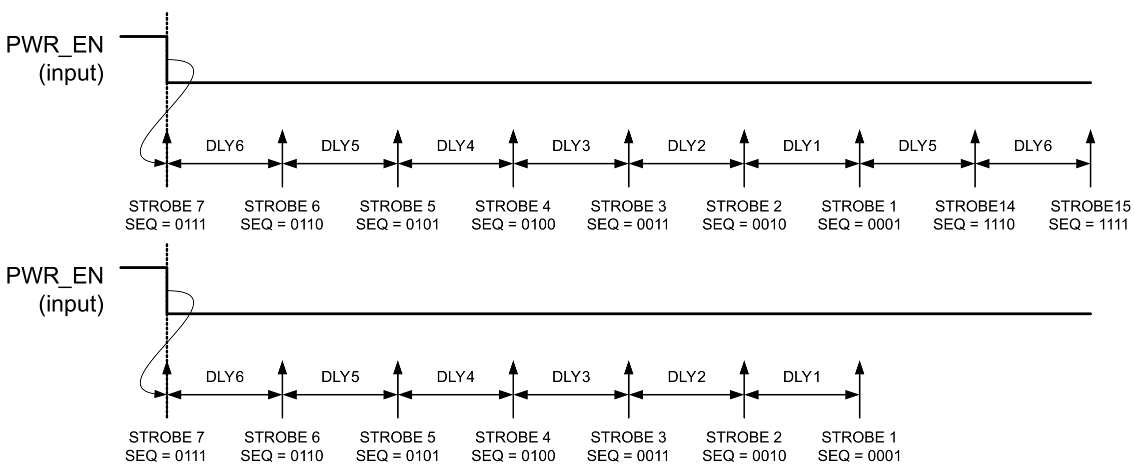
By default, power-down sequencing follows the reverse power-up sequence. When the power-down sequence is triggered, STROBE7 occurs first, and any rail assigned to STROBE7 is shut down. After a delay time of DLY6, STROBE6 occurs, and any rail assigned to STROBE6 is shut down. The sequence continues until all strobes have occurred and all DLYx times have been executed.

In some applications it is desired to shut down all rails simultaneously with no delay between rails. Set the INSTDWN bit in the SEQ6 register to bypass all delay times and shut-down all rails simultaneously when the power-down sequence is triggered.

A power-down sequence is executed if one of the following events occurs:

- The SEQDWN bit is set.
- The PWR_EN pin is pulled low.
- The push-button is pressed for > 8 s.
- The nRESET pin is pulled low.
- A fault occurs in the IC (OTS, UVLO, PGOOD failure).
- The PWR_EN pin is not asserted (pulled high) within 5 seconds of a power-up event and the OFF bit is set to 1.

When transitioning from ACTIVE to the OFF state, any rail not controlled by the sequencer is shut down after the power-down sequencer has finished. When transitioning from ACTIVE to the SLEEP state, any rail not controlled by the power-down sequencer maintains its state, which allows keeping the selected power rails up in the SLEEP state.



Power-down sequence follows reverse power-up sequence. TOP: Power-down sequence from ON state to OFF state (all rails are turned OFF). BOTTOM: Power-down sequence from ON state to SLEEP state. STROBE14 and STROBE15 are omitted to allow LDO1 or LDO2 to remain ON.

Figure 5. Power-Down Sequence

Feature Description (continued)

9.3.1.3 Special Strobes (STROBE 14 and 15)

STROBE 14 and STROBE 15 are not assigned to the main sequencer but used to control rails that are *always-on*, that is, are powered up as soon as the device exits the OFF state and remain ON in the SLEEP state. STROBE 14 and STROBE 15 options are available only for LDO1 and LDO2 and not for any of the other rails.

STROBE 15 occurs as soon as the push-button is pressed or the USB or ac adaptor is connected to the device. After a delay time of DLY6 STROBE 14 occurs. LDO1 and LDO2 can be assigned to either strobe and therefore can be powered up in any order (contact factory for details - default settings must be factory programmed since all registers are reset in SLEEP mode).

When a power-down sequence is initiated, STOBE 15 and STOBE 14 occur only if the OFF bit is set. Otherwise both strobes are omitted, and LDO1 and LDO2 maintain their state.

9.3.2 Power Good

Power-good is a signal used to indicate if an output rail is in regulation or at fault. Internally, all power-good signals of the enabled rails are monitored at all times and if any of the signals goes low, a fault is declared. All PGOOD signals are internally deglitched. When a fault occurs, all output rails are powered down and the device enters OFF state.

The TPS65217 device has two PGOOD outputs, one dedicated to LDO1 and 2 (LDO_PGOOD), and one programmable output (PGOOD). The following rules apply to both outputs:
- The power-up default state for PGOOD and LDO_PGOOD is low. When all rails are disabled, PGOOD and LDO_PGOOD outputs are both low.
- Only enabled rails are monitored. Disabled rails are ignored.
- Power-good monitoring of a particular rail starts 5 ms after the rail has been enabled. Power-good is continuously monitored thereafter, thus allowing the rail to power up.
- PGOOD and LDO_PGOOD outputs are delayed by the PGDLY (20 ms default) after the sequencer is done.
- If an enabled rail goes down due to a fault (output shorted, OTS, UVLO), PGOOD and/or LDO_PGOOD is declared low, and all rails are shut down.
- If the user disables a rail (either manually or through the sequencer), this action has no effect on the PGOOD or LDO_PGOOD pin.
- If the user disables all rails (either manually or through sequencer), PGOOD and/or LDO_PGOOD are pulled low.

9.3.2.1 LDO1, LDO2 PGOOD (LDO_PGOOD)

LDO_PGOOD is a push-pull output which is driven to a high level whenever LDO1 and/or LDO2 are enabled and in regulation. LDO_PGOOD is pulled low when both LDOs are disabled or at least one is enabled but has encountered a fault. A typical fault is an output short or overcurrent condition. In normal operation, LDO_PGOOD is high in the ACTIVE and SLEEP states and low in the RESET or OFF state.

9.3.2.2 Main PGOOD (PGOOD)

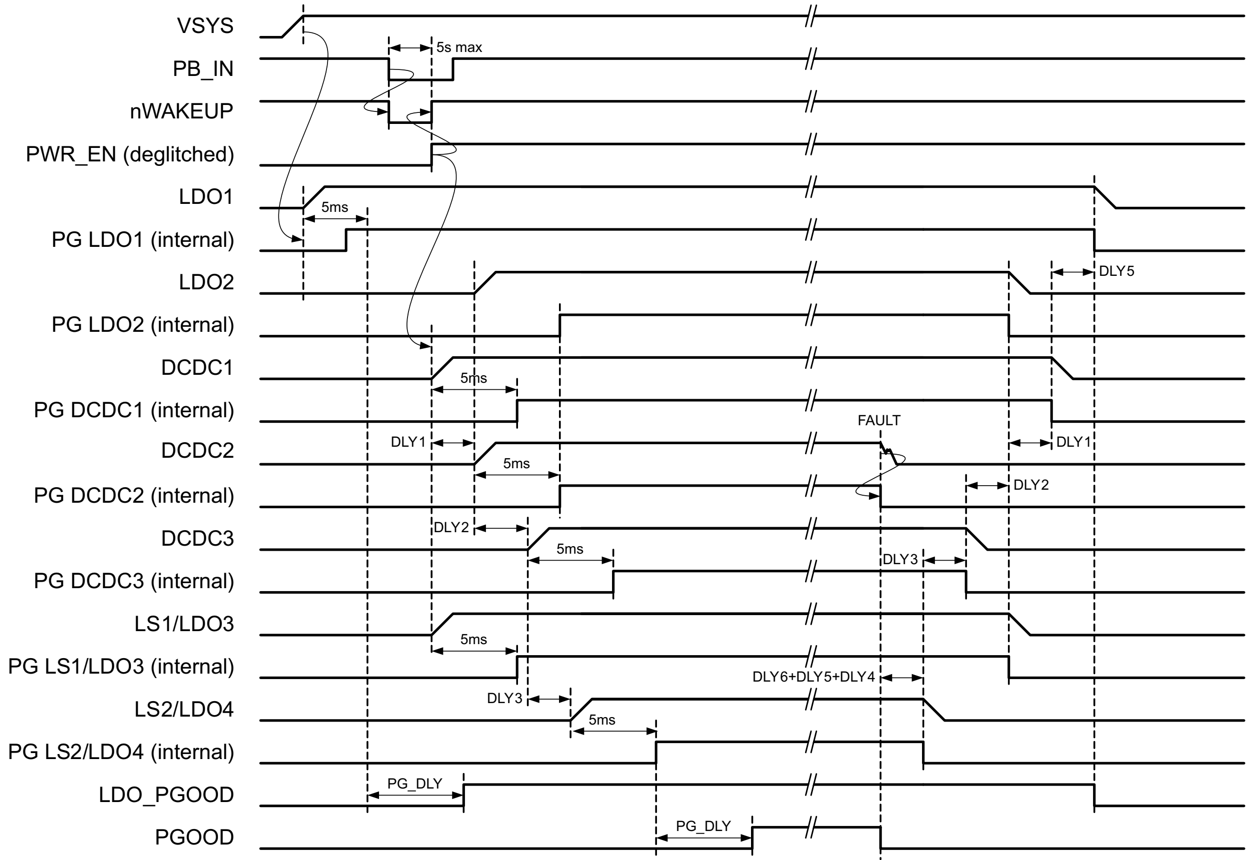
The main PGOOD pin has similar functionality to the LDO_PGOOD pin except that PGOOD monitors DCDC1, DCDC2, DCDC3, LS1 or LDO3, and LS2 or LDO4 if they are configured as LDOs. If LS1 or LDO3, and/or LS2 or LDO4 are configured as load switches, their respective PGOOD status is ignored. In addition, the user can choose to also monitor LDO1 and LDO2 by setting the LDO1PGM and LDO2PGM bits in the DEFPG register low. By default, LDO1 and LDO2 PGOOD status does not affect the PGOOD pin (mask bits are set to 1 by default). In normal operation PGOOD is high in the ACTIVE state but low in the SLEEP, RESET, or OFF state.

In SLEEP mode and WAIT PWR_EN state, PGOOD pin is forced low. PGOOD is pulled high after entering the ACTIVE mode, the power sequencer done, and the PGDLY expired. this function can be disabled by the factory.

9.3.2.3 Load Switch PGOOD

If either LS1 or LDO3, or LS2 or LDO4, is configured as a load switche, its respective PGOOD signal is ignored by the system. An overcurrent or short condition does not affect the PGOOD pin or any of the power rails unless the power dissipation leads to thermal shutdown.

Feature Description (continued)



Also shown is the power-down sequence for the case of a short on the DCDC2 output.

Figure 6. Default Power-Up Sequence

9.3.3 Push-Button Monitor (PB_IN)

The TPS65217 device has an active-low push-button input which is typically connected to a momentary switch to ground. The PB_IN input has a 50ms deglitch time and an internal pullup resistor to an always-on supply. The push button monitor is used to:

- Power-up the device from OFF or SLEEP mode upon detecting a falling edge on PB_IN.
- Power cycle the device when PB_IN is held low for > 8 s.

Both functions are described in the Modes of Operation section. A change in push-button status (PB_IN transitions high to low or low to high) is signaled to the host through the PBI interrupt bit in the INT register. The current status of the interrupt can be checked by reading the PB status bit in the STATUS register. A timing diagram for the push-button monitor is shown in Figure 7.

Feature Description (continued)

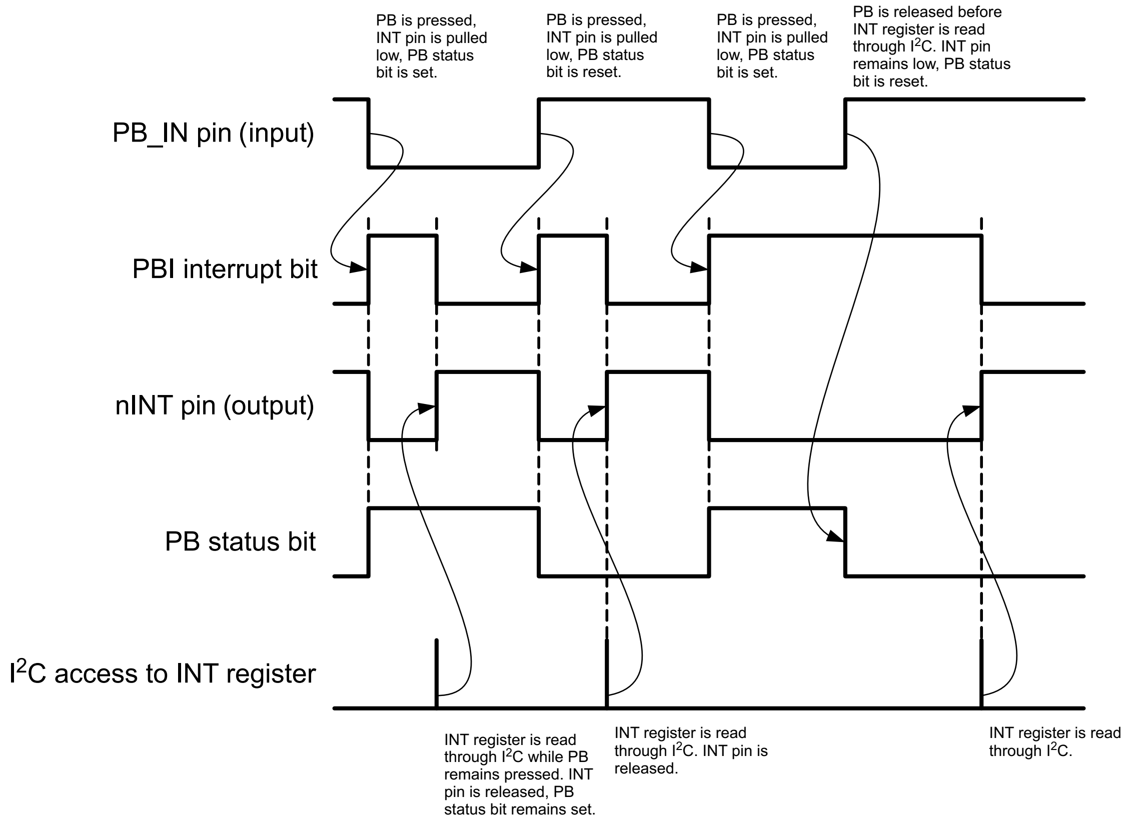


Figure 7. Timing Diagram of the Push-Button Monitor Circuit

9.3.4 nWAKEUP Pin (nWAKEUP)

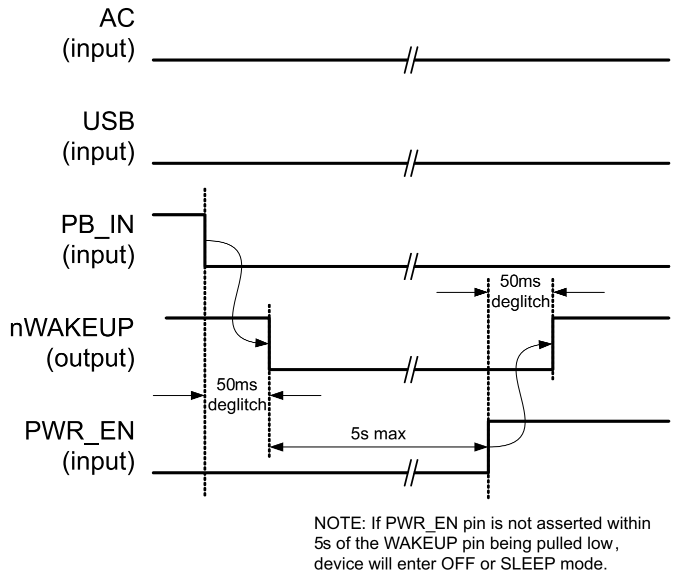
The nWAKEUP pin is an open drain, active-low output that is used to signal a wakeup event to the system host. This pin is pulled low whenever the device is in OFF or SLEEP state and detects a wakeup event as described in the Modes of Operation section. The nWAKEUP pin is delayed 50 ms over the power-up event and remains low for 50 ms after the PWR_EN pin has been asserted. If the PWR_EN pin is not asserted within 5 seconds of the power-up event, the device shuts down and enters the OFF state. In the ACTIVE mode, the nWAKEUP pin is always high. The timing diagram for the nWAKEUP pin is shown in Figure 8.

9.3.5 Power Enable Pin (PWR_EN)

The PWR_EN pin is used to keep the unit in the ACTIVE mode after it has detected a wakeup event as described in the Modes of Operation section. If the PWR_EN pin is not asserted within 5 seconds of the nWAKEUP pin being pulled low, the device shuts down the power and enter either the OFF or SLEEP mode, depending on the OFF bit in the STATUS register. The PWR_EN pin is level-sensitive, meaning that PWR_EN may be pulled high before the wake-up event.

The PWR_EN pin may also be used to toggle between the ACTIVE and SLEEP modes. See *SLEEP* in Modes of Operation for more information.

Feature Description (continued)



In the example shown, the wakeup event is a falling edge on the PB_IN.

Figure 8. nWAKEUP Timing Diagram

9.3.6 Reset Pin (nRESET)

When the nRESET pin is pulled low, all power rails including LDO1 and LDO2 are powered down, and default register settings are restored. The device remains powered down as long as the nRESET pin is held low, but for a minimum of 1 second. After the nRESET pin is pulled high the device enters ACTIVE mode, and the default power-up sequence executes. See *RESET* in Modes of Operation for more information.

9.3.7 Interrupt Pin (nINT)

The interrupt pin is used to signal any event or fault condition to the host processor. Whenever a fault or event occurs in the IC, the corresponding interrupt bit is set in the INT register, and the open-drain output is pulled low. The nINT pin is released (returns to Hi-Z state) and fault bits are cleared when the INT register is read by the host. However, if a failure persists, the corresponding INT bit remains set and the nINT pin is pulled low again after a maximum of 32 µs.

Interrupt events include push-button pressed or released, and USB and AC voltage status change.

The MASK bits in the INT register are used to mask events from generating interrupts. The MASK settings affect the nINT pin only and have no impact on protection and monitor circuits themselves. Note that persisting event conditions such as ISINK enabled shutdown can cause the nINT pin to be pulled low for an extended period of time, which can keep the host in a loop trying to resolve the interrupt. If this behavior is not desired, set the corresponding mask bit after receiving the interrupt and keep polling the INT register to see when the event condition has disappeared. Then unmask the interrupt bit again.

9.3.8 Analog Multiplexer

The TPS65217 device provides an analog multiplexer that allows access to critical system voltages such as:

- Battery voltage (VBAT)
- System voltage (VSYS)
- Temperature-sense voltage (VTS), and
- VICHARGE, a voltage proportional to the charging current.

In addition, one external input is available to monitor an additional system voltage. VBAT and VSYS are divided down by a factor of 1:3 to be compatible with the input-voltage range of the ADC that resides on the system host side. The output of the MUX is buffered and can drive a maximum of 1-mA load current.

Feature Description (continued)

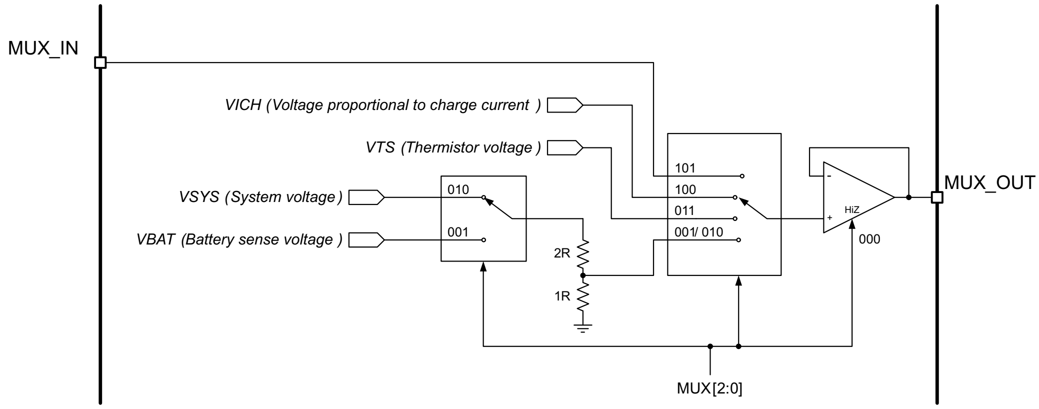


Figure 9. Analog Multiplexer

9.3.9 Battery Charger and Power Path

The TPS65217 device provides a linear charger for Li+ batteries and a triple system-power path targeted at space-limited portable applications. The power path allows simultaneous and independent charging of the battery and powering of the system. This feature enables the system to run with a defective or absent battery pack and allows instant system turn-on even with a totally discharged battery. The input power source for charging the battery and running the system can be either an ac adapter or a USB port. The power path prioritizes the AC input over the USB input, and both over the battery input, to reduce the number of charge and discharge cycles on the battery. Charging current is automatically reduced when system load increases and the system load exceeds the maximum current of the USB or ac adapter supply. In this case the battery supplements, meaning that the battery is discharged to supply the remaining current. A block diagram of the power path is shown in Figure 10, and an example of the power path management function is shown in Figure 11.

Feature Description (continued)

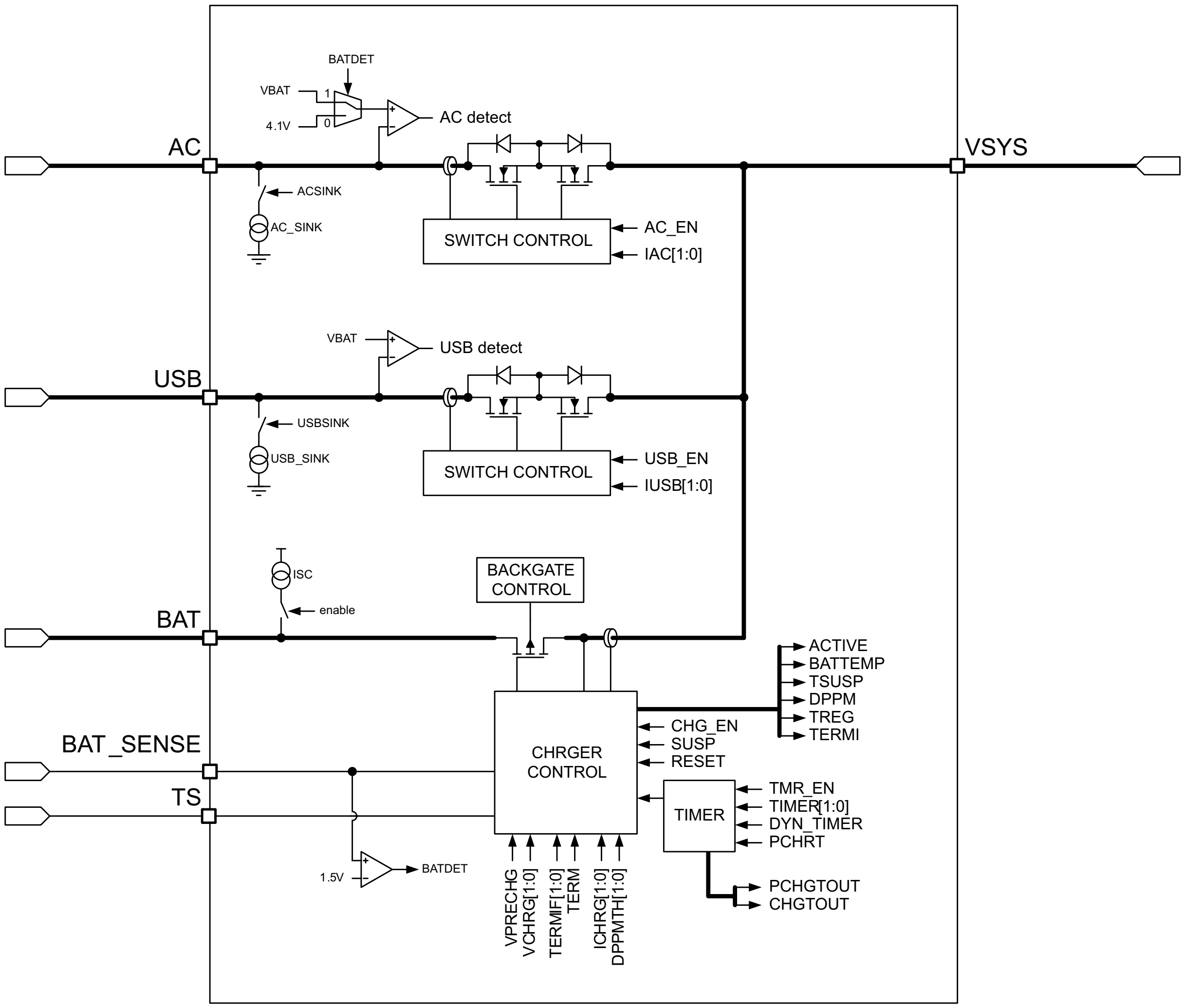
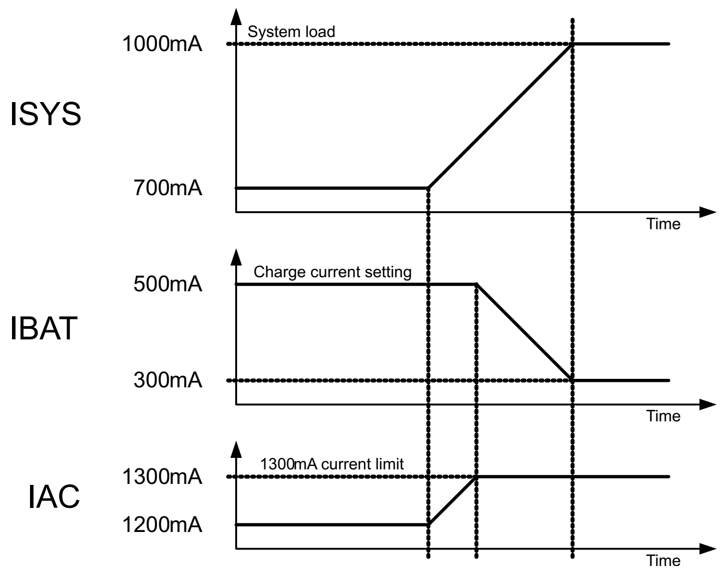


Figure 10. Block Diagram of the Power Path and Battery Charger

Feature Description (continued)



In this example, the AC input current limit is set to 1300 mA, battery charge current is 500 mA, and system load is 700 mA. As the system load increases to 1000 mA, battery charging current is reduced to 300 mA to maintain the AC input current of 1300 mA.

Figure 11. Power Path Management

Detection thresholds for AC and USB inputs are a function of the battery voltage, and three basic use cases must be considered:

9.3.9.1 Shorted or Absent Battery (V_{BAT} < 1.5 V)

The AC or USB inputs are valid and the chip powers up if V_{AC} or V_{USB} rises above 4.3 V. After powering up, the input voltage can drop to the V_{UVLO} + V_{OFFSET} level (for example, 3.3 V + 200 mV) before the chip powers down.

The AC input is prioritized over the USB input; that is, if both inputs are valid, current is pulled from the AC input and not USB. If both AC and USB supplies are available, the power-path switches to the USB input if V_{AC} drops below 4.1 V (fixed threshold).

Note that the rise time of V_{AC} and V_{USB} must be less than 50 ms for the detection circuits to operate properly. If the rise time is longer than 50 ms, the IC may fail to power up.

The linear charger periodically applies a 10-mA current source to the BAT pin to check for the presence of a battery. This current application causes the BAT terminal to float up to > 3 V, which may interfere with AC removal detection and the ability to switch from the AC to the USB input. For this reason, it is not recommended to use both the AC and USB inputs when the battery is absent.

9.3.9.2 Dead Battery (1.5 V < V_{BAT} < V_{UVLO})

Functionality is the same as for the shorted battery case. The only difference is that after AC is selected as the input and the power-path does not switch back to USB as V_{AC} falls below 4.1 V.

9.3.9.3 Good Battery (V_{BAT} > V_{UVLO})

The AC and USB supplies are detected when the input is 190 mV above the battery voltage, and are considered absent when the voltage difference to the battery is less than 125 mV. This feature ensures that the AC and USB supplies are used whenever possible to save battery life. The USB and AC inputs are both current-limited and controlled through the PPATH register.

In case AC or USB is not present or is blocked by the power path control logic (for example, in the OFF state), the battery voltage always supplies the system (SYS pin).

Feature Description (continued)

9.3.9.4 AC and USB Input Discharge

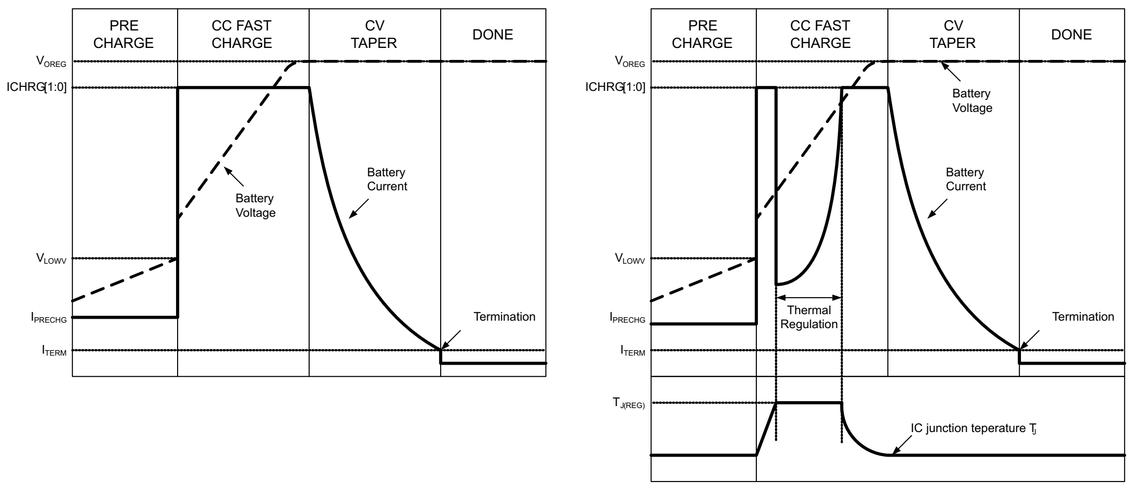
The AC and USB inputs have 90-µA internal current sinks which are used to discharge the input pins to avoid false detection of an input source. The AC sink is enabled when USB is a valid supply and V_{AC} is below the detection threshold. Likewise, the USB sink is enabled when AC is a valid supply and V_{USB} is below the detection limit. Both current sinks can be forced OFF by setting the [ACSINK, USBSINK] bits to 11b. Both bits are located in register 0x01 (PPATH).

NOTE

[ACSINK, USBSINK] = 01b and 10b combinations are not recommended as these may lead to unexpected enabling and disabling of the current sinks.

9.3.10 Battery Charging

When the charger is enabled (CH_EN bit set to 1), it first checks for a short circuit on the BAT pin by sourcing a small current and monitoring the BAT voltage. If the voltage on the BAT pin rises above $V_{BAT(SC)}$, a battery is present and charging can begin. The battery is charged in three phases: precharge, constant-current fast charge (current regulation), and a constant-voltage charge (voltage regulation). In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if an internal temperature threshold is exceeded. Figure 12 shows a typical charging profile.



LEFT: Typical charge current profile with termination enabled.
RIGHT: Modified charging profile with thermal regulation loop active and termination enabled.

Figure 12. Charging Profiles

In the precharge phase, the battery is charged at a current of IPRECHG, which is typically 10% of the fast-charge current rate. The battery voltage starts rising. After the battery voltage crosses the V_{LOWV} threshold, the battery is charged at a current of I_{CHG}. The battery voltage continues to rise. When the battery voltage reaches V_{OREG}, the battery is held at a constant value of V_{OREG}. The battery current now decreases as the battery approaches full charge. When the battery current reaches I_{TERM}, the TERMI flag in register CHGCONFIG0 is set to 1. To avoid false termination when the DPPM or thermal loop kicks in, termination is disabled when either loop is active.

The charge current cannot exceed the input current limit of the power path minus the load current on the SYS pin, because the power-path manager reduces the charge current to support the system load if the input current limit is exceeded. Whenever the nominal charge current is reduced by action of the power path manger, the DPPM loop, or the thermal loop, the safety timer is clocked with half the nominal frequency to extend the charging time by a factor of 2.

Feature Description (continued)

9.3.11 Precharge

The precharge current is preset to a factor of 10% of the fast-charge current ICHRG[1:0] and cannot be changed by the user.

9.3.12 Charge Termination

When the charging current drops below the termination current threshold, the charger is turned off. The value of the termination current threshold can be set in register CHGCONFIG3 using bits TERMIF[1:0]. The termination current has a default setting of 7.5% of the ICHRG[1:0] setting.

Charge termination is enabled by default and can be disabled by setting the TERM bit of the CHGCONFIG1 register to 1. When termination is disabled, the device goes through the precharge, fast-charge and CV phases, then remains in the CV phase. The charger behaves like an LDO with an output voltage equal to V_{OREG}, able to source current up to I_{CHG} or I_{IN-MAX}, whichever is less. Battery detection is not performed.

NOTE

Termination current threshold is not a tightly controlled parameter. Using the lowest setting (2.5% of nominal charge current) is not recommended because the minimum termination current can be very close to 0. Any leakage on the battery side may cause the termination not to trigger and charging to time out eventually.

9.3.13 Battery Detection and Recharge

Whenever the battery voltage falls below V_{RCH}, $I_{BAT(DET)}$ is pulled from the battery for a duration t_{DET} to determine if the battery has been removed. The voltage on the BAT pin remaining above V_{LOWV} indicates that the battery is still connected. If the charger is enabled (CH_EN = 1), a new battery charging cycle begins.

The BAT pin voltage faling below V_{LOWV} in the battery detection test indicates that the battery has been removed. The device then checks for battery insertion: it turns on the charging path and sources I_{PRECHG} out of the BAT pin for duration t_{DET}. Failure of the voltage to rise above V_{RCH} indicates that a battery has been inserted, and a new charge cycle can begin. If, however, the voltage does rise above V_{RCH}, it is possible that a fully charged battery has been inserted. To check for this, $I_{BAT(DET)}$ is pulled from the battery for t_{DET} and if the voltage falls below V_{LOWV}, no battery is present. The battery detection cycle continues until the device detects a battery or the charger is disabled.

When the battery is removed from the system, the charger also flags a BATTEMP error, indicating that the TS input is not connected to a thermistor.

9.3.14 Safety Timer

The TPS65217 device hosts an internal safety timer for the precharge and fast-charge phases to prevent potential damage to either the battery or the system. The default fast-charge time can be changed in register CHGCONFIG1 and the precharge time in CHGCONFIG3. The timer functions can be disabled by resetting the TMR_EN bit of the CHGCONFIG1 register to 0. Note that both timers are disabled when charge termination is disabled (TERM = 0).

9.3.14.1 Dynamic Timer Function

Under some circumstances, the charger current is reduced to react to changes in the system load or junction temperature. The two events that can reduce the charging current are:

- The system load current increases, and the DPPM loop reduces the available charging current.
- The device has entered thermal regulation because the IC junction temperature has exceeded $T_{J(REG)}$.

In each of these events, the timer is clocked with half-frequency to extend the charger time by a factor of 2, and charger termination is disabled. Normal operation resumes after the IC junction temperature has cooled off and/or the system load drops to a level where enough current is available to charge the battery at the desired charge rate. This feature is enabled by default and can be disabled by resetting the DYNTMR bit in the CHGCONFIG2 register to 0. A modified charge cycle with the thermal loop active is shown in Figure 12.

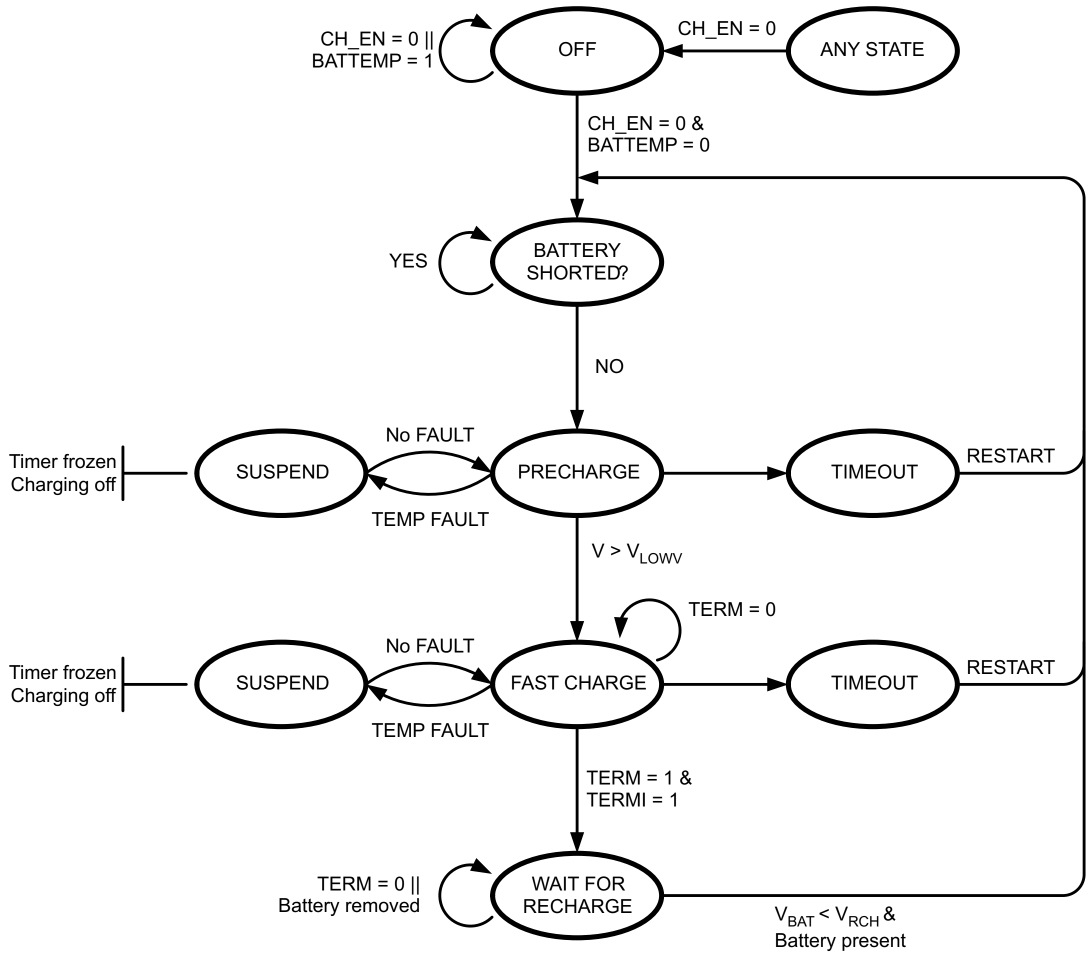
Feature Description (continued)

9.3.14.2 Timer Fault

A timer fault occurs if:

- If the battery voltage does not exceed V_{LOWV} in time t_{PRECHG} during pre-charging.
- If the battery current does not reach I_{TERM} in fast charge before the safety timer expires. Fast-charge time is measured from the beginning of the fast-charge cycle.

The fault status is indicated by the CHTOUT and PCHTOUT bits in the CHGCONFIG0 register. Time-out faults are cleared and a new charge cycle is started when either the USB or AC supply is connected (rising edge of V_{USB} or V_{AC}), the charger RESET bit is set to 1 in the CHGCONFIG1 register, or the battery voltage drops below the recharge threshold V_{RCH}.



NOTES:
TEMP FAULT = Battery HOT || Battery cold || Thermal shutdown
RESTART = V_{USB} (↑) || V_{AC} (↑) || Charger RESET bit (↑) || $V_{BAT} < V_{RCH}$

Figure 13. State Diagram of Battery Charger

9.3.15 Battery-Pack Temperature Monitoring

The TS pin of the TPS65217 device connects to the NTC resistor in the battery pack. During charging, if the resistance of the NTC indicates that the battery is operating outside the limits of safe operation, charging is suspended and the safety timer value is frozen. When the battery pack temperature returns to a safe value, charging resumes with the current timer setting.

Feature Description (continued)

By default, the device is set up to support a 10 kΩ NTC with a B-value of 3480. The NTC is biased through a 7.35-kΩ internal resistor connected to the BYPASS rail (2.25 V) and requires an external 75-kΩ resistor parallel to the NTC to linearize the temperature response curve.

The TPS65217 device supports two different temperature ranges for charging, 0°C to 45°C and 0°C to 60°C, which can be selected through the TRANGE bit in register CHCONFIG3.

NOTE

The device can be configured to support a 100-kΩ NTC (B = 3960) by setting the the NTC_TYPE bit in register CHGCONFIG1 to 1. However, it is not recommended to do so. In sleep mode, the charger continues charging the battery, but all register values are reset to default values. Therefore, the charger would get the wrong temperature information. If a 100-kΩ NTC setting is required, please contact the factory.

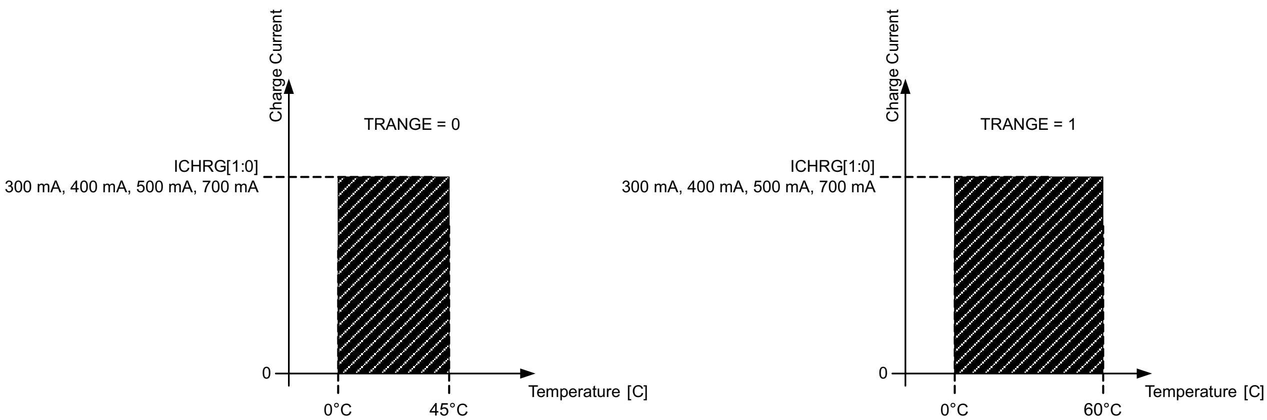


Figure 14. Charge Current as a Function of Battery Temperature

Feature Description (continued)

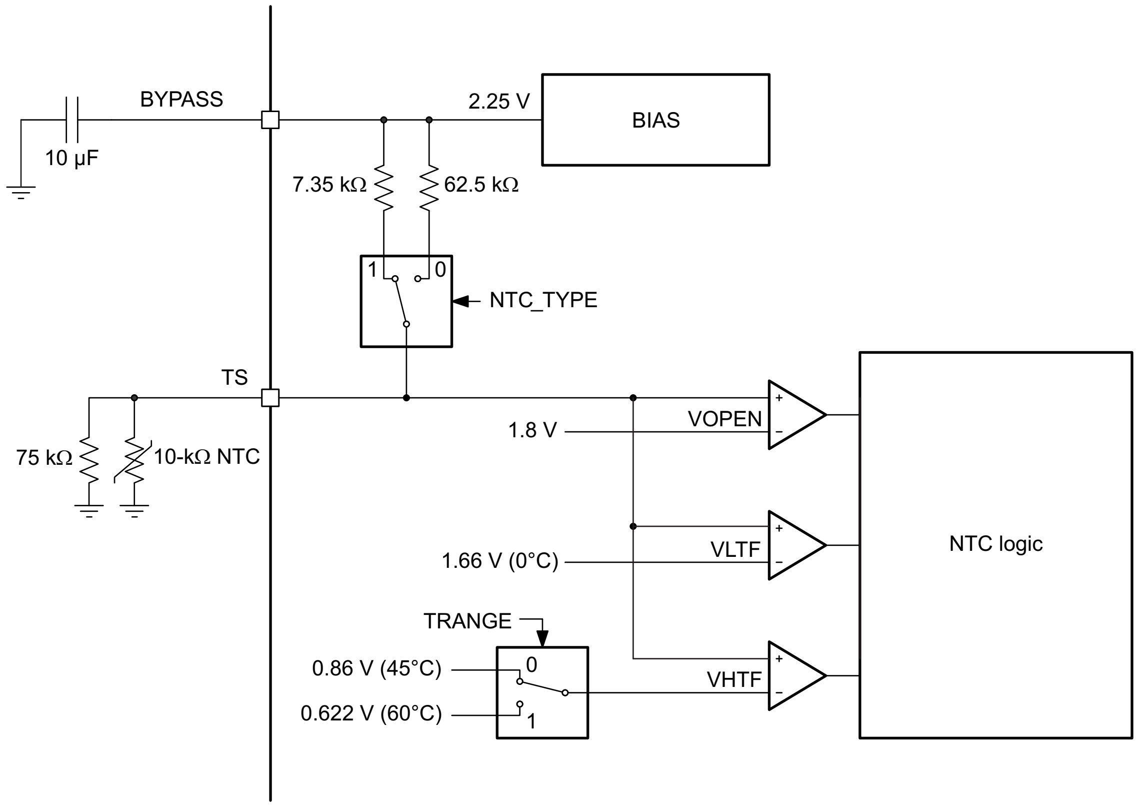


Figure 15. NTC Bias Circuit

9.3.16 DC-DC Converters

9.3.16.1 Operation

The TPS65217 step-down converters typically operate with 2.25-MHz fixed-frequency pulse-width modulation (PWM) at moderate to heavy load currents. At light load currents, the converter automatically enters power-save mode and operates in pulse-frequency modulation (PFM).

During PWM operation, the converter uses a unique fast-response voltage-mode controller scheme with input-voltage feed-forward to achieve good line and load regulation, allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle, the high-side MOSFET is turned on. The current flows from the input capacitor via the high-side MOSFET through the inductor to the output capacitor and load. During this phase, the current ramps up until the PWM comparator trips and the control logic turns off the switch. The current-limit comparator also turns off the switch in case the current limit of the high-side MOSFET switch is exceeded. After a dead time to prevent shoot-through current, the low-side MOSFET rectifier is turned on and the inductor current ramps down. The current flows now from the inductor to the output capacitor and to the load. The current returns back to the inductor through the low-side MOSFET rectifier.

The next cycle turns off the low-side MOSFET rectifier and turns on the on the high-side MOSFET.

The dc-dc converters operate synchronized to each other, with converter 1 as the master. A 120° phase shift between DCDC1 and DCDC2, and between DCDC2 and DCDC3, decreases the combined input rms current at the VIN_DCDCx pins. Therefore, smaller input capacitors can be used.

9.3.16.2 Output Voltage Setting

The output voltage of the dc-dc converters can be set in two different ways:

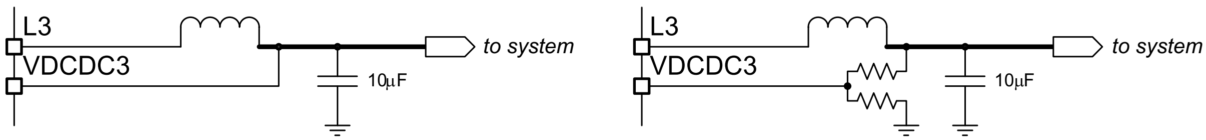
- As a fixed-voltage converter where the voltage is defined in register DEFDCDCx.
- As an external resistor network. Set the XADJx bit in the DEFDCDCx register and calculate the output voltage

Feature Description (continued)

with the following formula:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

Where V_{REF} is the feedback voltage of 0.6 V. It is recommended to set the total resistance of R1 + R2 to less than 1 MΩ. Shield the VDCDC1, VDCDC2, and VDCDC3 lines from switching nodes and from inductor L1, L2, and L3 to prevent coupling of noise into the feedback pins.



DCDC1, DCDC2, and DCDC3 offer two methods to adjust the output voltage.
LEFT: Fixed-voltage options programmable through I^2C (XADJ3 = 0, default).
RIGHT: Voltage is set by external feedback resistor network (XADJ3 = 1).

Figure 16. Example for DCDC3

9.3.16.3 Power-Save Mode and Pulse-Frequency Modulation (PFM)

By default, all three dc-dc converters enter pulse-frequency modulation (PFM) mode at light loads, and fixed-frequency pulse-width modulation (PWM) mode at heavy loads. In some applications, it is desirable to force PWM operation even at light loads, which can be accomplished by setting the PFM_ENx bits in the DEFSLEW registers to 1 (default setting is 0). In PFM mode, the converter skips switching cycles and operates with reduced frequency with a minimum quiescent current to maintain high efficiency. The converter positions the output voltage typically 1% above the nominal output voltage. This voltage-positioning feature minimizes the voltage drop caused by a sudden load step.

The transition from PWM to PFM mode occurs after the inductor current in the low-side MOSFET switch becomes 0.

During the power save mode, the output voltage is monitored with a PFM comparator. As the output voltage falls below the PFM comparator threshold of V_{OUT} – 1%, the device starts a PFM current pulse. For this, the high-side MOSFET turns on and the inductor current ramps up. Then the high-side MOSFET turns off and the low-side MOSFET switch turns on until the inductor current becomes 0 again.

The converter effectively delivers a current to the output capacitor and the load. If the load is below the delivered current, the output voltage rises. If the output voltage is equal to or higher than the PFM comparator threshold, the device stops switching and enters a sleep mode with a typical 15-µA current consumption. In case the output voltage is still below the PFM comparator threshold, further PFM current pulses are generated until the PFM comparator threshold is reached. The converter starts switching again after the output voltage drops below the PFM comparator threshold.

With a single threshold comparator, the output-voltage ripple during PFM mode operation can be kept very small. The ripple voltage depends on the PFM comparator delay, the size of the output capacitor, and the inductor value. Increasing output capacitor values and/or inductor values minimizes the output ripple.

The PFM mode is left and PWM mode entered in case the output current can no longer be supported in PFM mode or if the output voltage falls below a second threshold, called PFM comparator-low threshold. This PFM comparator-low threshold is set to 1% below nominal V_{OUT} and enables a fast transition from power-save mode to PWM mode during a load step.

The power-save mode can be disabled through the I^2C interface for each of the step-down converters, independently of each other. If the power-save mode is disabled, the converter then operates in fixed-PWM mode.

Feature Description (continued)

9.3.16.4 Dynamic Voltage Positioning

This feature reduces the voltage undershoots and overshoots at load steps from light to heavy load and vice versa. This is active in power-save mode and provides more headroom for both the voltage drop at a load step and the voltage increase at a load throw-off. This improves load-transient behavior. At light loads, in which the converter operates in PFM mode, the output voltage is regulated typically 1% higher than the nominal value. In case of a load transient from light load to heavy load, the output voltage drops until it reaches the low threshold of the PFM comparator set to –1% below the nominal value, and enters PWM mode. During a load throw-off from heavy load to light load, the voltage overshoot is also minimized due to active regulation turning on the low-side MOSFET.

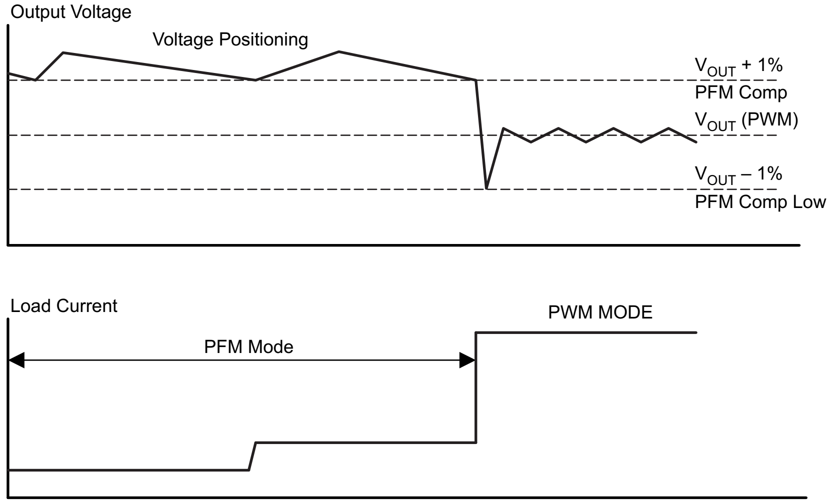


Figure 17. Dynamic Voltage Positioning in Power Save Mode

9.3.16.5 100% Duty-Cycle Low-Dropout Operation

The device starts to enter the 100% duty-cycle mode after the input voltage comes close to the nominal output voltage. In order to maintain the output voltage, the high-side MOSFET is turned on 100% for one or more cycles. As VIN decreases further, the high-side MOSFET is turned on completely. In this case, the converter offers a low input-to-output voltage difference. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range.

The minimum input voltage to maintain regulation depends on the load current and output voltage, and can be calculated as:

$$V_{IN,MIN} = V_{OUT,MAX} + I_{OUT,MAX} \times \left(R_{DSON,MAX} + R_L\right)$$

where
- $I_{OUT,MAX}$ = Maximum output current plus inductor ripple current
- $R_{DSON,MAX}$ = Maximum upper MOSFET switch R_{DSON}
- R_L = DC resistance of the inductor
- $V_{OUT,MAX}$ = Nominal output voltage plus maximum output voltage tolerance (2)

9.3.16.6 Short-Circuit Protection

High-side and low-side MOSFET switches are short-circuit protected. After the high-side MOSFET switch reaches its current limit, it is turned off and the low-side MOSFET switch is turned ON. The high-side MOSFET switch can only turn on again after the current in the low-side MOSFET switch decreases below its current limit.

Feature Description (continued)

9.3.16.7 Soft Start

The three step-down converters in the TPS65217 device have an internal soft-start circuit that controls the ramp-up of the output voltage. The output voltage ramps up from 5% to 95% of its nominal value within 750 µs. This limits the inrush current in the converter during start-up and prevents possible input voltage drops when a battery or high-impedance power source is used. The soft-start circuit is enabled after the start-up time t_{Start} has expired.

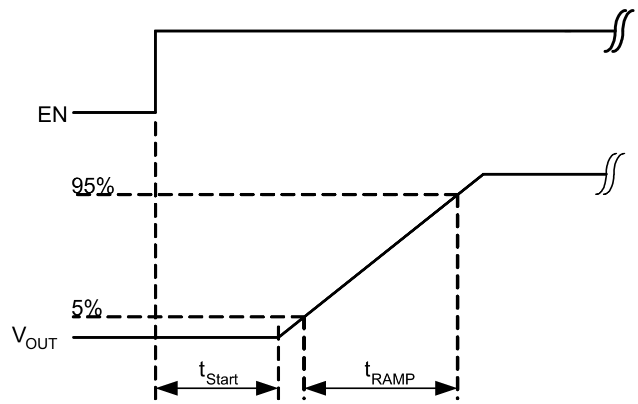


Figure 18. Output of the DC-DC Converters is Ramped Up Within 750 µs

9.3.17 Standby LDOs (LDO1, LDO2)

LDO1 and LDO2 support up to 100 mA each, are internally current limited, and have a maximum dropout voltage of 200 mV at rated output current. In SLEEP mode, however, output current is limited to 1 mA each. When disabled, both outputs are discharged to ground through a 430-Ω resistor.

LDO1 supports an output voltage range of 1 V to 1.8 V, which is controlled through the DEFLDO1 register. LDO2 supports an output voltage range from 0.9 V to 1.5 V, and is controlled through the DEFLDO2 register. By default, LDO1 is enabled immediately after a power-up event as described in the *Modes of Operation* section and remains ON in SLEEP mode to support system standby. Each LDO has low standby current of < 15 µA, typical.

LDO2 can be configured to track the output voltage of DCDC3 (core voltage). When the TRACK bit is set in the DEFLDO2 register, the output is determined by the DCDC3[5:0] bits of the DEFDCDC3 register and the LDO2[5:0] bits of the DEFLDO2 register are ignored.

LDO1 and LDO2 can be controlled through STROBE 1–6, special STROBES 14 and 15, or through the corresponding enable bits in the ENABLE register. By default, LDO1 and LDO2 are controlled through STROBE15, which keeps it alive in SLEEP mode. The STROBE assignments can be changed by the user while in ACTIVE mode, but be aware that all register settings are reset to default values in SLEEP or OFF mode. This can cause the LDO to power up automatically when leaving SLEEP mode, even though they have been disabled in SLEEP mode previously by assigning them to a different strobe or resetting the corresponding enable bit. If this is not desired, new default values must be programmed into non-volatile memory by the factory. Contact TI for details.

9.3.18 Load Switches or LDOs (LS1 or LDO3, LS2 or LDO4)

The TPS65217 device provides two general-purpose load switches that can also be configured as LDOs. As LDOs, they support up to 200 mA each, are internally current-limited, and have a maximum dropout voltage of 200 mV at rated output current. LDO3 and LDO4 of the TPS65217C and TPS65217D devices support up to 400-mA of current. The ON-OFF state of the load switches of LDOs be controlled either through the sequencer or the LS1_EN and LS2_EN bits of the ENABLE register. When disabled, both outputs are discharged to ground through a 375-Ω resistor.

As load switches, LS1 and LS2 have a maximum impedance of 650 mΩ. Different from LDO operation, load switches can remain in current limit indefinitely without affecting the internal power-good signal or affecting the other rails. Note, however, that excessive power dissipation in the switches may cause thermal shutdown of the IC.

Feature Description (continued)

Load switch and LDO modes are controlled by the LS1LDO3 and LS2LDO4 bits of the DEFLS1 and DEFLS2 registers.

9.3.19 White LED Driver

The TPS65217 device contains a boost converter and two current sinks capable of driving up to 2 × 10 LEDs at 25 mA or a single string at 50 mA of current. The current per current sink is approximated by the following equation:

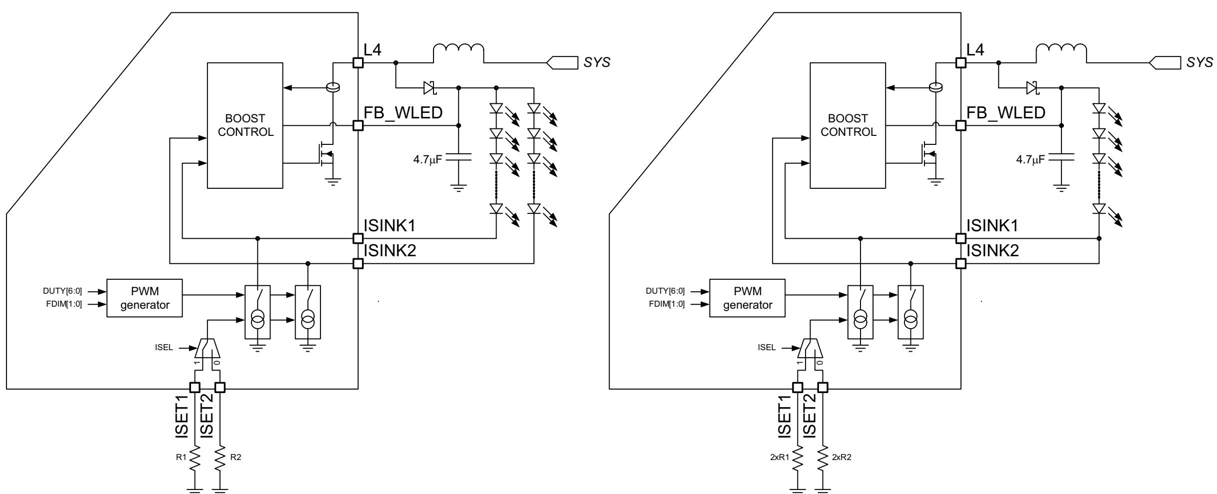
$$I_{LED} = 1048 \times \frac{1.24\ V}{R_{SET}} \quad (3)$$

Two different current levels can be programmed using two external R_{SET} resistors. Only one current setting is active at any given time, and both current sinks are always regulated to the same current. The active current setting is selected through the ISEL bit of the WLEDCTRL1 register.

Brightness dimming is supported by an internal PWM signal and I^2C control. Both current sources are controlled together and cannot operate independently. By default, the PWM frequency is set to 200 Hz, but can be changed to 100 Hz, 500 Hz, or 1000 Hz. The PWM duty cycle can be adjusted from 1% (default) to 100% in 1% steps through the WLEDCTRL2 register.

When the ISINK_EN bit of WLEDCTRL1 register is set to 1, both current sinks are enabled, and the boost output voltage at the FB_WLED pin is regulated to support the same I_{SINK} current through each current sink. The boost output voltage, however, is internally limited to 39 V.

If only a single WLED string is required, short the ISINK1 and ISINK2 pins together and connect them to the cathode of the diode string. Note that the LED current in this case is 2 × I_{SINK}. See Table 32 and Table 33 for recommended inductors and output capacitors for the WLED boost converters.



LEFT: Dual-string operation.
RIGHT: Single-string operation (same LED current as dual string). Note that for single-string operation, both ISINK pins are shorted together and the RSET values are doubled.

Figure 19. Block Diagram of WLED Driver

9.4 Device Functional Modes

9.4.1 Modes of Operation

OFF In OFF mode, the PMIC is completely shut down with the exception of a few circuits to monitor the AC, USB, and push-button inputs. All power rails are turned off and the registers are reset to their default values. The I^2C communication interface is turned off. This is the lowest-power mode of operation. To exit the OFF mode, one of the following wake-up events must occur:

- The push-button input is pulled low.
- The USB supply is connected (positive edge).
- The ac adapter is connected (positive edge).

To enter the OFF state, set the OFF bit in the STATUS register to 1, and then pull the PWR_EN pin low. Note that in normal operation, the OFF state can only be entered from the ACTIVE state. Whenever a fault occurs during operation, such as thermal shutdown, power-good fail, undervoltage lockout, or a PWR_EN pin timeout, all power rails are shut down and the device goes to the OFF state. The device remains in the OFF state until the fault has been removed and a new power-up event has occurred.

ACTIVE This is the typical mode of operation when the system is up and running. All dc-dc converters, LDOs, load switches, the WLED driver, and the battery charger are operational and can be controlled through the I^2C interface.

After a wake-up event, the PMIC enables all rails not controlled by the sequencer and pulls the nWAKEUP pin low to signal the event to the host processor. The device enters the ACTIVE state only if the host asserts the PWR_EN pin within 5 seconds after the wake-up event. Otherwise, the device enters the OFF state. In the ACTIVE state, the sequencer is triggered to bring up the remaining power rails. The nWAKEUP pin returns to the Hi-Z state after the PWR_EN pin has been asserted. A timing diagram is shown in Figure 3. The ACTIVE state can also be entered from the SLEEP state directly by pulling the PWR_EN pin high. See the SLEEP state description for details.

To exit ACTIVE mode the PWR_EN pin must be pulled low.

SLEEP The SLEEP state is a low-power mode of operation intended to support system standby. Typically, all power rails are turned off with the exception of LDO1, and the registers are reset to their default values. LDO1 remains operational but can support only a limited amount of current (1 mA typical).

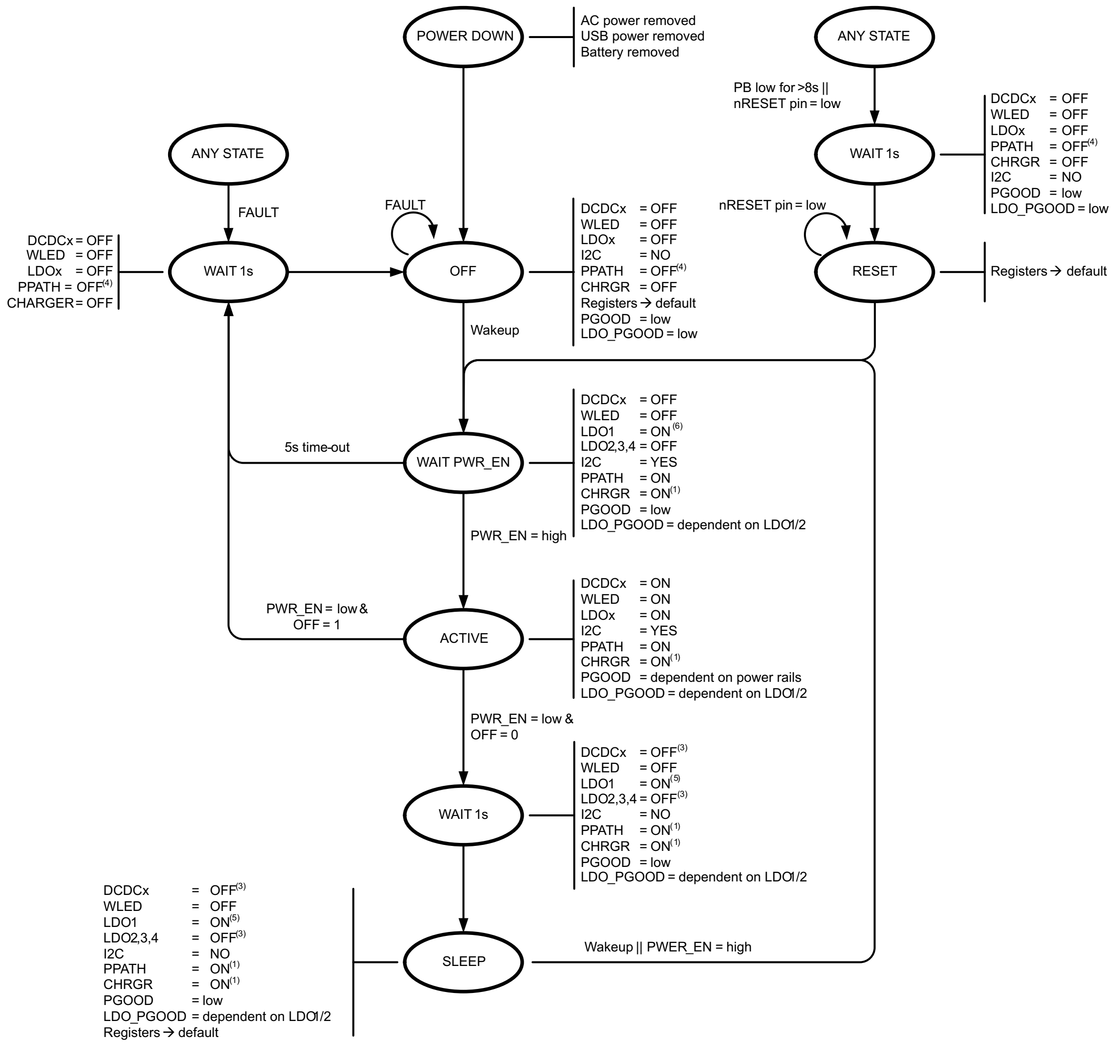
To enter the SLEEP state, set the OFF bit in the STATUS register to 0 (default), and then pull the PWR_EN pin low. All power rails controlled by the power-down sequencer are shut down, and after 1 seccond the device enters the SLEEP state. If LDO1 was enabled in the ACTIVE state, LDO1 remains enabled in the SLEEP sate. All rails not controlled by the power-down sequencer also maintain state. The battery charger remains active for as long as either the USB or AC supply is connected to the device. Note that all register values are reset when the device enters the SLEEP state, including charger parameters.

The device enters the ACTIVE state after detecting a wake-up event as described in the previous sections. In addition, the device transitions from the SLEEP to the ACTIVE state when the PWR_EN pin is pulled high. This allows the system host to switch the PMIC from the ACTIVE to the SLEEP state by control of the PWR_EN pin only.

RESET The TPS65217 device can be reset by either pulling the nRESET pin low or by holding the PB_IN pin low for more than 8 seconds. All rails are shut down by the sequencer and all register values are reset to their default values. Rails not controlled by the sequencer are shut down after the power-down sequencer has finished. The device remains in the this state for as long as the reset pin is held low, and the nRESET pin must be high to exit the RESET state. However, the device remains in the RESET state for a minimum of 1 second before returning to the ACTIVE state. As described under the the ACTIVE subsection in Modes of Operation, the PWR_EN pin must be asserted within 5 seconds of the nWAKEUP pin going low to enter the ACTIVE state. Note that the RESET function power-cycles the device and only shuts down the output rails temporarily. Resetting the device does not lead to the OFF state.

If the PB_IN pin is kept low for an extended amount of time, the device continues to cycle between the ACTIVE and RESET states, entering RESET every 8 seconds.

Device Functional Modes (continued)



NOTES:
Wakeup = V_{USB} (↑) || V_{AC} (↑) || PB (↓) || Returning from RESET state || SEQUP bit = 1
FAULT = UVLO || OTS || PGOOD low || PWR_EN pin not asserted within 5s of Wakeup event
If no battery is present, OVP on AC input also leads to OFF mode. With battery present, device switches automatically from AC to BAT if AC is >6.5V and back to AC when voltage recovers to <6.5V.
Device will remain in RESET state for at least 1s.
Sequencer is triggered when entering ACTIVE state

(1) Only if USB or AC supply is present
(3) All rails not controlled by the sequencer maintain state when entering SLEEP mode, i.e. they will not be powered down when entering SLEEP mode
(4) Battery voltage always supplies the system (SYS pin)
(5) LDO1/2 are not powered down when entering SLEEP mode if assigned to STROBE 14/15 or not under sequencer control. In SLEEP mode, LDO1 and 2 can source 1 mA only. By default LDO1 is asigned to STROBE15 and LDO2 to STROBE2.
(6) LDO1 and/or LDO2 are powered up if assigned to to STROBE 14/15. By default LDO1 is asigned to STROBE15 and LDO2 to STROBE2.

Figure 20. Global State Diagram

9.5 Programming

9.5.1 I²C Bus Operation

The TPS65217 device hosts a slave I²C interface that supports data rates up to 400 kbit/s and auto-increment addressing and is compliant to I²C standard 3.0.

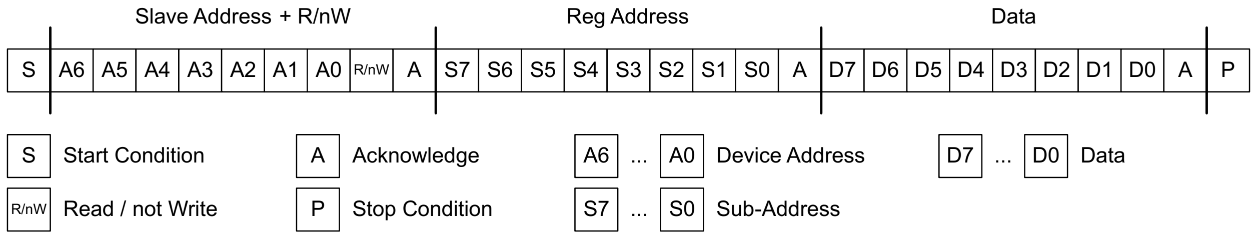
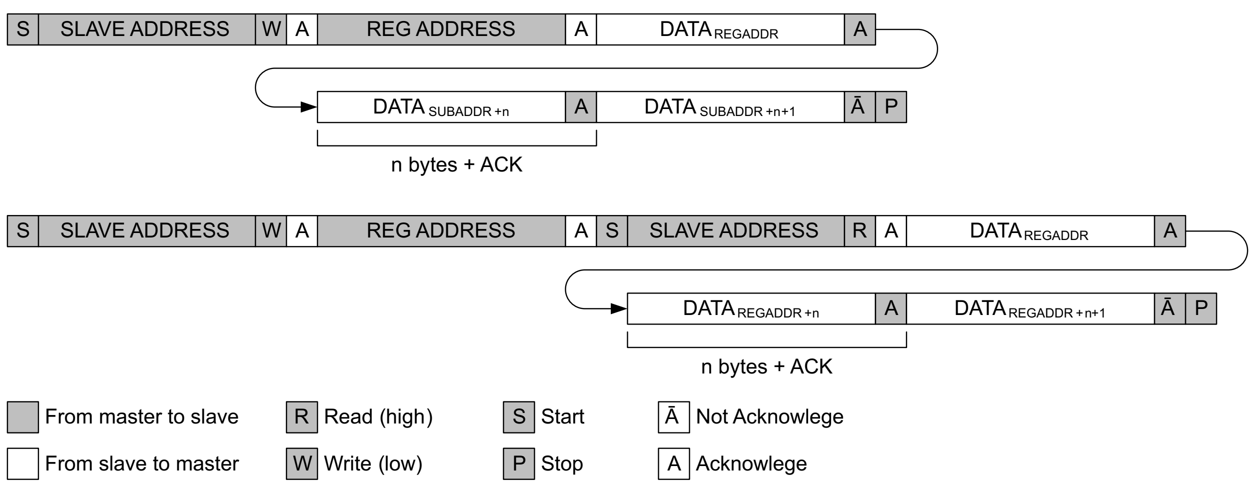


Figure 21. Subaddress in I²C Transmission

The I²C bus is a communications link between a controller and a series of slave terminals. The link is established using a two-wire bus consisting of a serial clock signal (SCL) and a serial data signal (SDA). The serial clock is sourced from the controller in all cases, where the serial data line is bidirectional for data communication, between the controller and the slave terminals. Each device has an open-drain output to transmit data on the serial data line. An external pullup resistor must be placed on the serial data line to pull the drain output high during data transmission.

Data transmission is initiated with a start bit from the controller as shown in Figure 23. The start condition is recognized when the SDA line transitions from high to low during the high portion of the SCL signal. On reception of a start bit, the device receives serial data on the SDA input and checks for valid address and control information. If the appropriate group and address bits are set for the device, then the device issues an acknowledge pulse and prepares for the reception of subaddress data. Subaddress data is decoded and responded to as per *Register Maps*. Data transmission is completed by either the reception of a stop condition or the reception of the data word sent to the device. A stop condition is recognized as a low-to-high transition of the SDA input during the high portion of the SCL signal. All other transitions of the SDA line must occur during the low portion of the SCL signal. An acknowledge is issued after the reception of valid address, subaddress and data words. The I²C interface auto-sequences through register addresses, so that multiple data words can be sent for a given I²C transmission. See Figure 22 and Figure 23 for details.



TOP: Master writes data to slave. BOTTOM: Master reads data from slave.

Figure 22. I²C Data Protocol

Programming (continued)

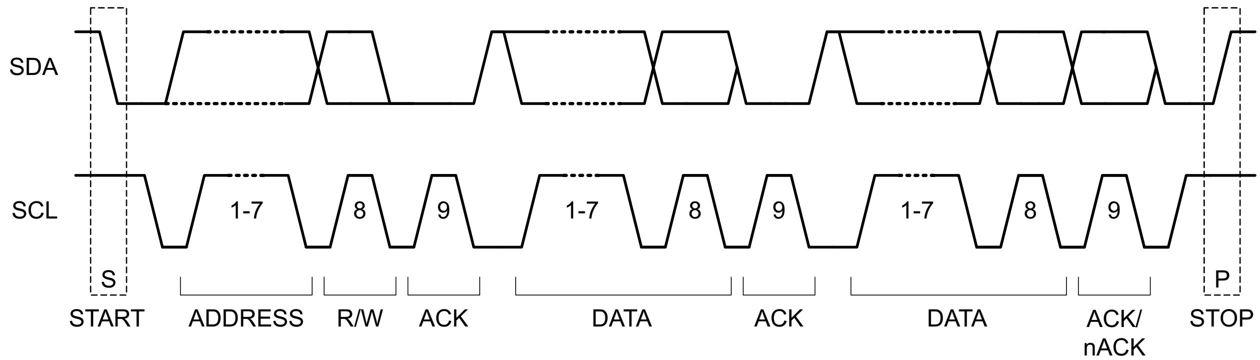


Figure 23. I²C Start-Stop-Acknowledge Protocol

9.5.2 Password Protection

Registers 0x0B through 0x1F with the exception of the password register are protected against accidental writing by an 8-bit password. The password must be written prior to writing to a protected register and is automatically reset to 0x00h after the following I²C transaction, regardless of the register that was accessed and regardless of the transaction type (read or write). The password is required for write access only and is not required for read access.

9.5.2.1 Level1 Protection

To write to a Level1 protected register:

1. Write the address of the destination register, XORed with the protection password (0x7Dh) to the PASSWORD register.
2. Write data to the password-protected register.
3. Only if the content of the PASSWORD register XORed with the address sent in step 2 matches 0x7Dh is the data transferred to the protected register. Otherwise, the transaction is ignored. In any case, the PASSWORD register is reset to 0x00 after the transaction.

The cycle must be repeated for any other register that is Level1 write protected.

9.5.2.2 Level2 Protection

To write to a Level2 protected register:

1. Write the address of the destination register, XORed with the protection password (0x7Dh) to the PASSWORD register.
2. Write to the password-protected register. The register value does not change at this point, but the data is temporarily stored if the content of the PASSWORD register XORed with the address sent in step 2 matches 0x7Dh. In any case, the PASSWORD register is reset to 0x00 after the transaction.
3. Write the address of the destination register, XORed with the protection password (0x7Dh) to the PASSWORD register.
4. Write the same data as in step 2 to the password protected register. Again, the content of the PASSWORD register XORed with the address sent in step 4 must match 0x7Dh for the data to be valid.
5. The register is updated only if both data transfers 2 and 4 were valid, and the transferred data matched.

Note that no other I²C transaction is allowed between steps 2 and 4, and the register is not updated if any other transaction occurs between steps 2 and 4. The cycle must be repeated for any other register that is Level2 write protected.

9.5.3 Reset to Default Values

All registers are reset to default values when one or more of the following conditions occur:

- The device transitions from the ACTIVE state to the SLEEP or OFF state.

Programming (continued)

- VBAT or VUSB is applied from a power-less state (power-on reset).
- The push-button input is pulled low for > 8 s.
- The nRESET pin is pulled low.
- A fault occurs.

9.6 Register Maps

9.6.1 Register Address Map

Figure 24. Register Address Map

REGISTER	ADDRESS (HEX)	NAME	PROTECTION	DEFAULT VALUE	DESCRIPTION
0	0	CHIPID	None	NA	Chip ID
1	1	PPATH	None	NA	Power path control
2	2	INT	None	NA	Interrupt flags and masks
3	3	CHGCONFIG0	None	NA	Charger control register 0
4	4	CHGCONFIG1	None	NA	Charger control register 1
5	5	CHGCONFIG2	None	NA	Charger control register 2
6	6	CHGCONFIG3	None	NA	Charger control register 3
7	7	WLEDCTRL1	None	NA	WLED control register
8	8	WLEDCTRL2	None	NA	WLED PWM duty cycle
9	9	MUXCTRL	None	NA	Analog multiplexer control register
10	0A	STATUS	None	NA	Status register
11	0B	PASSWORD	None	NA	Write password
12	0C	PGOOD	None	NA	Power good (PG) flags
13	0D	DEFPG	Level1	NA	Power good (PG) delay
14	0E	DEFDCDC1	Level2	NA	DCDC1 voltage adjustment
15	0F	DEFDCDC2	Level2	NA	DCDC2 voltage adjustment
16	10	DEFDCDC3	Level2	NA	DCDC3 voltage adjustment
17	11	DEFSLEW	Level2	NA	Slew control for DCDC1, DCDC2, DCDC3, and PFM mode enable
18	12	DEFLDO1	Level2	NA	LDO1 voltage adjustment
19	13	DEFLDO2	Level2	NA	LDO2 voltage adjustment
20	14	DEFLS1	Level2	NA	LS1 or LDO3 voltage adjustment
21	15	DEFLS2	Level2	NA	LS2 or LDO4 voltage adjustment
22	16	ENABLE	Level1	NA	Enable register
23	18	DEFUVLO	Level1	NA	UVLO control register
24	19	SEQ1	Level1	NA	Power-up STROBE definition
25	1A	SEQ2	Level1	NA	Power-up STROBE definition
26	1B	SEQ3	Level1	NA	Power-up STROBE definition
27	1C	SEQ4	Level1	NA	Power-up STROBE definition
28	1D	SEQ5	Level1	NA	Power-up delay times
29	1E	SEQ6	Level1	NA	Power-up delay times

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

9.6.2 Chip ID Register (CHIPID)

Figure 25. Chip ID Register (CHIPID) – Address – 0x00h

DATA BIT		D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME		CHIP[3:0]				REV[3:0]			
READ/WRITE		R	R	R	R	R	R	R	R
RESET VALUE	TPS65217A	0	1	1	1	0	0	1	0
	TPS65217B	1	1	1	1	0	0	1	0
	TPS65217C	1	1	1	0	0	0	1	0
	TPS65217D	0	1	1	0	0	0	1	0

Table 1. Chip ID Register (CHIPID) Field Descriptions

Bit	Field	Type	Reset	Description
D7–D4	CHIP[3:0]	R	TPS65217A: 0111 TPS65217B: 1111 TPS65217C: 1110 TPS65217D: 0110	Chip ID 0000 – Future use 0001 – Future use 0110 – TPS65217D 0111 – TPS65217A 1000 – Future use 1001 to 1101 – Reserved 1110 – TPS65217C 1111 – TPS65217B
D3–D0	REV[3:0]	R	0010	Revision code 0000 – revision 1.0 0001 – revision 1.1 0010 – revision 1.2 0011 to 1110 – Reserved 1111 – Future use

9.6.3 Power Path Control Register (PPATH)

Figure 26. Power Path Control Register (PPATH)
Address – 0x01h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	ACSINK	USBSINK	AC_EN	USB_EN	IAC[1:0]		IUSB[1:0]	
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	0	1	1	1	1	0	1

Table 2. Power Path Control Register (PPATH) Field Descriptions

Bit	Field	Type	Reset	Description
D7	ACSINK	R/W	0	AC current-sink control 0 – AC sink is enabled when USB is a valid supply and V_{AC} is below the detection threshold 1 – Set [ACSINK, USBSINK] = 11 to force both (AC and USB) current sinks OFF NOTE: [ACSINK, USBSINK] = 01b and 10b combinations are not recommended, as these may lead to unexpected enabling and disabling of the current sinks.
D6	USBSINK	R/W	1	USB current-sink control 0 – USB sink is enabled when AC is a valid supply and V_{USB} is below the detection threshold 1 – Set [ACSINK, USBSINK] = 11 to force both (AC and USB) current sinks OFF NOTE: [ACSINK, USBSINK] = 01b and 10b combinations are not recommended, as these may lead to unexpected enabling and disabling of the current sinks.
D5	AC_EN	R/W	1	AC power path enable 0 – AC power input is turned off. 1 – AC power input is turned on.
D4	USB_EN	R/W	1	USB power path enable 0 – USB power input is turned off (USB suspend mode). 1 – USB power input is turned on.
D3–D2	IAC[1:0]	R/W	1	AC input-current limit 00 – 100 mA 01 – 500 mA 10 – 1300 mA 11 – 2500 mA
D1–D0	IUSB[1:0]	R/W	1	USB input-current limit 00 – 100 mA 01 – 500 mA 10 – 1300 mA 11 – 1800 mA

9.6.4 Interrupt Register (INT)

Figure 27. Interrupt Register (INT)
Address – 0x02h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	Not used	PBM	ACM	USBM	Not used	PBI	ACI	USBI
READ/WRITE	R/W	R/W	R/W	R/W	R	R	R	R
RESET VALUE	1	0	0	0	0	0	0	0

Table 3. Interrupt Register (INT) Field Descriptions

Bit	Field	Type	Reset	Description
D7	Reserved	R/W	1	
D6	PBM	R/W	0	Pushbutton status change interrupt mask 0 – Interrupt is issued when PB status changes. 1 – No interrupt is issued when PB status changes.
D5	ACM	R/W	0	AC interrupt mask 0 – Interrupt is issued when power to the AC input is applied or removed. 1 – No interrupt is issued when power to the AC input is applied or removed.
D4	USBM	R/W	0	USB power status change interrupt mask 0 – Interrupt is issued when power to USB input is applied or removed. 1 – No interrupt is issued when power to USB input is applied or removed.
D3	Reserved	R	0	
D2	PBI	R	0	Push-button status change interrupt 0 – No change in status 1 – Pushbutton status change (PB_IN changed high to low or low to high) NOTE: Status information is available in the STATUS register.
D1	ACI	R	0	AC power status change interrupt 0 – No change in status 1 – AC power status change (power to the AC pin has either been applied or removed) NOTE: Status information is available in the STATUS register.
D0	USBI	R	0	USB power status change interrupt 0 – No change in status 1 – USB power status change (power to the USB pin has either been applied or removed) NOTE: Status information is available in the STATUS register.

9.6.5 Charger Configuration Register 0 (CHGCONFIG0)

Figure 28. Charger Configuration Register 0 (CHGCONFIG0) Address – 0x03h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	TREG	DPPM	TSUSP	TERMI	ACTIVE	CHGTOUT	PCHGTOUT	BATTEMP
READ/WRITE	R	R	R	R	R	R	R	R
RESET VALUE	0	0	0	0	0	0	0	0

Table 4. Charger Configuration Register 0 (CHGCONFIG0) Field Descriptions

Bit	Field	Type	Reset	Description
D7	TREG	R	0	Thermal regulation 0 – Charger is in normal operation. 1 – Charge current is reduced due to high chip temperature.
D6	DPPM	R	0	DPPM active 0 – DPPM loop is not active. 1 – DPPM loop is active; charge current is reduced to support the load with the current required.
D5	TSUSP	R	0	Thermal suspend 0 – Charging is allowed. 1 – Charging is temporarily suspended because battery temperature is out of range.
D4	TERMI	R	0	Termination current detect 0 – Charging, charge termination current threshold has not been crossed. 1 – Charge termination current threshold has been crossed and charging has been stopped. This can be due to a battery reaching full capacity or to a battery removal condition.
D3	ACTIVE	R	0	Charger active bit 0 – Charger is not charging. 1 – Charger is charging (DPPM or thermal regulation may be active).
D2	CHGTOUT	R	0	Charge timer time-out 0 – Charging, timers did not time out. 1 – One of the timers has timed out and charging has been terminated.
D1	PCHGTOUT	R	0	Precharge timer time-out 0 – Charging, precharge timer did not time out. 1 – Precharge timer has timed out and charging has been terminated.
D0	BATTEMP	R	0	BAT TEMP AND NTC ERROR 0 – Battery temperature is in the allowed range for charging. 1 – No temperature sensor detected or battery temperature outside valid charging range NOTE: This bit does not indicate that the battery temperature is within the valid range for charging.

9.6.6 Charger Configuration Register 1 (CHGCONFIG1)

Figure 29. Charger Configuration Register 1 (CHGCONFIG1) Address – 0x04h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	TIMER[1:0]		TMR_EN	NTC_TYPE	RESET	TERM	SUSP	CHG_EN
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	1	0	1	1	0	0	0	1

Table 5. Charger Configuration Register 1 (CHGCONFIG1) Field Descriptions

Bit	Field	Type	Reset	Description
D7–D6	TIMER[1:0]	R/W	10	Charge safety timer setting (fast-charge timer) 00 – 4h 01 – 5h 10 – 6h 11 – 8h
D5	TMR_EN	R/W	1	Safety timer enable 0 – Precharge timer and fast charge timer are disabled. 1 – Precharge timer and fast charge time are enabled.
D4	NTC_TYPE	R/W	1	NTC TYPE (for battery temperature measurement) 0 – 100k (curve 1, B = 3960) 1 – 10k (curve 2, B = 3480)
D3	RESET	R/W	0	Charger reset 0 – Inactive 1 – Reset active. This bit must be set and then reset via the serial interface to restart the charge algorithm.
D2	TERM	R/W	0	Charge termination on-off 0 – Charge termination enabled, based on timers and termination current 1 – Current-based charge termination does not occur and the charger is always on
D1	SUSP	R/W	0	Suspend charge 0 – Safety timer and precharge timers are not suspended. 1 – Safety timer and precharge timers are suspended.
D0	CHG_EN	R/W	1	Charger enable 0 – Charger is disabled. 1 – Charger is enabled.

9.6.7 Charger Configuration Register 2 (CHGCONFIG2)

Figure 30. Charger Configuration Register 2 (CHGCONFIG2) Address – 0x05h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	DYNTMR	VPRECHG	VOREG[1:0]		Reserved	Reserved	Reserved	Reserved
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	1	0	0	0	0	0	0	0

Table 6. Charger Configuration Register 2 (CHGCONFIG2) Field Descriptions

Bit	Field	Type	Reset	Description
D7	DYNTMR	R/W	1	Dynamic timer function 0 – Safety timers run with their nominal clock speed. 1 – Clock speed is divided by 2 if thermal loop or DPPM loop is active.
D6	VPRECHG	R/W	0	Precharge voltage 0 – Precharge to fast-charge transition voltage is 2.9 V. 1 – Precharge to fast-charge transition voltage is 2.5 V.
D5–D4	VOREG[1:0]	R/W	0	Charge voltage selection 00 – 4.1 V 01 – 4.15 V 10 – 4.2 V 11 – 4.2 V
D3–D0	Reserved	R	0	

9.6.8 Charger Configuration Register 3 (CHGCONFIG3)

Figure 31. Charger Configuration Register 3 (CHGCONFIG3) Address – 0x06h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	ICHRG[1:0]		DPPMTH[1:0]		PCHRGT	TERMIF[1:0]		TRANGE
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	1	0	1	1	0	0	1	0

Table 7. Charger Configuration Register 3 (CHGCONFIG3) Field Descriptions

Bit	Field	Type	Reset	Description
D7–D6	ICHRG[1:0]	R/W	10	Charge current setting 00 – 300 mA 01 – 400 mA 10 – 500 mA 11 – 700 mA
D5–D4	DPPMTH[1:0]	R/W	11	Power path DPPM threshold 00 – 3.5 V 01 – 3.75 V 10 – 4 V 11 – 4.25 V
D3	PCHRGT	R/W	0	Precharge time 0 – 30 min 1 – 60 min
D2–D1	TERMIF[1:0]	R/W	01	Termination current factor 00 – 2.5% 01 – 7.5% 10 – 15% 11 – 18% NOTE: Termination current = TERMIF x ICHRG
D0	TRANGE	R/W	0	Temperature range for charging 0 – 0°C–45°C 1 – 0°C–60°C

9.6.9 WLED Control Register 1 (WLEDCTRL1)

Figure 32. WLED Control Register 1 (WLEDCTRL1)
Address – 0x07h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	Not used	Not used	Not used	Not used	ISINK_EN	ISEL	FDIM[1:0]	
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	0	0	0	0	0	0	1

Table 8. WLED Control Register 1 (WLEDCTRL1) Field Descriptions

Bit	Field	Type	Reset	Description
D7–D4	Reserved	R/W	0	
D3	ISINK_EN	R/W	0	Current sink enable 0 – Current sink is disabled (OFF). 1 – Current sink is enabled (ON). NOTE: This bit enables both current sinks.
D2	ISEL	R/W	0	ISET selection bit 0 – Low-level (define by ISET1 pin) 1 – High-level (defined by ISET2 pin)
D1–D0	FDIM[1:0]	R/W	1	PWM dimming frequency 00 – 100 Hz 01 – 200 Hz 10 – 500 Hz 11 – 1000 Hz

9.6.10 WLED Control Register 2 (WLEDCTRL2)

Figure 33. WLED Control Register 2 (WLEDCTRL2) Address – 0x08h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	Not used	DUTY[6:0]						
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	0	0	0	0	0	0	0

Table 9. WLED Control Register 2 (WLEDCTRL2) Field Descriptions

Bit	Field	Type	Reset	Description
D7	Reserved	R/W	0	
D6–D0	DUTY[6:0]	R/W	0	000 0000 – 1% 000 0001 – 2% ... 110 0010 – 99% 110 0011 – 100% 110 0100 – 0% ... 111 1110 – 0% 111 1111 – 0%

9.6.11 MUX Control Register (MUXCTRL)

Figure 34. MUX Control Register (MUXCTRL)
Address – 0x09h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	Not used	Not used	Not used	Not used	Not used	MUX[2:0]		
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	0	0	0	0	0	0	0

Table 10. MUX Control Register (MUXCTRL) Field Descriptions

Bit	Field	Type	Reset	Description
D7–D3	Reserved	R/W	0	
D2–D0	MUX[2:0]	R/W	0	Analog multiplexer selection 000 – MUX is disabled, output is Hi-Z. 001 – VBAT 010 – VSYS 011 – VTS 100 – VICHARGE 101 – MUX_IN (external input) 110 – MUX is disabled, output is Hi-Z. 111 – MUX is disabled, output is Hi-Z.

9.6.12 Status Register (STATUS)

Figure 35. Status Register (STATUS)
Address – 0x0Ah

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	OFF	Not used	Not used	Not used	ACPWR	USBPWR	Not used	PB
READ/WRITE	R/W	R/W	R/W	R/W	R	R	R	R
RESET VALUE	0	0	0	0	0	0	0	0

Table 11. Status Register (STATUS) Field Descriptions

Bit	Field	Type	Reset	Description
D7	OFF	R/W	0	OFF bit. Set this bit to 1 to enter the OFF state when PWR_EN pin is pulled low. The bit is automatically reset to 0.
D6–D4	Reserved	R/W	0	
D3	ACPWR	R	0	AC power status bit 0 – AC power is not present and/or not in the range valid for charging. 1 – AC source is present and in the range valid for charging.
D2	USBPWR	R	0	USB power 0 – USB power is not present and/or not in the range valid for charging. 1 – USB source is present and in the range valid for charging.
D1	Reserved	R	0	
D0	PB	R	0	Push Button status bit 0 – Push-button is inactive (PB_IN is pulled high). 1 – Push-button is active (PB_IN is pulled low).

9.6.13 Password Register (PASSWORD)

**Figure 36. Password Register (PASSWORD)
Address – 0x0Bh**

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	PWRD[7:0]							
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	0	0	0	0	0	0	0

Table 12. Password Register (PASSWORD) Field Descriptions

Bit	Field	Type	Reset	Description
D7–D0	PWRD[7:0]	R/W	0	0000 0000 – Password-protected registers are locked for write access. ... 0111 1100 – Password-protected registers are locked for write access. 0111 1101 – Allows writing to a password-protected register in the next write cycle 0111 1110 – Password-protected registers are locked for write access. ... 1111 1111 – Password-protected registers are locked for write access. NOTE: Register is automatically reset to 0x00h after the following I^2C transaction. See the Password Protection section for details.

9.6.14 Power Good Register (PGOOD)

Figure 37. Power Good Register (PGOOD)
Address – 0x0Ch

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	Not used	LDO3_PG	LDO4_PG	DC1_PG	DC2_PG	DC3_PG	LDO1_PG	LDO2_PG
READ/WRITE	R/W	R	R	R	R	R	R	R
RESET VALUE	0	0	0	0	0	0	0	0

Table 13. Power-Good Register (PGOOD) Field Descriptions

Bit	Field	Type	Reset	Description
D7	Reserved	R/W	0	
D6	LDO3_PG	R	0	LDO3 power-good 0 – LDO is either disabled or not in regulation. 1 – LDO is in regulation or LS1 or LDO3 is configured as a switch.
D5	LDO4_PG	R	0	LDO4 power-good 0 – LDO is either disabled or not in regulation 1 – LDO is in regulation or LS2 or LDO4 is configured as a switch.
D4	DC1_PG	R	0	DCDC1 power-good 0 – DCDC1 is either disabled or not in regulation. 1 – DCDC1 is in regulation.
D3	DC2_PG	R	0	DCDC2 power-good 0 – DCDC2 is either disabled or not in regulation. 1 – DCDC2 is in regulation.
D2	DC3_PG	R	0	DCDC3 power-good 0 – DCDC3 is either disabled or not in regulation. 1 – DCDC3 is in regulation.
D1	LDO1_PG	R	0	LDO1 power-good. 0 – LDO is either disabled or not in regulation 1 – LDO is in regulation
D0	LDO2_PG	R	0	LDO2 power-good 0 – LDO is either disabled or not in regulation 1 – LDO is in regulation

9.6.15 Power-Good Control Register (DEFPG)

Figure 38. Power-Good Control Register (DEFPG)
Address – 0x0Dh (Password Protected)

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	Not used	Not used	Not used	Not used	LDO1PGM	LDO2PGM	PGDLY[1:0]	
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	0	0	0	1	1	0	0

Table 14. Power Good Control Register (DEFPG) Field Descriptions

Bit	Field	Type	Reset	Description
D7–D4	Reserved	R/W	0	
D3	LDO1PGM	R/W	1	LDO1 power-good masking bit 0 – PGOOD pin is pulled low if LDO1_PG is low 1 – LDO1_PG status does not affect the status of the PGOOD output pin.
D2	LDO2PGM	R/W	1	LDO2 power-good masking bit 0 – PGOOD pin is pulled low if LDO2_PG is low 1 – LDO2_PG status does not affect the status of the PGOOD output pin.
D1–D0	PGDLY[1:0]	R/W	0	Power-good delay 00 – 20 ms 01 – 100 ms 10 – 200 ms 11 – 400 ms Note: PGDLY applies to th ePGOOD pin.

9.6.16 DCDC1 Control Register (DEFDCDC1)

Figure 39. DCDC1 Control Register (DEFDCDC1)
Address – 0x0Eh (Password Protected)

DATA BIT		D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME		XADJ1	Not used	DCDC1[5:0]					
READ/WRITE		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	TPS65217A	0	0	0	1	1	1	1	0
	TPS65217B	0	0	0	1	1	1	1	0
	TPS65217C	0	0	0	1	1	0	0	0
	TPS65217D	0	0	0	1	0	0	1	0

Table 15. DCDC1 Control Register (DEFDCDC1) Field Descriptions

Bit	Field	Type	Reset	Description			
D7	XADJ1	R/W	0	DCDC1 voltage adjustment option 0 – Output voltage is adjusted through the register setting. 1 – Output voltage is externally adjusted.			
D6	Reserved	R/W	0				
D5–D0	DCDC1[5:0]	R/W	TPS65217A: 0111 TPS65217B: 0111 TPS65217C: 0110 TPS65217D: 0100	DCDC1 output-voltage setting			
				00 0000 – 0.9 V	01 0000 – 1.3 V	10 0000 – 1.9 V	11 0000 – 2.7 V
				00 0001 – 0.925 V	01 0001 – 1.325 V	10 0001 – 1.95 V	11 0001 – 2.75 V
				00 0010 – 0.95 V	01 0010 – 1.35 V	10 0010 – 2 V	11 0010 – 2.8 V
				00 0011 – 0.975 V	01 0011 – 1.375 V	10 0011 – 2.05 V	11 0011 – 2.85 V
				00 0100 – 1 V	01 0100 – 1.4 V	10 0100 – 2.1 V	11 0100 – 2.9 V
				00 0101 – 1.025 V	01 0101 – 1.425 V	10 0101 – 2.15 V	11 0101 – 3 V
				00 0110 – 1.05 V	01 0110 – 1.45 V	10 0110 – 2.2 V	11 0110 – 3.1 V
				00 0111 – 1.075 V	01 0111 – 1.475 V	10 0111 – 2.25 V	11 0111 – 3.2 V
				00 1000 – 1.1 V	01 1000 – 1.5 V	10 1000 – 2.3 V	11 1000 – 3.3 V
				00 1001 – 1.125 V	01 1001 – 1.55 V	10 1001 – 2.35 V	11 1001 – 3.3 V
				00 1010 – 1.15 V	01 1010 – 1.6 V	10 1010 – 2.4 V	11 1010 – 3.3 V
				00 1011 – 1.175 V	01 1011 – 1.65 V	10 1011 – 2.45 V	11 1011 – 3.3 V
				00 1100 – 1.2V	01 1100 – 1.7 V	10 1100 – 2.5 V	11 1100 – 3.3 V
				00 1101 – 1.225 V	01 1101 – 1.75 V	10 1101 – 2.55 V	11 1101 – 3.3 V
				00 1110 – 1.25 V	01 1110 – 1.80V	10 1110 – 2.6 V	11 1110 – 3.3 V
				00 1111 – 1.275 V	01 1111 – 1.85 V	10 1111 – 2.65 V	11 1111 – 3.3 V

9.6.17 DCDC2 Control Register (DEFDCDC2)

Figure 40. DCDC2 Control Register (DEFDCDC2)
Address – 0x0Fh (Password Protected)

DATA BIT		D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME		XADJ2	Not used	DCDC2[5:0]					
READ/WRITE		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	TPS65217A	0	0	1	1	1	0	0	0
	TPS65217B	0	0	0	0	1	0	0	0
	TPS65217C	0	0	0	0	1	0	0	0
	TPS65217D	0	0	0	0	1	0	0	0

Table 16. DCDC2 Control Register (DEFDCDC2) Field Descriptions

Bit	Field	Type	Reset	Description
D7	XADJ2	R/W	0	DCDC2 voltage adjustment option 0 – Output voltage is adjusted through the register setting. 1 – Output voltage is externally adjusted.
D6	Reserved	R/W	0	
D5–D0	DCDC2[5:0]	R/W	TPS65217A: 1110 TPS65217B: 0010 TPS65217C: 0010 TPS65217D: 0010	DCDC2 output voltage setting

00 0000 – 0.9 V	01 0000 – 1.3 V	10 0000 – 1.9 V	11 0000 – 2.7 V
00 0001 – 0.925 V	01 0001 – 1.325 V	10 0001 – 1.95 V	11 0001 – 2.75 V
00 0010 – 0.950V	01 0010 – 1.35 V	10 0010 – 2 V	11 0010 – 2.8 V
00 0011 – 0.975 V	01 0011 – 1.375 V	10 0011 – 2.05 V	11 0011 – 2.85 V
00 0100 – 1.V	01 0100 – 1.4 V	10 0100 – 2.1 V	11 0100 – 2.9 V
00 0101 – 1.025 V	01 0101 – 1.425 V	10 0101 – 2.15 V	11 0101 – 3 V
00 0110 – 1.05 V	01 0110 – 1.45 V	10 0110 – 2.2 V	11 0110 – 3.1 V
00 0111 – 1.075 V	01 0111 – 1.475 V	10 0111 – 2.25 V	11 0111 – 3.2 V
00 1000 – 1.1 V	01 1000 – 1.5 V	10 1000 – 2.3 V	11 1000 – 3.3 V
00 1001 – 1.125 V	01 1001 – 1.55 V	10 1001 – 2.35 V	11 1001 – 3.3 V
00 1010 – 1.15 V	01 1010 – 1.6 V	10 1010 – 2.4 V	11 1010 – 3.3 V
00 1011 – 1.175 V	01 1011 – 1.65 V	10 1011 – 2.45 V	11 1011 – 3.3 V
00 1100 – 1.2 V	01 1100 – 1.7 V	10 1100 – 2.5 V	11 1100 – 3.3 V
00 1101 – 1.225 V	01 1101 – 1.75 V	10 1101 – 2.55 V	11 1101 – 3.3 V
00 1110 – 1.25 V	01 1110 – 1.8 V	10 1110 – 2.6 V	11 1110 – 3.3 V
00 1111 – 1.275 V	01 1111 – 1.85 V	10 1111 – 2.65 V	11 1111 – 3.3 V

9.6.18 DCDC3 Control Register (DEFDCDC3)

Figure 41. DCDC3 Control Register (DEFDCDC3)
Address – 0x10h (Password Protected)

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	XADJ3	Not used	DCDC3[5:0]					
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	0	0	0	1	0	0	0

Table 17. DCDC3 Control Register (DEFDCDC3) Field Descriptions

Bit	Field	Type	Reset	Description			
D7	XADJ3	R/W	028	DCDC3 voltage adjustment option 0 – Output voltage is adjusted through register setting 1 – Output voltage is externally adjusted			
D6	Reserved	R/W	0				
D5–D0	DCDC3[5:0]	R/W	1000	DCDC3 output voltage setting			
				00 0000 – 0.9 V	01 0000 – 1.3 V	10 0000 – 1.9 V	11 0000 – 2.7 V
				00 0001 – 0.925 V	01 0001 – 1.325 V	10 0001 – 1.95 V	11 0001 – 2.75 V
				00 0010 – 0.95 V	01 0010 – 1.35 V	10 0010 – 2 V	11 0010 – 2.8 V
				00 0011 – 0.975 V	01 0011 – 1.375 V	10 0011 – 2.05 V	11 0011 – 2.85 V
				00 0100 – 1 V	01 0100 – 1.4 V	10 0100 – 2.1 V	11 0100 – 2.9 V
				00 0101 – 1.025 V	01 0101 – 1.425 V	10 0101 – 2.15 V	11 0101 – 3 V
				00 0110 – 1.05 V	01 0110 – 1.45 V	10 0110 – 2.2 V	11 0110 – 3.1 V
				00 0111 – 1.075 V	01 0111 – 1.475 V	10 0111 – 2.25 V	11 0111 – 3.2 V
				00 1000 – 1.1 V	01 1000 – 1.5 V	10 1000 – 2.30 V	11 1000 – 3.3 V
				00 1001 – 1.125 V	01 1001 – 1.55 V	10 1001 – 2.35 V	11 1001 – 3.3 V
				00 1010 – 1.15 V	01 1010 – 1.6 V	10 1010 – 2.4 V	11 1010 – 3.3 V
				00 1011 – 1.175 V	01 1011 – 1.65 V	10 1011 – 2.45 V	11 1011 – 3.3 V
				00 1100 – 1.2 V	01 1100 – 1.7 V	10 1100 – 2.5 V	11 1100 – 3.3 V
				00 1101 – 1.225 V	01 1101 – 1.75 V	10 1101 – 2.55 V	11 1101 – 3.3 V
				00 1110 – 1.25 V	01 1110 – 1.8 V	10 1110 – 2.6 V	11 1110 – 3.3 V
				00 1111 – 1.275 V	01 1111 – 1.85 V	10 1111 – 2.65 V	11 1111 – 3.3 V

9.6.19 Slew-Rate Control Register (DEFSLEW)

Figure 42. Slew-Rate Control Register (DEFSLEW)
Address – 0x11h (Password Protected)

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	GO	GODSBL	PFM_EN1	PFM_EN2	PFM_EN3	SLEW[2:0]		
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	0	0	0	0	1	1	0

Table 18. Slew-Rate Control Register (DEFSLEW) Field Descriptions

Bit	Field	Type	Reset	Description(1)
D7	GO	R/W	0	Go bit 0 – No change 1 – Initiates the transition from the present state to the output voltage setting currently stored in the DEFDCDCx register NOTE: Bit is automatically reset at the end of the voltage transition.
D6	GODSBL	R/W	0	Go Disable bit 0 – Enabled 1 – Disabled; DCDCx output voltage changes whenever setpoint is updated in DEFDCDCx register without having to write to the GO bit. SLEW[2:0] setting does apply.
D5	PFM_EN1	R/W	0	PFM enable bit, DCDC1 0 – DC-DC converter operates in the PWM or PFM mode, depending on load. 1 – DC-DC converter is forced into the fixed-frequency PWM mode.
D4	PFM_EN2	R/W	0	PFM enable bit, DCDC2 0 – DC-DC converter operates in the PWM or PFM mode, depending on load. 1 – DC-DC converter is forced into the fixed-frequency PWM mode.
D3	PFM_EN3	R/W	0	PFM enable bit, DCDC3 0 – DC-DC converter operates in the PWM or PFM mode, depending on load. 1 – DC-DC converter is forced into the fixed-frequency PWM mode.
D2–D0	SLEW[2:0]	R/W	0110	Output slew-rate setting 000 – 224 µs/step (0.11 mV/µs at 25 mV per step) 001 – 112 µs/step (0.22 mV/µs at 25 mV per step) 010 – 56 µs/step (0.45 mV/µs at 25 mV per step) 011 – 28 µs/step (0.90 mV/µs at 25 mV per step) 100 – 14 µs/step (1.80 mV/µs at 25 mV per step) 101 – 7 µs/step (3.60 mV/µs at 25 mV per step) 110 – 3.5 µs/step (7.2 mV/µs at 25 mV per step) 111 – Immediate; slew rate is only limited by the control loop response time. Note: The actual slew rate depends on the voltage step per code. See the DCDC1 and DCDC2 registers for details.

(1) Slew-rate control applies to all three dc-dc converters.

9.6.20 LDO1 Control Register (DEFLDO1)

**Figure 43. LDO1 Control Register (DEFLDO1)
Address – 0x12h (Password Protected)**

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	Not used	Not used	Not used	Not used	LDO1[3:0]			
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	0	0	0	1	0	0	1

Table 19. LDO1 Control Register (DEFLDO1) Field Descriptions

Bit	Field	Type	Reset	Description	
D7–D4	Reserved	R/W	0		
D3–D0	LDO1[3:0]	R/W	1001	LDO1 output voltage setting	
				0000 – 1 V	1000 – 1.6 V
				0001 – 1.1 V	1001 – 1.8 V
				0010 – 1.2 V	1010 – 2.5 V
				0011 – 1.25 V	1011 – 2.75 V
				0100 – 1.3 V	1100 – 2.8 V
				0101 – 1.35 V	1101 – 3 V
				0110 – 1.4 V	1110 – 3.1 V
				0111 – 1.5 V	1111 – 3.3 V

9.6.21 LDO2 Control Register (DEFLDO2)

Figure 44. LDO2 Control Register (DEFLDO2)
Address – 0x13h (Password Protected)

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	Not used	TRACK	LDO2[5:0]					
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	0	1	1	1	0	0	0

Table 20. LDO2 Control Register (DEFLDO2) Field Descriptions

Bit	Field	Type	Reset	Description			
D7	Reserved	R/W	0				
D6	TRACK	R/W	0	LDO2 tracking bit 0 – Output voltage is defined by the LDO2[5:0] bits. 1 – Output voltage follows the DCDC3 voltage setting (DEFDCDC3 register).			
D5–D0	LDO2[5:0]	R/W	1110	LDO2 output voltage setting			
				00 0000 – 0.9 V	01 0000 – 1.3 V	10 0000 – 1.9 V	11 0000 – 2.7 V
				00 0001 – 0.925 V	01 0001 – 1.325 V	10 0001 – 1.95 V	11 0001 – 2.75 V
				00 0010 – 0.95 V	01 0010 – 1.35 V	10 0010 – 2 V	11 0010 – 2.8 V
				00 0011 – 0.975 V	01 0011 – 1.375 V	10 0011 – 2.05 V	11 0011 – 2.85 V
				00 0100 – 1 V	01 0100 – 1.4 V	10 0100 – 2.1 V	11 0100 – 2.9 V
				00 0101 – 1.025 V	01 0101 – 1.425 V	10 0101 – 2.15 V	11 0101 – 3 V
				00 0110 – 1.05 V	01 0110 – 1.45 V	10 0110 – 2.2 V	11 0110 – 3.1 V
				00 0111 – 1.075 V	01 0111 – 1.475 V	10 0111 – 2.25 V	11 0111 – 3.2 V
				00 1000 – 1.1 V	01 1000 – 1.5 V	10 1000 – 2.3 V	11 1000 – 3.3 V
				00 1001 – 1.125 V	01 1001 – 1.55 V	10 1001 – 2.35 V	11 1001 – 3.3 V
				00 1010 – 1.15 V	01 1010 – 1.60 V	10 1010 – 2.4 V	11 1010 – 3.3 V
				00 1011 – 1.175 V	01 1011 – 1.65 V	10 1011 – 2.45 V	11 1011 – 3.3 V
				00 1100 – 1.2 V	01 1100 – 1.7 V	10 1100 – 2.5 V	11 1100 – 3.3 V
				00 1101 – 1.225 V	01 1101 – 1.75 V	10 1101 – 2.55 V	11 1101 – 3.3 V
				00 1110 – 1.25 V	01 1110 – 1.8 V	10 1110 – 2.6 V	11 1110 – 3.3 V
				00 1111 – 1.275 V	01 1111 – 1.85 V	10 1111 – 2.65 V	11 1111 – 3.3 V

9.6.22 Load Switch1 or LDO3 Control Register (DEFLS1)

Figure 45. Load Switch1 or LDO3 Control Register (DEFLS1) Address – 0x14h (Password Protected)

DATA BIT		D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME		Not used	Not used	LS1LDO3	LDO3[4:0]				
READ/WRITE		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	TPS65217A	0	0	0	0	0	1	1	0
	TPS65217B	0	0	1	1	1	1	1	1
	TPS65217C	0	0	1	0	0	1	1	0
	TPS65217D	0	0	1	0	0	1	1	0

Table 21. Load Switch1 or LDO3 Control Register Field Descriptions

Bit	Field	Type	Reset	Description	
D7–D6	Reserved	R/W	0		
D5	LS1LDO3	R/W	TPS65217A: 0 TPS65217B: 1 TPS65217C: 1 TPS65217D: 1	LS or LDO tracking bit 0 – FET functions as load switch (LS1). 1 – FET is configured as LDO3.	
D5–D0	LDO3[5:0]	R/W	1110	LDO3 output voltage setting	
				0 0000 – 1.5 V	01 0000 – 2.55 V
				0 0001 – 1.55 V	01 0001 – 2.6 V
				0 0010 – 1.6 V	01 0010 – 2.65 V
				0 0011 – 1.65 V	01 0011 – 2.7 V
				0 0100 – 1.7 V	01 0100 – 2.75 V
				0 0101 – 1.75 V	01 0101 – 2.8 V
				0 0110 – 1.8 V	01 0110 – 2.85 V
				0 0111 – 1.85 V	01 0111 – 2.9 V
				0 1000 – 1.90V	01 1000 – 2.95 V
				0 1001 – 2 V	01 1001 – 3 V
				0 1010 – 2.1 V	01 1010 – 3.05 V
				0 1011 – 2.2 V	01 1011 – 3.1 V
				0 1100 – 2.3 V	01 1100 – 3.15 V
				0 1101 – 2.4 V	01 1101 – 3.2 V
				0 1110 – 2.45 V	01 1110 – 3.25 V
				0 1111 – 2.5 V	01 1111 – 3.3 V

9.6.23 Load Switch2 or LDO4 Control Register (DEFLS2)

Figure 46. Load Switch2 or LDO4 Control Register (DEFLS2)
Address – 0x15h (Password Protected)

DATA BIT		D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME		Not used	Not used	LS2LDO4	LDO4[4:0]				
READ/WRITE		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	TPS65217A	0	0	0	1	0	1	0	1
	TPS65217B	0	0	1	1	1	1	1	1
	TPS65217C	0	0	1	1	1	1	1	1
	TPS65217D	0	0	1	1	1	1	1	1

Table 22. Load Switch2 or LDO4 Control Register (DEFLS2) Field Descriptions

Bit	Field	Type	Reset	Description	
D7–D6	Reserved	R/W	0		
D5	LS1LDO4	R/W	TPS65217A: 0 TPS65217B: 1 TPS65217C: 1 TPS65217D: 1	LS or LDO configuration bit 0 – FET functions as load a switch (LS2). 1 – FET is configured as LDO4.	
D5–D0	LDO4[5:0]	R/W	TPS65217A: 1010 TPS65217B: 1111 TPS65217C: 1111 TPS65217D: 1111	LDO4 output voltage setting (LS2LDO4 = 1)	
				0 0000 – 1.5 V	01 0000 – 2.55 V
				0 0001 – 1.55 V	01 0001 – 2.6 V
				0 0010 – 1.6 V	01 0010 – 2.65 V
				0 0011 – 1.65 V	01 0011 – 2.7 V
				0 0100 – 1.7 V	01 0100 – 2.75 V
				0 0101 – 1.75 V	01 0101 – 2.8 V
				0 0110 – 1.8 V	01 0110 – 2.85 V
				0 0111 – 1.85 V	01 0111 – 2.9 V
				0 1000 – 1.9 V	01 1000 – 2.95 V
				0 1001 – 2 V	01 1001 – 3 V
				0 1010 – 2.1 V	01 1010 – 3.05 V
				0 1011 – 2.2 V	01 1011 – 3.1 V
				0 1100 – 2.3 V	01 1100 – 3.15 V
				0 1101 – 2.4 V	01 1101 – 3.2 V
				0 1110 – 2.45 V	01 1110 – 3.25 V
				0 1111 – 2.5 V	01 1111 – 3.3 V

9.6.24 Enable Register (ENABLE)

Figure 47. Enable Register (ENABLE)
Address – 0x16h (Password Protected)

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	Not used	LS1_EN	LS2_EN	DC1_EN	DC2_EN	DC3_EN	LDO1_EN	LDO2_EN
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	0	0	0	0	0	0	0

Table 23. Enable Register (ENABLE) Field Descriptions

Bit	Field	Type	Reset	Description
D7	Reserved	R/W	0	
D6	LS1_EN	R/W	0	Load switch1 or LDO3 enable bit 0 – Disabled 1 – Enabled NOTE: PWR_EN pin must be high to enable LS1 or LDO3.
D5	LS2_EN	R/W	0	Load switch2 or LDO4 enable bit 0 – Disabled 1 – Enabled NOTE: PWR_EN pin must be high to enable LS2 or LDO4.
D4	DC1_EN	R/W	0	DCDC1 enable bit 0 – DCDC1 is disabled. 1 – DCDC1 is enabled. NOTE: PWR_EN pin must be high to enable the dc-dc converter.
D3	DC2_EN	R/W	0	DCDC2 enable bit 0 – DCDC2 is disabled. 1 – DCDC2 is enabled. NOTE: PWR_EN pin must be high to enable the dc-dc converter.
D2	DC3_EN	R/W	0	DCDC3 enable bit 0 – DCDC3 is disabled. 1 – DCDC3 is enabled. NOTE: PWR_EN pin must be high to enable the dc-dc converter.
D1	LDO1_EN	R/W	0	LDO1 enable bit 0 – Disabled 1 – Enabled
D0	LDO2_EN	R/W	0	LDO2 enable bit 0 – Disabled 1 – Enabled

9.6.25 UVLO Control Register (DEFUVLO)

Figure 48. UVLO Control Register (DEFUVLO)
Address – 0x18h (Password Protected)

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	Not used	Not used	Not used	Not used	Not used	Not used	UVLO[1:0]	
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	0	0	0	0	0	1	1

Table 24. UVLO Control Register (DEFUVLO) Field Descriptions

Bit	Field	Type	Reset	Description
D7–D2	Reserved	R/W	0	
D1–D0	UVLO[1:0]	R/W	0011	Undervoltage lockout setting 00 – 2.73 V 01 – 2.89 V 10 – 3.18 V 11 – 3.3 V

9.6.26 Sequencer Register 1 (SEQ1)

Figure 49. Sequencer Register 1 (SEQ1)
Address – 0x19h (Password Protected)

DATA BIT		D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME		DC1_SEQ[3:0]				DC2_SEQ[3:0]			
READ/WRITE		R	R/W	R/W	R/W	R	R/W	R/W	R/W
RESET VALUE	TPS65217A	0	0	0	1	0	0	1	0
	TPS65217B	0	0	0	1	0	1	0	1
	TPS65217C	0	0	0	1	0	1	0	1
	TPS65217D	0	0	0	1	0	1	0	1

Table 25. Sequencer Register 1 (SEQ1) Field Descriptions

Bit	Field	Type	Reset	Description
D7–D4	DC1_SEQ[3:0]	R/W	TPS65217A: 0001 TPS65217B: 0001 TPS65217C: 0001 TPS65217D: 0001	DCDC1 enable STROBE 0000 – Rail is not controlled by sequencer. 0001 – Enable at STROBE1 0010 – Enable at STROBE2 0011 – Enable at STROBE3 0100 – Enable at STROBE4 0101 – Enable at STROBE5 0110 – Enable at STROBE6 0111 – Enable at STROBE7
D3–D0	DC2_SEQ[3:0]	R/W	TPS65217A: 0010 TPS65217B: 0101 TPS65217C: 0101 TPS65217D: 0101	DCDC2 enable STROBE 0000 – Rail is not controlled by sequencer. 0001 – Enable at STROBE1 0010 – Enable at STROBE2 0011 – Enable at STROBE3 0100 – Enable at STROBE4 0101 – Enable at STROBE5 0110 – Enable at STROBE6 0111 – Enable at STROBE7

9.6.27 Sequencer Register 2 (SEQ2)

Figure 50. Sequencer Register 2 (SEQ2)
Address – 0x1Ah (Password Protected)

DATA BIT		D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME		DC3_SEQ[3:0]				LDO1_SEQ[3:0]			
READ/WRITE		R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	TPS65217A	0	0	1	1	1	0	1	1
	TPS65217B	0	1	0	1	1	1	1	1
	TPS65217C	0	1	0	1	1	1	1	1
	TPS65217D	0	1	0	1	1	1	1	1

Table 26. Sequencer Register 2 (SEQ2) Field Descriptions

Bit	Field	Type	Reset	Description
D7–D4	DC3_SEQ[3:0]	R/W	TPS65217A: 0011 TPS65217B: 0101 TPS65217C: 0101 TPS65217D: 0101	DCDC3 enable STROBE 0000 – Rail is not controlled by sequencer. 0001 – Enable at STROBE1 0010 – Enable at STROBE2 0011 – Enable at STROBE3 0100 – Enable at STROBE4 0101 – Enable at STROBE5 0110 – Enable at STROBE6 0111 – Enable at STROBE7 1000 to 1111 – Reserved
D3–D0	LDO1_SEQ[3:0]	R/W	TPS65217A: 1011 TPS65217B: 1111 TPS65217C: 1111 TPS65217D: 1111	LDO1 enable state 0000 – Rail is not controlled by sequencer. 0001 – Enable at STROBE1 0010 – Enable at STROBE2 0011 – Enable at STROBE3 0100 – Enable at STROBE4 0101 – Enable at STROBE5 0110 – Enable at STROBE6 0111 – Enable at STROBE7 1000 – Rail is not controlled by sequencer 1001 – Rail is not controlled by sequencer 1010 to 1101 – Reserved 1110 – Enable at STROBE14 1111 – Enabled at STROBE15 (with SYS)

9.6.28 Sequencer Register 3 (SEQ3)

Figure 51. Sequencer Register 3 (SEQ3)
Address – 0x1Bh (Password Protected)

DATA BIT		D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME		LDO2_SEQ[3:0]				LDO3_SEQ[3:0]			
READ/WRITE		R/WR	R/W	R/W	R/W	R	R/W	R/W	R/W
RESET VALUE	TPS65217A	0	0	1	0	0	0	0	1
	TPS65217B	0	0	1	0	0	0	1	1
	TPS65217C	0	0	1	1	0	0	1	0
	TPS65217D	0	0	1	1	0	0	1	0

Table 27. Sequencer Register 3 (SEQ3) Field Descriptions

Bit	Field	Type	Reset	Description
D7–D4	LDO2_SEQ[3:0]	R/W	TPS65217A: 0010 TPS65217B: 0010 TPS65217C: 0011 TPS65217D: 0011	LDO2 enable STROBE 0000 – Rail is not controlled by sequencer. 0001 – Enable at STROBE1 0010 – Enable at STROBE2 0011 – Enable at STROBE3 0100 – Enable at STROBE4 0101 – Enable at STROBE5 0110 – Enable at STROBE6 0111 – Enable at STROBE7 1000 – Rail is not controlled by sequencer. 1001 – Rail is not controlled by sequencer. 1010 to 1101 – Reserved 1110 – Enable at STROBE14 1111 – Enabled at STROBE15 (with SYS)
D3–D0	LDO3_SEQ[3:0]	R/W	TPS65217A: 0001 TPS65217B: 0011 TPS65217C: 0010 TPS65217D: 0010	LS1 or LDO3 enable state 0000 – Rail is not controlled by sequencer 0001 – Enable at STROBE1 0010 – Enable at STROBE2 0011 – Enable at STROBE3 0100 – Enable at STROBE4 0101 – Enable at STROBE5 0110 – Enable at STROBE6 0111 – Enable at STROBE7 1000 to 1111 – Reserved

9.6.29 Sequencer Register 4 (SEQ4)

**Figure 52. Sequencer Register 4 (SEQ4)
Address – 0x1Ch (Password Protected)**

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	LDO4_SEQ[3:0]				Not used	Not used	Not used	Not used
READ/WRITE	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	1	0	0	0	0	0	0

Table 28. Sequencer Register 4 (SEQ4) Field Descriptions

Bit	Field	Type	Reset	Description
D7–D4	LDO4_SEQ[3:0]	R/W	0100	LS2 or LDO4 enable state 0000 – Rail is not controlled by sequencer. 0001 – Enable at STROBE1 0010 – Enable at STROBE2 0011 – Enable at STROBE3 0100 – Enable at STROBE4 0101 – Enable at STROBE5 0110 – Enable at STROBE6 0111 – Enable at STROBE7
D3–D0	Reserved	R/W	0	

9.6.30 Sequencer Register 5 (SEQ5)

Figure 53. Sequencer Register 5 (SEQ5)
Address – 0x1Dh (Password Protected)

DATA BIT		D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME		DLY1[1:0]		DLY2[1:0]		DLY3[1:0]		DLY4[1:0]	
READ/WRITE		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	TPS65217A	1	0	0	0	0	0	0	0
	TPS65217B	1	0	0	0	0	0	0	0
	TPS65217C	0	0	1	0	0	0	0	0
	TPS65217D	0	0	1	0	0	0	0	0

Table 29. Sequencer Register 5 (SEQ5) Field Descriptions

Bit	Field	Type	Reset	Description
D7–D6	DLY1[1:0]	R/W	TPS65217A: 10 TPS65217B: 10 TPS65217C: 0 TPS65217D: 0	Delay1 time 00 – 1 ms 01 – 2 ms 10 – 5 ms 11 – 10 ms
D5–D4	DLY2[1:0]	R/W	TPS65217A: 0 TPS65217B: 0 TPS65217C: 10 TPS65217D: 10	Delay2 time 00 – 1 ms 01 – 2 ms 10 – 5 ms 11 – 10 ms
D3–D2	DLY3[1:0]	R/W	0	Delay3 time 00 – 1 ms 01 – 2 ms 10 – 5 ms 11 – 10 ms
D1–D0	DLY4[1:0]	R/W	0	Delay4 time 00 – 1 ms 01 – 2 ms 10 – 5 ms 11 – 10 ms

9.6.31 Sequencer Register 6 (SEQ6)

Figure 54. Sequencer Register 6 (SEQ6) Address – 0x1Eh (Password Protected)

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	DLY5[1:0]		DLY6[1:0]		Not used	SEQUP	SEQDWN	INSTDWN
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	0	0	0	0	0	0	0

Table 30. Sequencer Register 6 (SEQ6) Field Descriptions

Bit	Field	Type	Reset	Description
D7–D6	DLY5[1:0]	R/W	0	Delay5 time 00 – 1 ms 01 – 2 ms 10 – 5 ms 11 – 10 ms
D5–D4	DLY6[1:0]	R/W	0	Delay6 time 00 – 1 ms 01 – 2 ms 10 – 5 ms 11 – 10 ms
D3	Reserved	R/W	0	
D2	SEQUP	R/W	0	Set this bit to 1 to trigger a power-up sequence. Bit is automatically reset to 0.
D1	SEQDWN	R/W	0	Set this bit to 1 to trigger a power-down sequence. Bit is automatically reset to 0.
D0	INSTDWN	R/W	0	Instant-shutdown bit 0 – Shutdown follows reverse power-up sequence 1 – All delays are bypassed and all rails are shut down simultaneously. NOTE: Shutdown occurs when the PWR_EN pin is pulled low or the SEQDWN bit is set. Only those rails controlled by the sequencer are shut down.

10 Application and Implementation

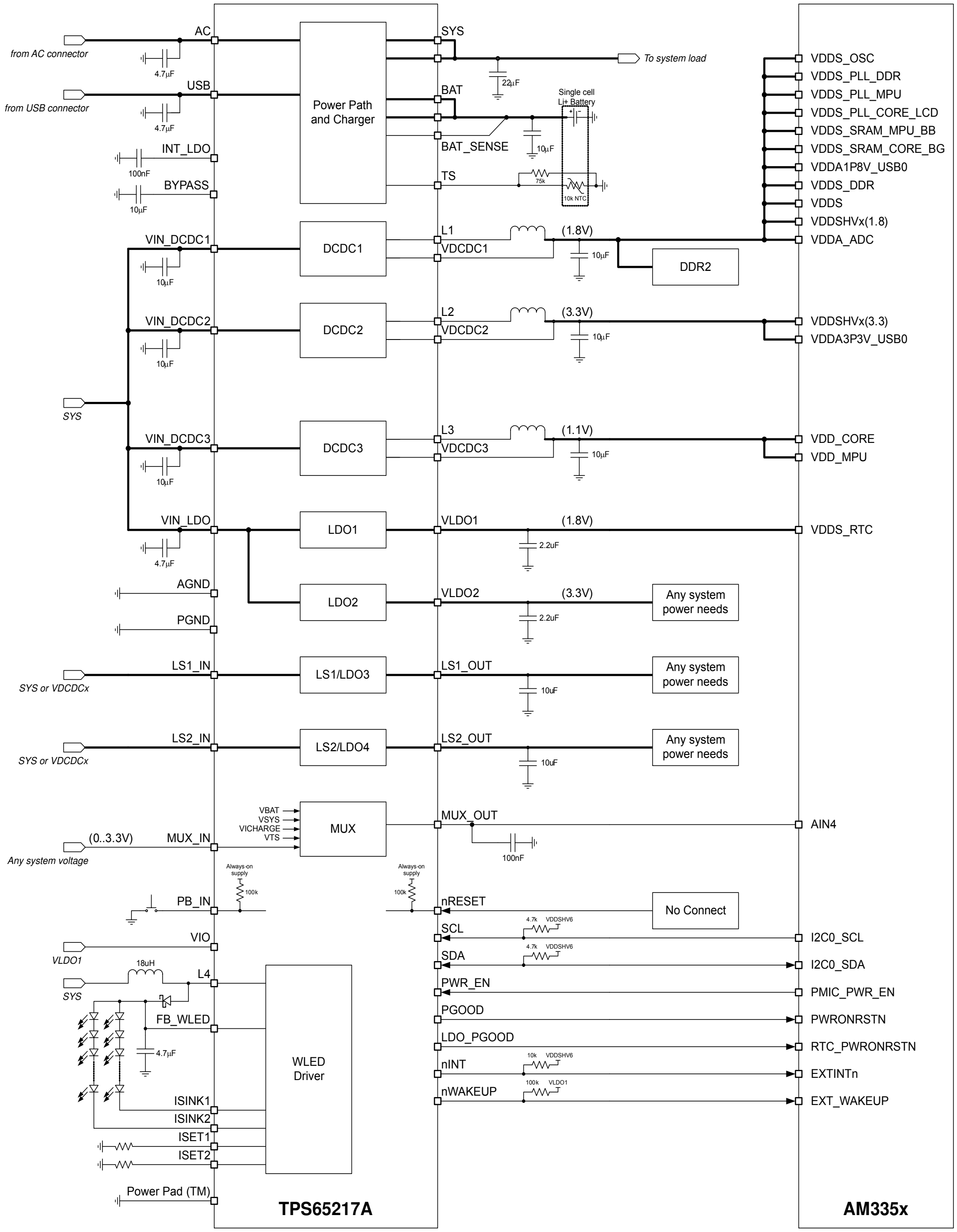
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPS65217 device is designed to pair with various application processors. For detailed information on using the TPS65217 device with Sitara AM335x processors, see *Powering the AM335x with TPS65217* (SLVU551).

10.2 Typical Application



See SLVU551 for connection diagrams for all members of the TPS65217x family.

Figure 55. Connection Diagram for Typical Application

Typical Application (continued)

10.2.1 Design Requirements

Table 31. Design Requirements

	VOLTAGE	SEQUENCE
DCDC1	1.8 V	1
DCDC2	3.3 V	2
DCDC3	1.1 V	3
LDO1	1.8 V	15
LDO2	3.3 V	2
LS1 or LDO3	Load switch	1
LS2 or LDO4	Load switch	4

10.2.2 Detailed Design Procedure

Table 32. Recommended Inductors for WLED Boost Converter

PART NUMBER	SUPPLIER	VALUE (µH)	R_{DS} (mΩ) MAX	RATED CURRENT (A)	DIMENSIONS (mm × mm × mm)
CDRH74NP-180M	Sumida	18	73	1.31	7.5 × 7.5 × 4.5
P1167.183	Pulse	18	37	1.5	7.5 × 7.5 × 4.5

Table 33. Recommended Output Capacitor for WLED Boost Converter

PART NUMBER	SUPPLIER	VOLTAGE RATING (V)	VALUE (µF)	DIMENSIONS	DIELECTRIC
UMK316BJ475ML-T	Taiyo Yuden	50	4.7	1206	X5R

10.2.2.1 Output Filter Design (Inductor and Output Capacitor)

10.2.2.1.1 Inductor Selection for Buck Converters

The step-down converters operate typically with 2.2-µH output inductors. Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. The selected inductor must be rated for its dc resistance and saturation current. The dc resistance of the inductance directly influences the efficiency of the converter. Therefore, an inductor with lowest dc resistance should be selected for highest efficiency.

The following formula can be used to calculate the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current, because during heavy load transients the inductor current rises above the calculated value.

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \tag{4}$$

$$I_{L\,max} = I_{OUT\,max} + \frac{\Delta I_L}{2}$$

where

- f = Switching frequency (2.25 MHz typical)
- L = Inductor value
- ΔI_L = Peak to peak inductor ripple current
- I_{Lmax} = Maximum inductor current (5)

The highest inductor current occurs at maximum V_{IN}. Open-core inductors have a soft saturation characteristic and can usually handle higher inductor currents than a comparable shielded inductor.

A more conservative approach is to select the inductor current rating just for the maximum switch current of the corresponding converter. It must be considered that the core material from inductor to inductor differs and has an impact on the efficiency, especially at high switching frequencies. Also, the resistance of the windings greatly affects the converter efficiency at high load. See Table 34 for recommended inductors.

Table 34. Recommended Inductors for DCDC1, DCDC2, and DCDC3

PART NUMBER	SUPPLIER	VALUE (µH)	R_{DS} (mΩ) MAX	RATED CURRENT (A)	DIMENSIONS (mm)
LQM2HPN2R2MG0L	Murata	2.2	100	1.3	2 x 2.5 x 0.9
VLCF4018T-2R2N1R4-2	TDK	2.2	60	1.44	3.9 x 4.7 x 1.8

10.2.2.1.2 Output Capacitor Selection

The advanced fast-response voltage-mode control scheme of the two converters allows the use of small ceramic capacitors with a typical value of 10 µF, without having large output voltage under- and overshoots during heavy load transients. Ceramic capacitors having low ESR values result in the lowest output voltage ripple and are therefore recommended.

If ceramic output capacitors are used, the capacitor rms ripple-current rating must always meet the application requirements. For completeness, the rms ripple current is calculated as:

$$I_{RMSCout} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (6)$$

At nominal load current, the inductive converters operate in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta V_{OUT} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \left(\frac{1}{8 \times C_{OUT} \times f} + ESR \right)$$

where

- the highest output voltage ripple occurs at the highest input voltage V_{IN} (7)

At light load currents, the converters operate in power-save mode, and the output-voltage ripple depends on the output capacitor value. The output-voltage ripple is set by the internal comparator delay and the external capacitor. The typical output-voltage ripple is less than 1% of the nominal output voltage.

10.2.2.1.3 Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low-ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input-voltage spikes. The converters require a ceramic input capacitor of 10 µF. The input capacitor can be increased without any limit for better input voltage filtering. See Table 35 for recommended ceramic capacitors.

Table 35. Recommended Input Capacitors for DCDC1, DCDC2, and DCDC3

PART NUMBER	SUPPLIER	VALUE (µF)	DIMENSIONS
C2012X5R0J226MT	TDK	22	0805
JMK212BJ226MG	Taiyo Yuden	22	0805
JMK212BJ106M	Taiyo Yuden	10	0805
C2012X5R0J106M	TDK	10	0805

10.2.2.2 5-V Operation Without a Battery

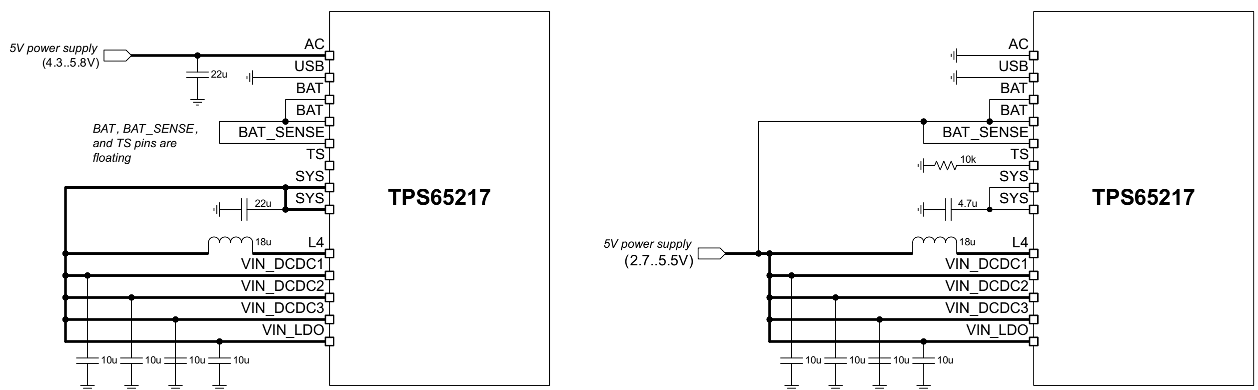
The TPS65217 device provides a linear charger for Li+ batteries, but the IC can operate without a battery attached. There are three basic use cases for operation without a battery:

1. The system is designed for battery operation, but the battery is not inserted. The system can be powered by connecting an ac adaptor or USB supply.
2. A non-portable system running on a (regulated) 5-V supply, but the PMIC must provide protection against

input overvoltage up to 20 V. Electrically, this is the same as the previous case where the IC is powered by an ac adaptor. The battery pins (BAT, BATSENSE, TS) are floating, and power is provided through the AC pin. The dc-dc converters, the WLED driver, and the LDOs connect to the overvoltage-protected SYS pins. Load switches (or LDO3 and LDO4, depending on configuration) typically connect to one of the lower system rails, but may also be connected to the SYS pin.

3. A non-portable system running on a regulated 5-V supply that does not require input overvoltage protection. In this case, the 5-V power supply is connected through the BAT pins, and the dc-dc converter inputs, WLED driver, LDO1, and LDO2 are connected directly to the 5-V supply. A 10-kΩ resistor is connected from TS to ground to simulate the NTC thermistor monitoring the battery. Load switches (or LDO3 and LDO4, depending on configuration) typically connect to one of the lower system rails, but may also be connected to the 5-V input supply directly. The main advantage of connecting the supply to the BAT pins is higher power efficiency, because the internal power path is bypassed and power loss across the internal switches is avoided.

Figure 56 shows the connection of the input power supply to the IC for 5-V only operation with and without 20-V input overvoltage protection and Table 36 lists the functional differences between both setups.



Left: Power-connection for 5-V only operation without a battery. The SYS node and dc-dc converters are protected against input overvoltage up to 20 V.
Right: Power-connection for 5-V only operation. The dc-dc converters are not protected against input overvoltage, but power efficiency is higher because the internal power-path switches are bypassed.

Figure 56. Power Connection for 5-V Only Operation Without a Battery and Power Connection for 5-V Only Operation

Table 36. Functional Differences Between 5-V Only Operation Without a Battery and With and Without 20-V Input Overvoltage Protection

RESOURCE IMPACTED	POWER SUPPLIED THROUGH AC PIN (CASE (1) AND (2))	POWER SUPPLIED THROUGH BAT PIN (CASE (3))
Input protection	Maximum operating input voltage is 5.8 V, but IC is protected against input overvoltage up to 20 V.	Maximum operating input voltage is 5.5 V.
Power efficiency	Iinput current for dc-dc converters passes through AC-SYS power-path switch (approximately 150 mΩ).	Internal power path is bypassed to minimize I^2R losses.
BATTEMP bit	BATTEMP bit (bit 0 in register 0x03h) always reads 1, but has no effect on operation of the part.	BATTEMP bit (bit 0 in register 0x03h) always reads 0.
Output rail status on initial power connection	LDO1 is automatically powered up when the AC pin is connected to the 5-V supply, and the device enters the [WAIT PWR_EN] state. IF the PWR_EN pin is not asserted within 5s, LDO1 turns OFF.	LDO1 is OFF when BAT is connected to the 5-V supply. PB_IN must be pulled low to enter the [WAIT PWR_EN] state.
Response to input overvoltage	Device enters the OFF mode. NOTE: If a battery is present in the system, the TPS65217 device automatically switches from the AC to to the BAT supply when the AC input exceeds 6.5 V and back to AC when the AC input recovers to a safe operating voltage range.	NA.

Table 36. Functional Differences Between 5-V Only Operation Without a Battery and With and Without 20-V Input Overvoltage Protection (continued)

RESOURCE IMPACTED	POWER SUPPLIED THROUGH AC PIN (CASE (1) AND (2))	POWER SUPPLIED THROUGH BAT PIN (CASE (3))
Power path	In an application with one source of input power, if the input power drops below UVLO and recovers before reaching 100 mV, the rising edge may not be detected by the power path. This causes a brownout state.[1]	NA

(1) As a workaround, supply power through the BAT input terminal or change UVLO to 2.73 V.

10.2.3 Application Curves

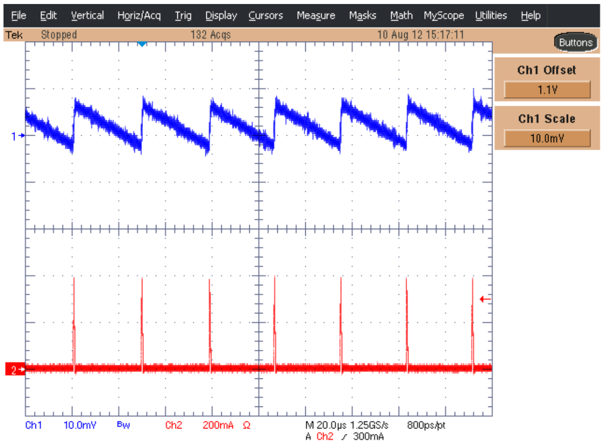


Figure 57. DCDC Inductor Current at 5 mA, 1.1-V Voltage Ripple

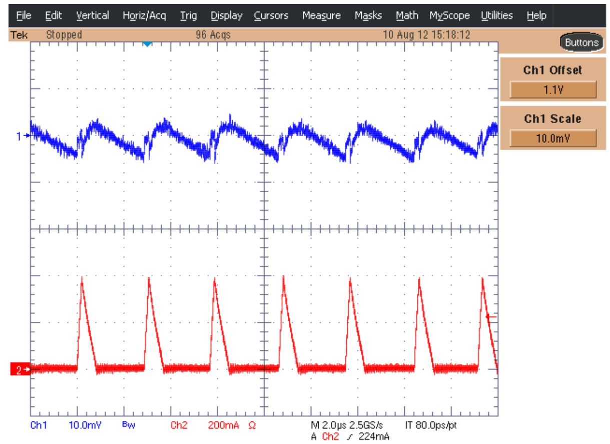


Figure 58. DCDC Inductor Current at 50 mA, 1.1-V Voltage Ripple

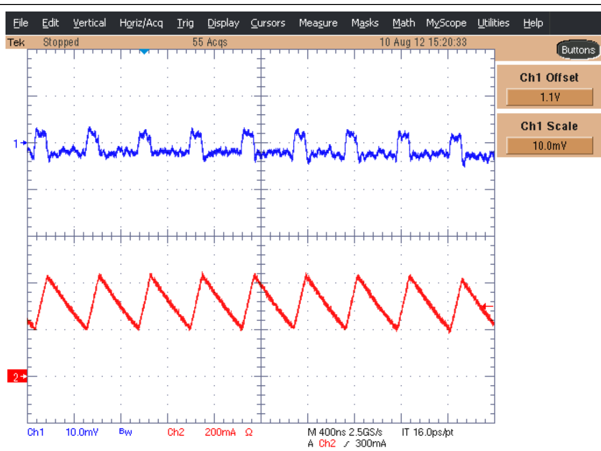


Figure 59. DCDC Inductor Current at 300 mA, 1.1-V Voltage Ripple

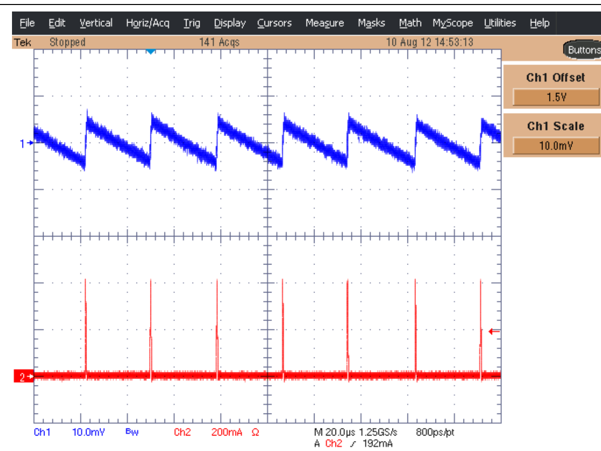


Figure 60. DCDC Inductor Current at 5 mA, 1.5-V Voltage Ripple

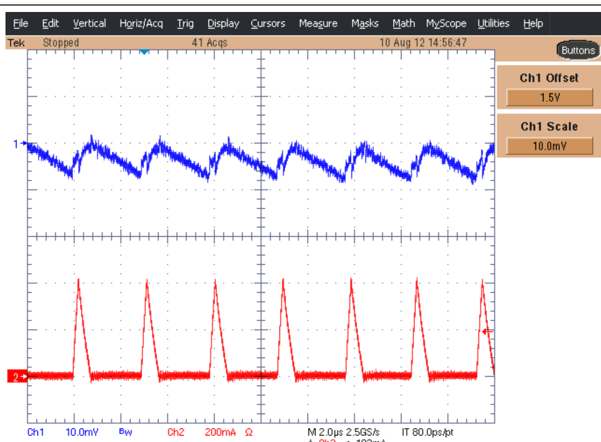


Figure 61. DCDC Inductor Current at 50 mA, 1.5-V Voltage Ripple

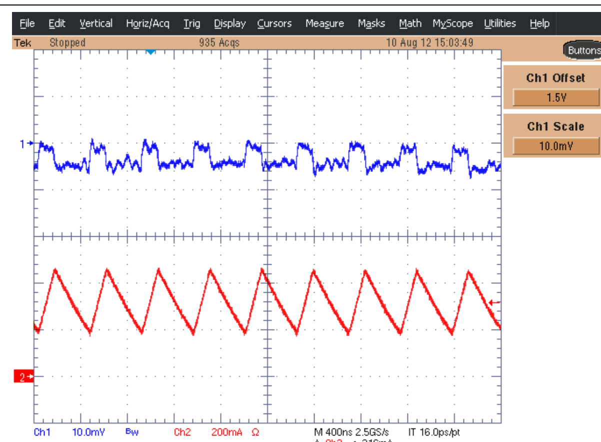


Figure 62. DCDC Inductor Current at 300 mA, 1.5-V Voltage Ripple

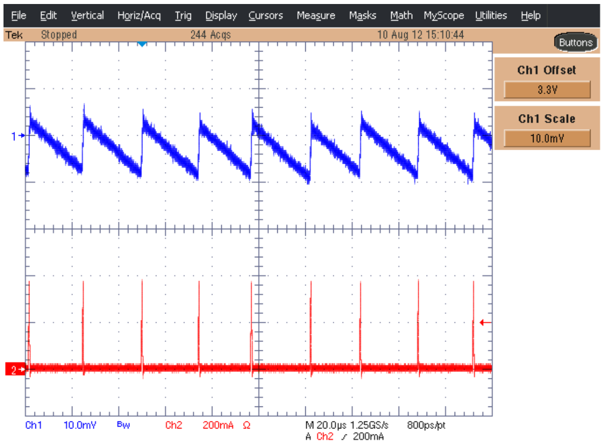


Figure 63. DCDC Inductor Current at 5 mA, 3.3-V Voltage Ripple

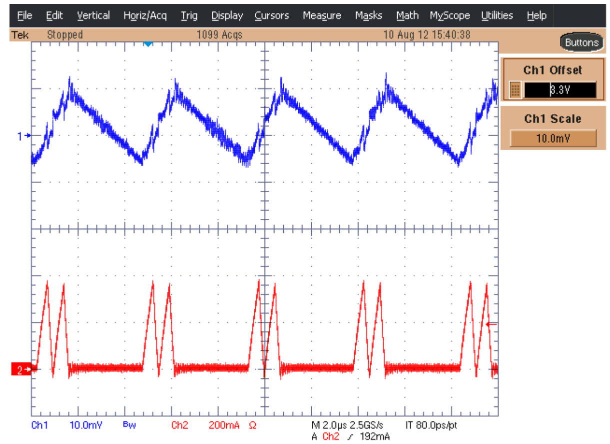


Figure 64. DCDC Inductor Current at 50 mA, 3.3-V Voltage Ripple

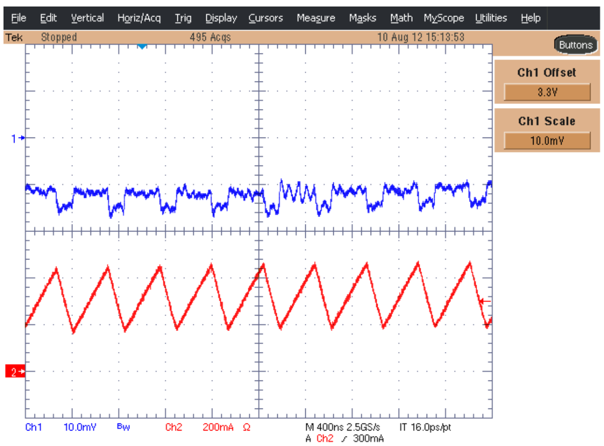


Figure 65. DCDC Inductor Current at 300 mA, 3.3-V Voltage Ripple

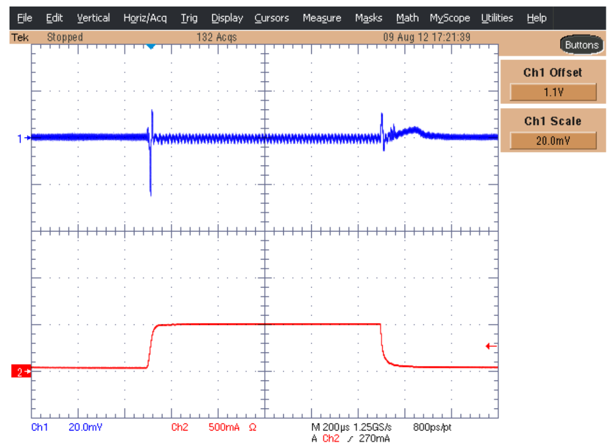


Figure 66. DCDC Load Transient, 1.1 V Out, 50-500-50 mA

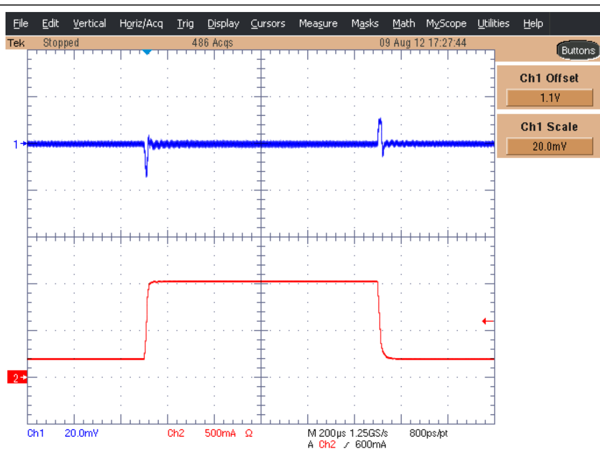


Figure 67. DCDC Load Transient, 1.1 V Out, 200-1000-200 mA

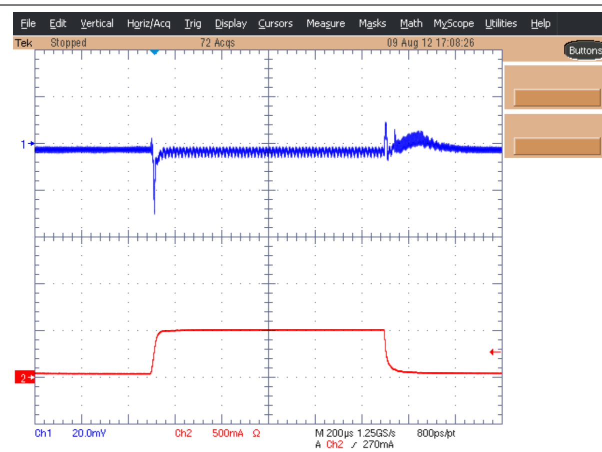


Figure 68. DCDC Load Transient, 1.5 V Out, 50-500-50 mA

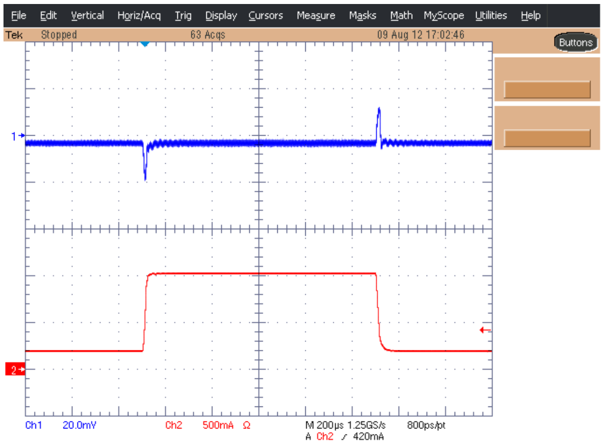


Figure 69. DCDC Load Transient, 1.5 V Out, 200-1000-200 mA

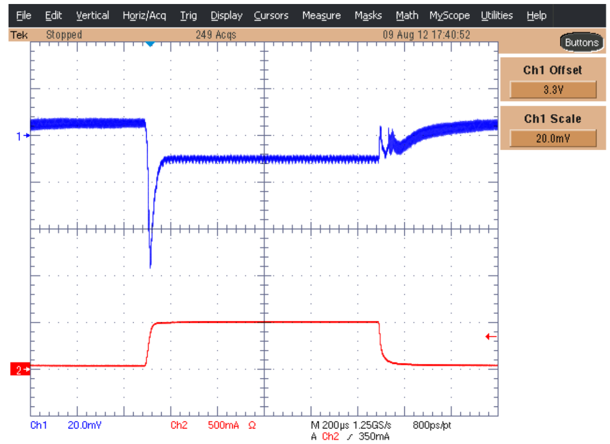


Figure 70. DCDC Load Transient, 3.3 V Out, 50-500-50 mA

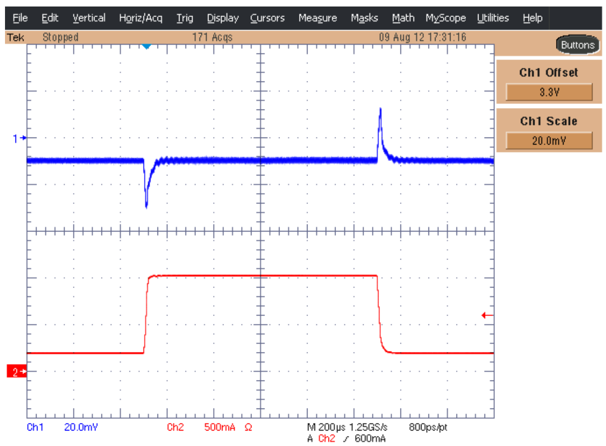


Figure 71. DCDC Load Transient, 3.3-V Out, 200-1000-200 mA

11 Power Supply Recommendations

The device is designed to operate with an input voltage supply range between 2.75 V and 5.8 V. This input supply can be from a single-cell Li-ion, Li-polymer batteries, dc supply, USB supply, or other externally regulated supply. If the input supply is located more than a few inches from the TPS65217 device, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 4.7 µF is a typical choice.

12 Layout

12.1 Layout Guidelines

- The VIN_DCDCx and VINLDO pins should be bypassed to ground with a low-ESR ceramic bypass capacitor. The typical recommended bypass capacitance is 10 μF and 4.7 μF with a X5R or X7R dielectric, respectively.
- The optimum placement is closest to the VIN_DCDCx and VINLDO pins of the device. Care should be taken to minimize the loop area formed by the bypass capacitor connection, the VIN_DCDCx and VINLDO pins, and the thermal pad of the device.
- The thermal pad should be tied to the PCB ground plane with multiple vias.
- The LX trace should be kept on the PCB top layer and free of any vias.
- The VLDOx and VDCDCx pin (feedback pin) traces should be routed away from any potential noise source to avoid coupling.
- DCDCx output capacitance should be placed immediately at the DCDCx pin. Excessive distance between the capacitance and DCDCx pin may cause poor converter performance.

12.2 Layout Example

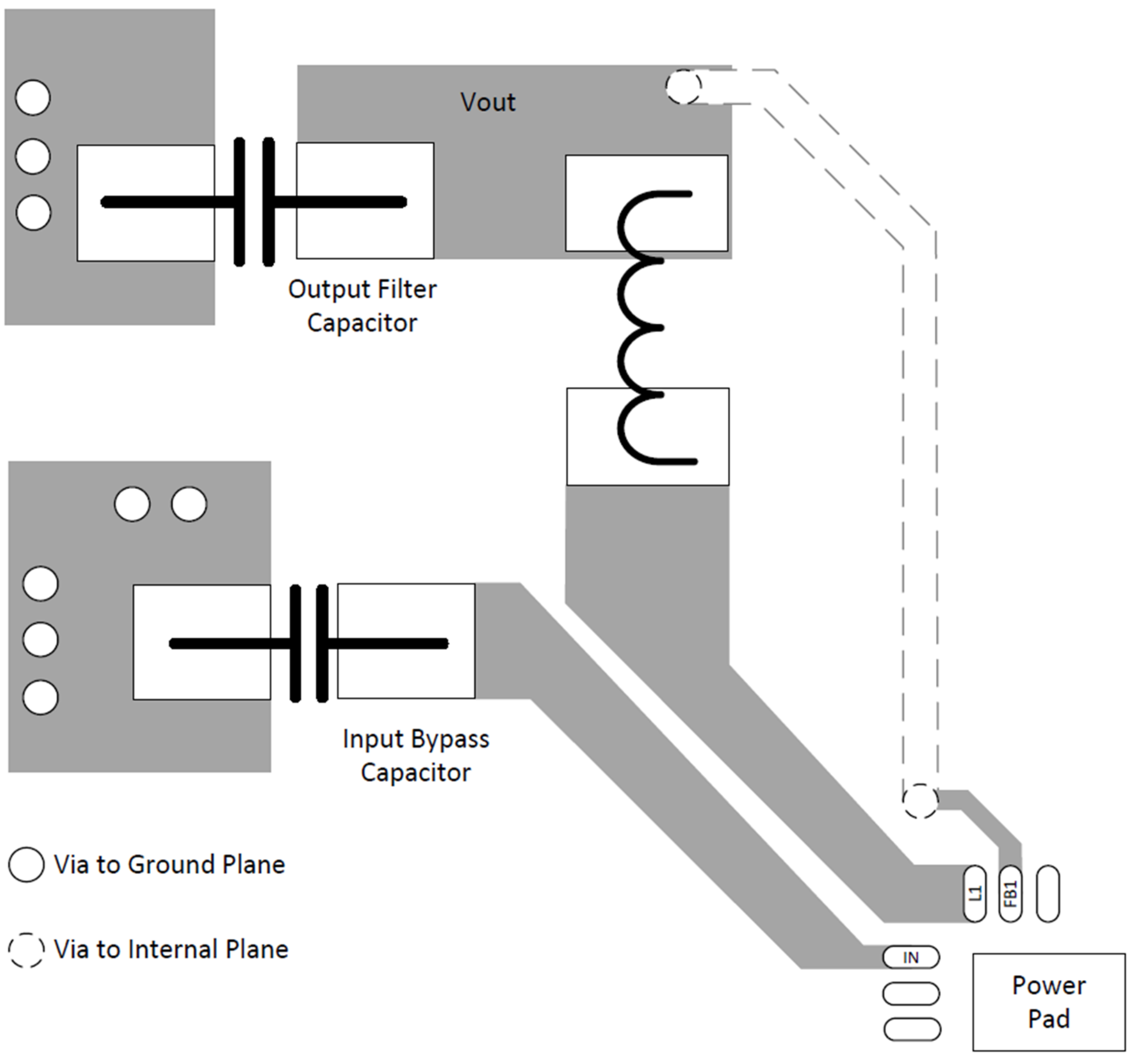


Figure 72. Layout Example Schematic

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

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13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65217ARSLR	ACTIVE	VQFN	RSL	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	TPS 65217A	Samples
TPS65217ARSLT	ACTIVE	VQFN	RSL	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	TPS 65217A	Samples
TPS65217BRSLR	ACTIVE	VQFN	RSL	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	TPS 65217B	Samples
TPS65217BRSLT	ACTIVE	VQFN	RSL	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	TPS 65217B	Samples
TPS65217CRSLR	ACTIVE	VQFN	RSL	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	TPS 65217C	Samples
TPS65217CRSLT	ACTIVE	VQFN	RSL	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	TPS 65217C	Samples
TPS65217DRSLR	ACTIVE	VQFN	RSL	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	TPS 65217D	Samples
TPS65217DRSLT	ACTIVE	VQFN	RSL	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	TPS 65217D	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

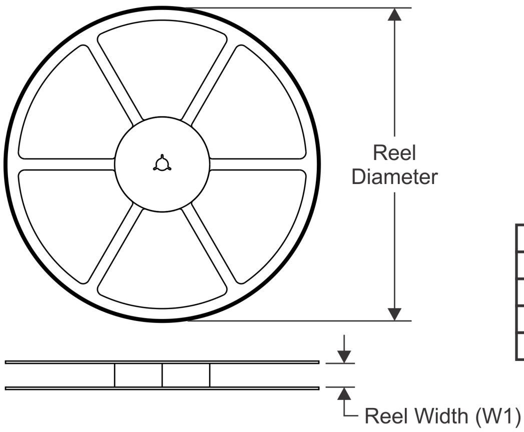
[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

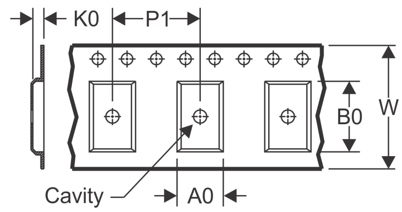
[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

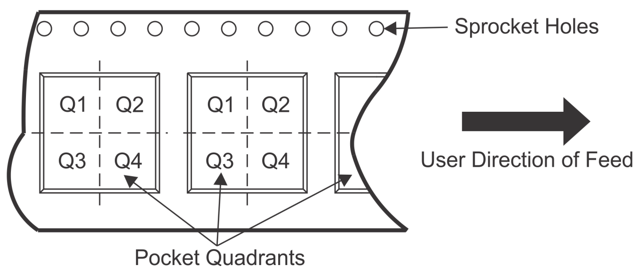


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

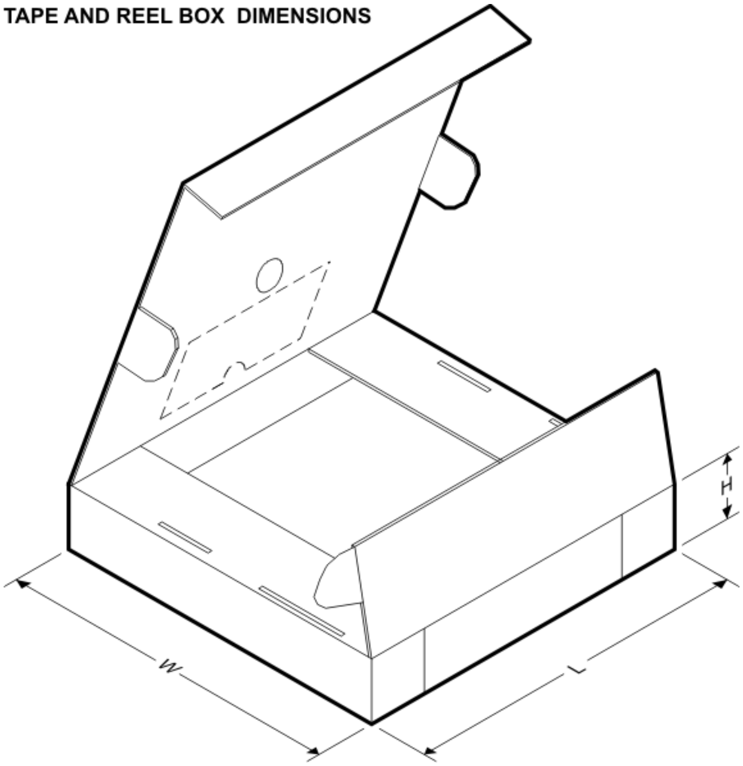
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65217ARSLR	VQFN	RSL	48	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65217ARSLT	VQFN	RSL	48	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65217BRSLR	VQFN	RSL	48	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65217BRSLT	VQFN	RSL	48	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65217CRSLR	VQFN	RSL	48	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65217CRSLT	VQFN	RSL	48	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65217DRSLR	VQFN	RSL	48	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65217DRSLT	VQFN	RSL	48	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

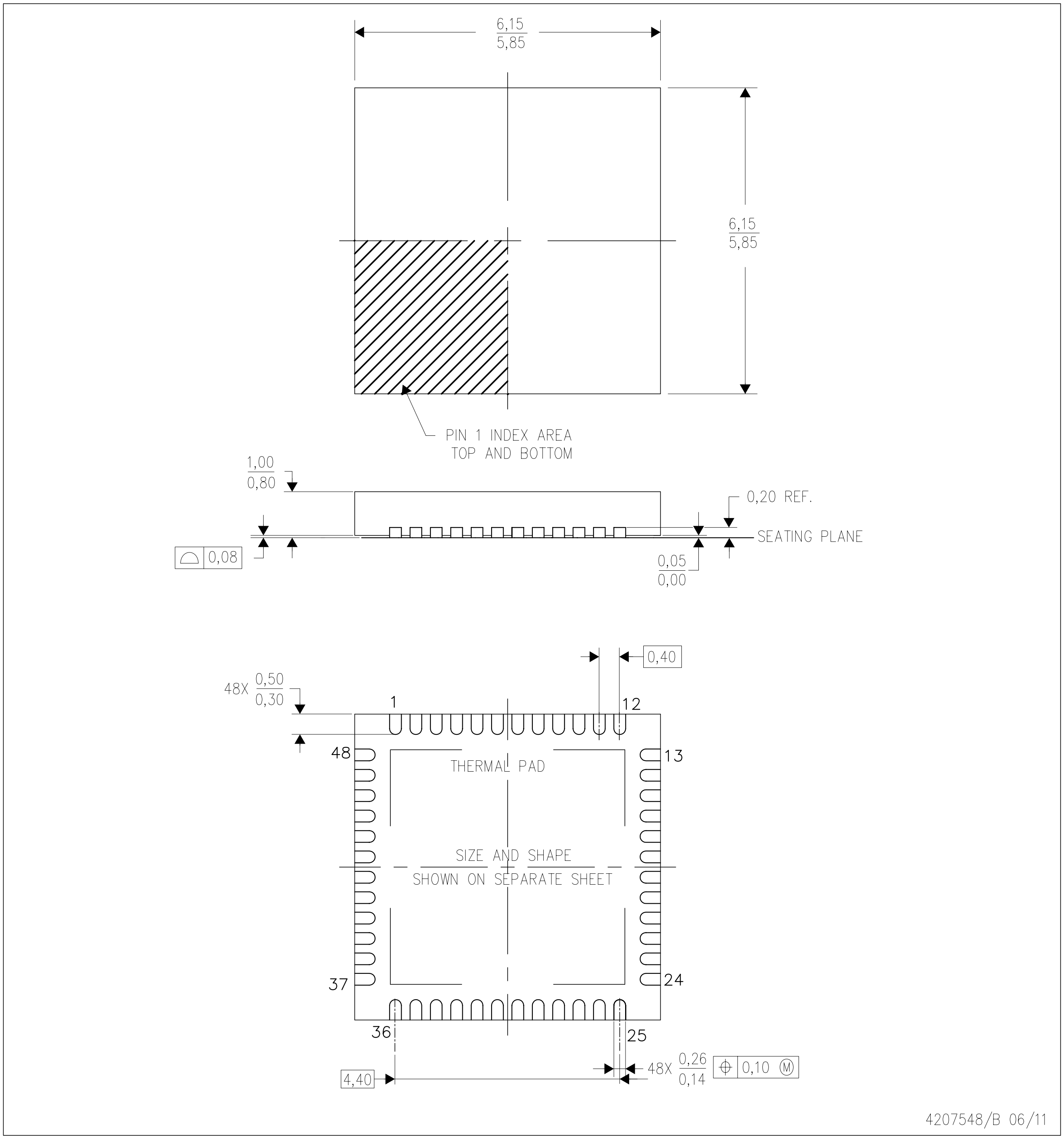
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65217ARSLR	VQFN	RSL	48	2500	367.0	367.0	38.0
TPS65217ARSLT	VQFN	RSL	48	250	210.0	185.0	35.0
TPS65217BRSLR	VQFN	RSL	48	2500	367.0	367.0	38.0
TPS65217BRSLT	VQFN	RSL	48	250	210.0	185.0	35.0
TPS65217CRSLR	VQFN	RSL	48	2500	367.0	367.0	38.0
TPS65217CRSLT	VQFN	RSL	48	250	210.0	185.0	35.0
TPS65217DRSLR	VQFN	RSL	48	2500	367.0	367.0	38.0
TPS65217DRSLT	VQFN	RSL	48	250	210.0	185.0	35.0

RSL (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

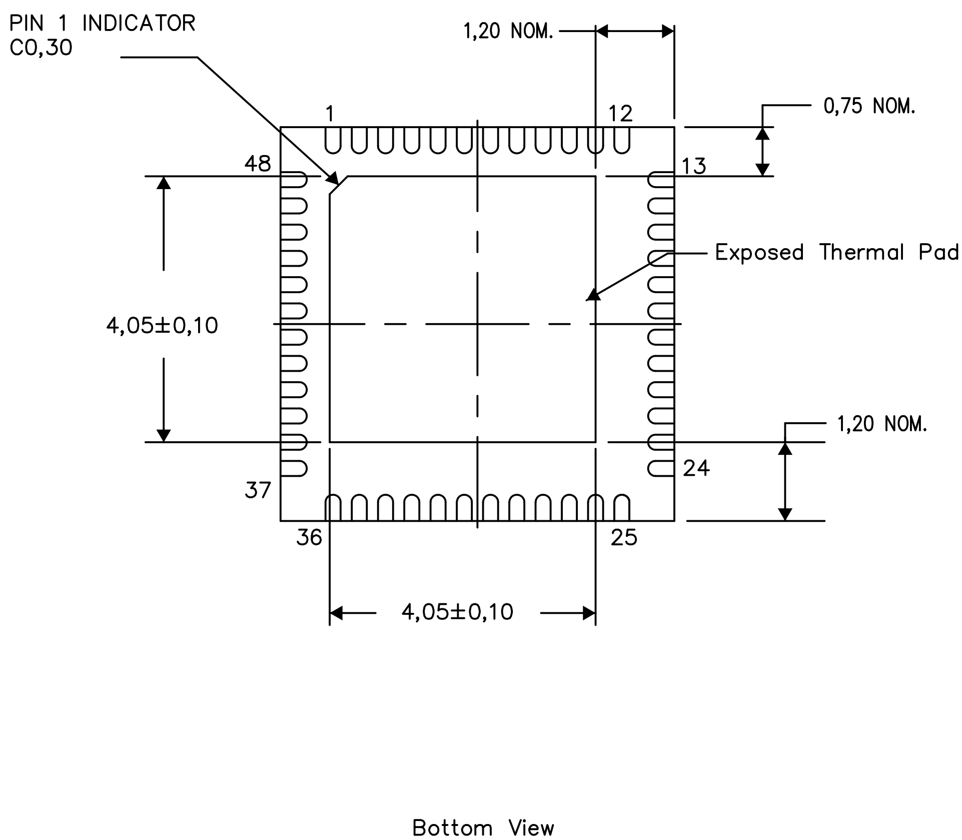
RSL (S-PVQFN-N48) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

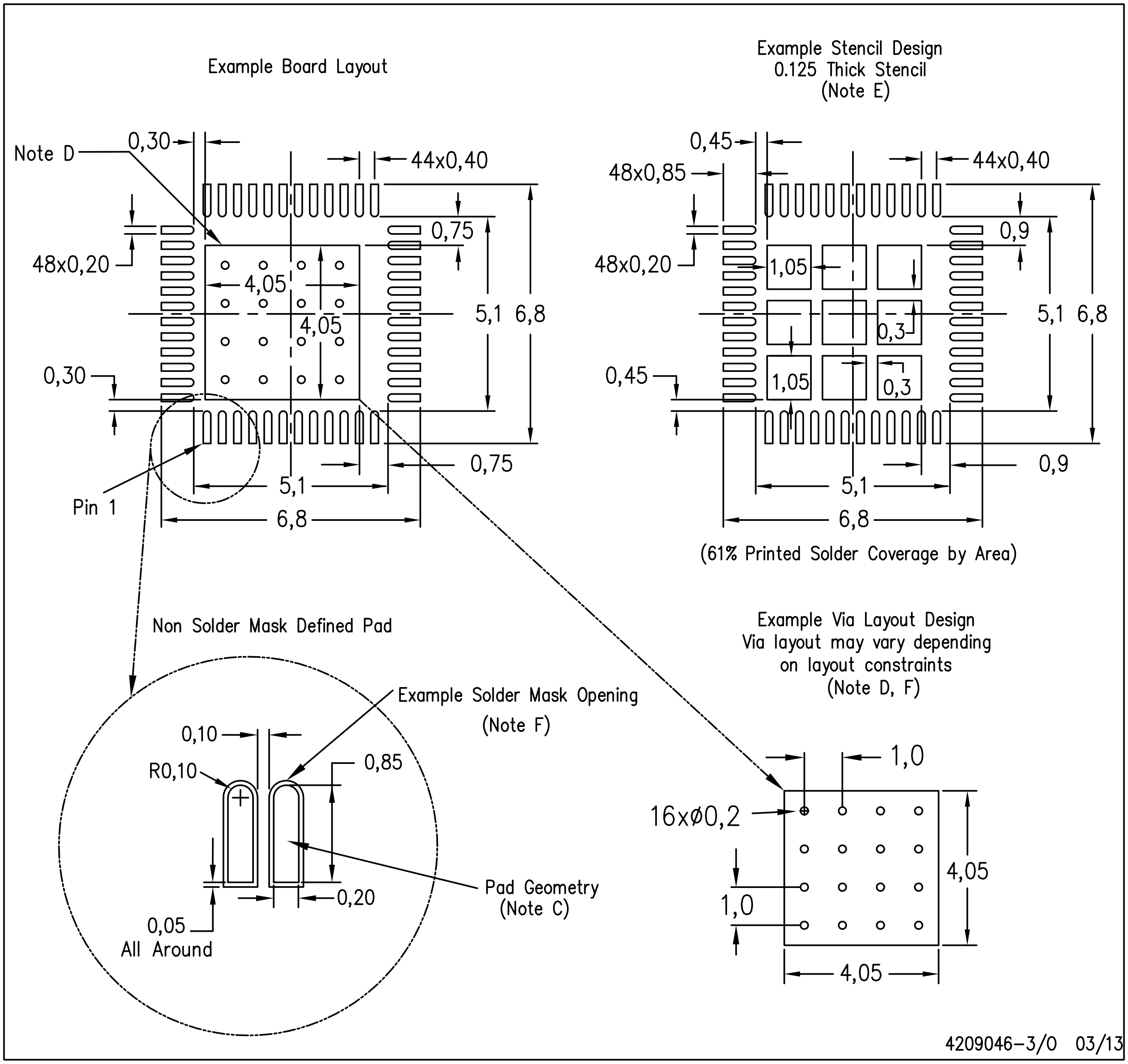


Exposed Thermal Pad Dimensions

4207841-4/P 03/13

NOTE: All linear dimensions are in millimeters

RSL (S-PVQFN-N48) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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