Integrated MCU Power Solution for C2000™ Microcontrollers

Check for Samples: TPS75005

FEATURES

- **Optimized to Supply TI's C2000 MCU Series: F2833x (DELFINO™), F2823x, F281x, and F280x/F2801x**
- **Dual 500-mA Voltage Regulators with Dedicated Supply Voltage Supervisors (SVSs)**
- **One Auxiliary SVS**
- **LDO1 and SVS1 for 1.8 V/1.9 V (Selectable): ±5% Specified with PG**
- **LDO2 and SVS2 for 3.3 V: ±5% Specified with PG**
- **Input Voltage Range: 3.75 V to 6.5 V**
- **Independent Soft-Start for LDO1 and LDO2**
- **Preset Power-Up and Power-Down Sequencing for C2000 MCUs**
- **Supports C2000 MCU Transient with Two 10-µF Ceramic Output Capacitors**
- **5-mm × 5-mm QFN Package** (1)

APPLICATIONS

- **C2000 MCUs**
- **DSPs/FPGAs/ASICs**

(1) 16-Pin HTSSOP package can be supported but minimum quantity may be required; contact sales representative.

DESCRIPTION

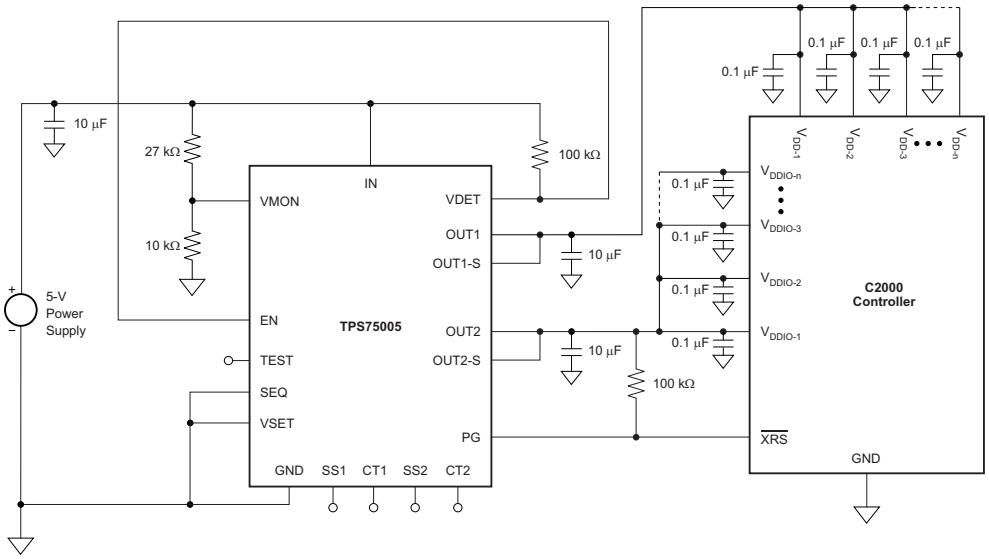
The TPS75005 is a complete power management solution for Texas Instruments' C2000 real-time microcontrollers and other DSP, FPGA, and ASIC MCUs. The device has been tested with and meets TI's F2833x (DELFINO), F2823x, F281x, and F280x/F2801x power requirements.

All of these C2000 controllers require ±5% power-rail accuracy. With the combination of high-accuracy, low-dropout regulators (LDOs) and dedicated SVSs, the device allows for a ±5% power supply to the C2000 with a power-good (PG) signal. (For more details, see Application Report SBVA032, *LDO+SVS Combined Accuracy*.)

Two power outputs are controlled by an integrated sequencer circuit. A single EN logic input signal makes sure that the power-up and power-down requirements of the C2000 controllers are met. The sequencer includes a soft-start for both LDOs to avoid inrush current. A third rail monitor is provided for general-purpose monitoring (for example, to monitor input voltage).

A quick-start guide (SBVA030) is available with step-by-step instructions for connection to a C2000 controller.

The TPS75005 is available in a 5-mm × 5-mm QFN package, yielding a compact total solution size with high power dissipation capability.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

VOLTAGE INFORMATION(1)

PRODUCT	V_{OUT1}		V_{OUT2}	V_{SVS1}		V_{SVS2}	V_{SVS3}
TPS75005(2)	VSET = L	VSET = H	3.333 V (101%)	VSET = H	VSET = L	3.234 (98%)	1.206 V
	1.818 V (101%)	1.919 V (101%)		1.764 V (98%)	1.862 V (98%)		
TPS75005ADJ	Adjustable, greater than 1.24 V		Adjustable, greater than 1.24 V	Adjustable, 97% of VOUT1		Adjustable, 97% of VOUT2	

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.
(2) VOUT1 and VSVS1 are selectable by VSET pin logic with the TPS75005.

ABSOLUTE MAXIMUM RATINGS(1)

At T_J = –40°C to +125°C (unless otherwise noted).

		VALUE		UNIT
		MIN	MAX	
Voltage(2)	IN, OUT1, OUT2, VMON, VSET, SEQ, OUT1_S, OUT2_S	–0.3	+7.0	V
	CT1 CT2, SS1, SS2	–0.3	+3.6	V
	EN, VDET, PG, TEST	–0.3	V_{IN} + 0.3(3)	V
Output current		Internally limited(4)		
Temperature	Storage, T_{stg}	–55	+150	°C
Electrostatic discharge ratings(5)	Human body model (HBM) QSS 009-105 (JESD22-A114A)		2	kV
	Charge device model (CDM) QSS 009-147 (JESD22-C101B.01)		500	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground terminal.
(3) Absolute maximum rating of these pins is V_{IN} + 0.3 V or + 7.0 V, whichever is smaller.
(4) See Electrical Characteristics.
(5) ESD testing is performed according to the respective JESD22 JEDEC standard.

THERMAL INFORMATION

THERMAL METRIC(1)(2)		TPS75005 RGW (QFN)(3) 20 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(4)	35.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(5)	31.9	
θ_{JB}	Junction-to-board thermal resistance(6)	14.4	
ψ_{JT}	Junction-to-top characterization parameter(7)	0.4	
ψ_{JB}	Junction-to-board characterization parameter(8)	14.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(9)	3.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953A.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.
(3) Thermal data for the RGW package is derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:
  (a) RGW: The exposed pad is connected to the PCB ground layer through a 4 x 4 thermal via array.
  (b) Each of top and bottom copper layers has a dedicated pattern for 4% copper coverage.
  (c) These data were generated with only a single device at the center of a JEDEC high-K (2s2p) board with 3in × 3in copper area. To understand the effects of the copper area on thermal performance, refer to the *Power Dissipation* and *Estimating Junction Temperature* sections.
(4) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(5) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the top of the package. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(6) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(7) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain θ_{JA} using a procedure described in JESD51-2a (sections 6 and 7).
(8) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain θ_{JA} using a procedure described in JESD51-2a (sections 6 and 7).
(9) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ELECTRICAL CHARACTERISTICS

Over operating temperature range of T_J = –40 °C to +125 °C, with 4.0 V ≤ V_{IN} ≤ 6.5 V, V_{OUT1_S} = V_{OUT1}, V_{OUT2_S} = V_{OUT2}, V_{EN} = V_{IN}, CT1 = OPEN, CT2 = OPEN, SS1 = OPEN, SS2 = OPEN, PG = pulled up to V_{OUT2} through 100-kΩ resistor, TEST = pulled up to V_{OUT2} through 100-kΩ resistor, V_{DET} = pulled up to V_{IN} through 100-kΩ resistor, V_{MON} = V_{IN}, C_{OUT1} = 10 µF, C_{OUT2} = 10 µF, R_{OUT1} = 1 kΩ to GND(1), R_{OUT2} = 1 kΩ to GND(1), and V_{SET} = SEQ = GND, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
COMPLETE DEVICE						
V_{IN}	Input voltage range		3.75		6.5	V
I_{GND}	GND current	I_{OUT1} = I_{OUT2} = 500 mA, V_{SET} = V_{IN} or GND			500	µA
I_Q	Quiescent GND current	I_{OUT1} = I_{OUT2} = 0 A, V_{SET} = V_{IN} or GND		175		µA
I_{SHDN}	Shutdown ground current	V_{IN} = 6.5 V, no pull-up resistors at PG, VDET, TEST pins		17	40	µA
V_{SVS3}	VMON supervisor threshold		1.181	1.206	1.230	V
ΔV_{SVS3}	VMON supervisor hysteresis	Relative to V_{SVS3}		+ 4		mV
V_{IH}	High-level input voltage	For EN, SEQ, and VSET pins	2.0			V
V_{IL}	Low-level input voltage	For EN, SEQ, and VSET pins	0		0.8	V
I_{IN}	Logic input current	For SEQ and VSET pins, V_{SEQ} = V_{SET} = 2.0 V	– 0.1		0.1	µA
		For EN pin	– 0.2		0.2	
V_{OL}	Low-level output voltage	Load current 1 mA into PG, TEST, and VDET pins force V_{OUT1} < V_{SVS1}, V_{MON} = 0.5 V			0.3	V
UVLO	Undervoltage lock out	Releasing: V_{IN} rising	3.4		3.75	V
		Locking: hysteresis, V_{IN} falling		60		mV
T_{TSD}	Thermal shutdown temperature	Temperature rising to shutdown		+165		°C
		Hysteresis, temperature falling to release shutdown		+145		°C
t_{DVS}	VSET transition time(2)			40		µs
LDO1 (1.8 V or 1.9 V Selectable by VSET Pin)						
V_{OUT1}	LDO1 output voltage accuracy	V_{SET}= H, 4.0 V ≤ V_{IN} ≤ 6.5 V, 1 mA ≤ I_{OUT1} ≤ 500 mA	1.881 (99%)	1.919 (101%)	1.957 (103%)	V
		V_{SET}= L, 4.0 V ≤ V_{IN} ≤ 6.5 V, 1 mA ≤ I_{OUT1} ≤ 500 mA	1.782 (99%)	1.818 (101%)	1.854 (103%)	V
$\Delta V_{OUT1}/\Delta V_{IN}$	LDO1 line regulation	4.0 V ≤ V_{IN} ≤ 6.5 V, I_{OUT1} = 1 mA			122	µV/V
$\Delta V_{OUT1}/\Delta I_{OUT1}$	LDO1 load regulation	1 mA ≤ I_{OUT1} ≤ 500 mA			29	µV/mA
I_{CL1}	LDO1 current limit	V_{OUT1} = 0.9 × $V_{OUT1(NOM)}$, 4.5 V < V_{IN} < 6.5 V		900		mA
V_{SVS1}	LDO1 supervisor threshold	V_{SET}= H, 4.0 V ≤ V_{IN} ≤ 6.5 V Force V_{OUT1} (decreasing)	1.805 (95%)		1.881 (99%)	V
		V_{SET}= L, 4.0 V ≤ V_{IN} ≤ 6.5 V Force V_{OUT1} (decreasing)	1.710 (95%)		1.782 (99%)	V
ΔV_{SVS1}	LDO1 supervisor hysteresis	Relative to V_{SVS1}		0.3		%
$t_{W(SVS1)}$	LDO1 supervisor minimum pulse width to Sense	V_{OUT1} = 100% → 90% → 100%		3.3		µs
$t_{D(SVS1)}$	LDO1 supervisor delay time	From (V_{OUT1} > V_{SVS1}) event to PG ↑ with SEQ = H, C_{CT1} = (open)		33		µs
I_{CT1}	CT1 charging current	Any capacitor connected between CT1 and GND, 0.2 V ≤ V_{CT1} ≤ 1.0 V	0.3		1	µA
V_{CT1}	CT1 timeout threshold	Any capacitor connected between CT1 and GND	1.05	1.206	1.35	V
t_{SS1}	LDO1 soft-start time	V_{OUT1} waveform from 0% to 95%, C_{SS1} = (open)		260		µs
I_{SS1}	SS1 charging current	Any capacitor connected between SS1 and GND, 0.2 V ≤ V_{SS1} ≤ 1.0 V	0.3		0.8	µA
R_{PD1}	LDO1 active pull-down ON resistance	EN = GND, V_{OUT1} = 1.8 V	225	360	475	Ω
V_{DOWN1}	LDO1 power-down detector accuracy			0.3		V

(1) These 1-kΩ resistors are disconnected when the test conditions specify an output current of LDO1 or LDO2.
(2) With recommended usage of TPS75005, VSET does not need to be controlled on-the-fly. VSET transition time varies significantly depending on application conditions. Stated typical value is almost the fastest transition.

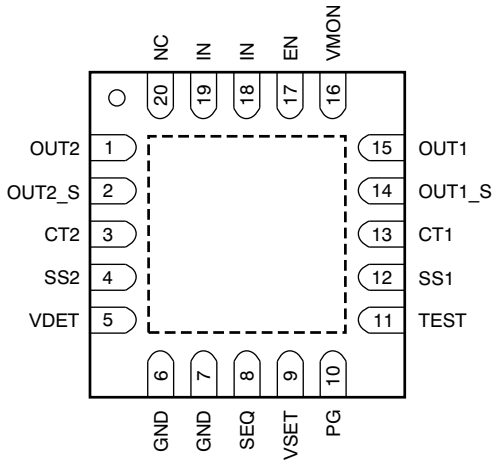
ELECTRICAL CHARACTERISTICS (continued)

Over operating temperature range of T_J = –40 °C to +125 °C, with 4.0 V ≤ V_{IN} ≤ 6.5 V, V_{OUT1_S} = V_{OUT1}, V_{OUT2_S} = V_{OUT2}, V_{EN} = V_{IN}, CT1 = OPEN, CT2 = OPEN, SS1 = OPEN, SS2 = OPEN, PG = pulled up to V_{OUT2} through 100-kΩ resistor, TEST = pulled up to V_{OUT2} through 100-kΩ resistor, V_{DET} = pulled up to V_{IN} through 100-kΩ resistor, V_{MON} = V_{IN}, C_{OUT1} = 10 µF, C_{OUT2} = 10 µF, R_{OUT1} = 1 kΩ to GND(1), R_{OUT2} = 1 kΩ to GND(1), and V_{SET} = SEQ = GND, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LDO2 (3.3 V)						
V_{OUT2}	LDO2 output voltage accuracy	4.0 V ≤ V_{IN} ≤ 6.5 V, 1mA ≤ I_{OUT2} ≤ 500 mA	3.267 (99%)	3.333 (101%)	3.399 (103%)	V
$\Delta V_{OUT2}/\Delta V_{IN}$	LDO2 line regulation	4.0 V ≤ V_{IN} ≤ 6.5 V, I_{OUT2} = 1 mA			461	µV/V
$\Delta V_{OUT2}/\Delta I_{OUT1}$	LDO2 load regulation	1 mA ≤ I_{OUT2} ≤ 500 mA			50	µV/mA
I_{CL2}	LDO2 current limit	V_{OUT2} = 0.9 × $V_{OUT2(NOM)}$, 4.5 V < V_{IN} < 6.5 V		900		mA
V_{SVS2}	LDO2 supervisor threshold	4.0 V ≤ V_{IN} ≤ 6.5 V force V_{OUT2} (decreasing)	3.135 (95%)		3.267 (99%)	V
ΔV_{SVS2}	LDO2 supervisor hysteresis	Relative to V_{SVS2}		0.3		%
$t_{W(SVS2)}$	LDO2 supervisor minimum pulse width to sense	V_{OUT2} = 100% → 90% → 100%		3.3		µs
$t_{D(SVS2)}$	LDO2 supervisor delay time	From (V_{OUT2} > V_{SVS2}) event to PG↑ with SEQ = L, C_{CT2} = (open)		33		µs
I_{CT2}	CT2 charging current	Any capacitor connected between CT2 and GND, 0.2 V ≤ V_{CT2} ≤ 1.0 V	0.3		1	µA
V_{CT2}	CT2 timeout threshold	Any capacitor connected between CT2 and GND	1.05	1.206	1.35	V
t_{SS2}	LDO2 soft-start time	V_{OUT2} waveform from 0% to 95%, C_{SS2} = (open)		260		µs
I_{SS2}	SS2 charging current	Any capacitor connected between SS2 and GND, 0.2 V ≤ V_{SS2} ≤ 1.0 V	0.3		0.8	µA
R_{PD2}	LDO2 active pull-down ON resistance	EN = L, V_{OUT2} = 3.3 V	225	360	475	Ω
V_{DOWN2}	LDO2 power-down detector accuracy			0.3		V

PIN CONFIGURATION

RGW PACKAGE
5-mm x 5-mm QFN-20
(TOP VIEW)



PIN DESCRIPTIONS

PIN		DESCRIPTION
NAME	RGW QFN-20	
CT1	13	SVS1 internal-power-good delay setting. Leave this pin open for the default delay setting or connect capacitor between this node and GND to program the delay. **Do not connect a regular oscilloscope probe for monitoring.**
CT2	3	SVS2 internal-power-good delay setting. Leave this pin open for the default delay setting or connect a capacitor between this pin and GND to program the delay. **Do not connect a regular oscilloscope probe for monitoring.**
EN	17	Enable inputs. Logic-H input to this pin triggers power-up sequence. Logic-L triggers power-down sequence. NOTE: The sequencing logic will automatically prevent powering up until the TPS75005 pulls the output rails to GND. This ensures a proper startup every time.
GND	6, 7	Ground. Tie these pins to the thermal pad and maximize the copper in this area for optimal performance.
IN	18, 19	Power supply to the device. Connect a 10-µF X5R or X7R dielectric capacitor between IN and GND close to the device.
NC	20	Not internally connected. This pin can be either tied to IN or GND to simplify layout.
OUT1	15	LDO1 output voltage. Connect a 10-µF X5R or X7R capacitor between this pin and ground close to the device.
OUT1_S	14	LDO1 output voltage sense input. Connect directly to output capacitor close to pin 15.
OUT2	1	LDO2 output voltage. Connect a 10-µF X5R or X7R capacitor between this pin and ground close to the device.
OUT2_S	2	LDO2 output voltage sense input. Connect directly to output capacitor close to pin 1.
PG	10	Power-Good output. This is an open-drain output terminal and a pull-up resistor is required. The typical connection is 100 kΩ to OUT2. When $V_{OUT1} > V_{SVS1}$ and $V_{OUT2} > V_{SVS2}$, this pin outputs logic-H.
SEQ	8	Sequence select pin. Logic-L input to this pin powers-up two LDOs in this order: LDO1 first, and then LDO2. Logic-L also powers-down LDO2 first, and then LDO1. Logic-H to this pin powers-up two LDOs in this order: LDO2 first, and then LDO1. Logic-H also powers-down LDO1 first, and then LDO2. SEQ should be hard-wired to either IN or GND depending on the sequencing mode required.
SS1	12	LDO1 soft-start setting. Leave this pin open for the default ramp up setting or connect a capacitor, 10 nF or less, between this pin and GND to program V_{OUT1} ramp-up slew rate. **Do not connect a regular oscilloscope probe for monitoring.**
SS2	4	LDO2 soft-start setting. Leave this pin open for the default ramp up setting or connect a capacitor between this pin and GND to program V_{OUT2} ramp-up slew rate. **Do not connect a regular oscilloscope probe for monitoring.**
TEST	11	Test pin for test and debugging purposes only. Do not connect this pin.
VDET	5	Output of SVS3. This is an open-drain output terminal and a pull-up resistor is required. The typical connection is 100 kΩ to IN. When $V_{MON} > V_{SVS3}$, VDET outputs logic-H; when $V_{MON} < V_{SVS3}$, VDET is logic-L.
VMON	16	Monitor input voltage of third voltage detector. A resistor divider on this pin between the voltage rail to be monitored and GND sets the threshold voltage. The detect threshold is 1.206 V.
VSET	9	LDO1 output voltage setting. Logic-H input sets V_{OUT1} to 1.9 V. Logic-L sets V_{OUT1} to 1.8 V. It is recommended to tie this pin either to IN or GND depending on voltage required for the application.
Thermal pad		Pad for thermal dissipation. Tie this pin to GND with vias through the board to internal heat spreading layers as well as the back side of the PCB.

FUNCTIONAL BLOCK DIAGRAM

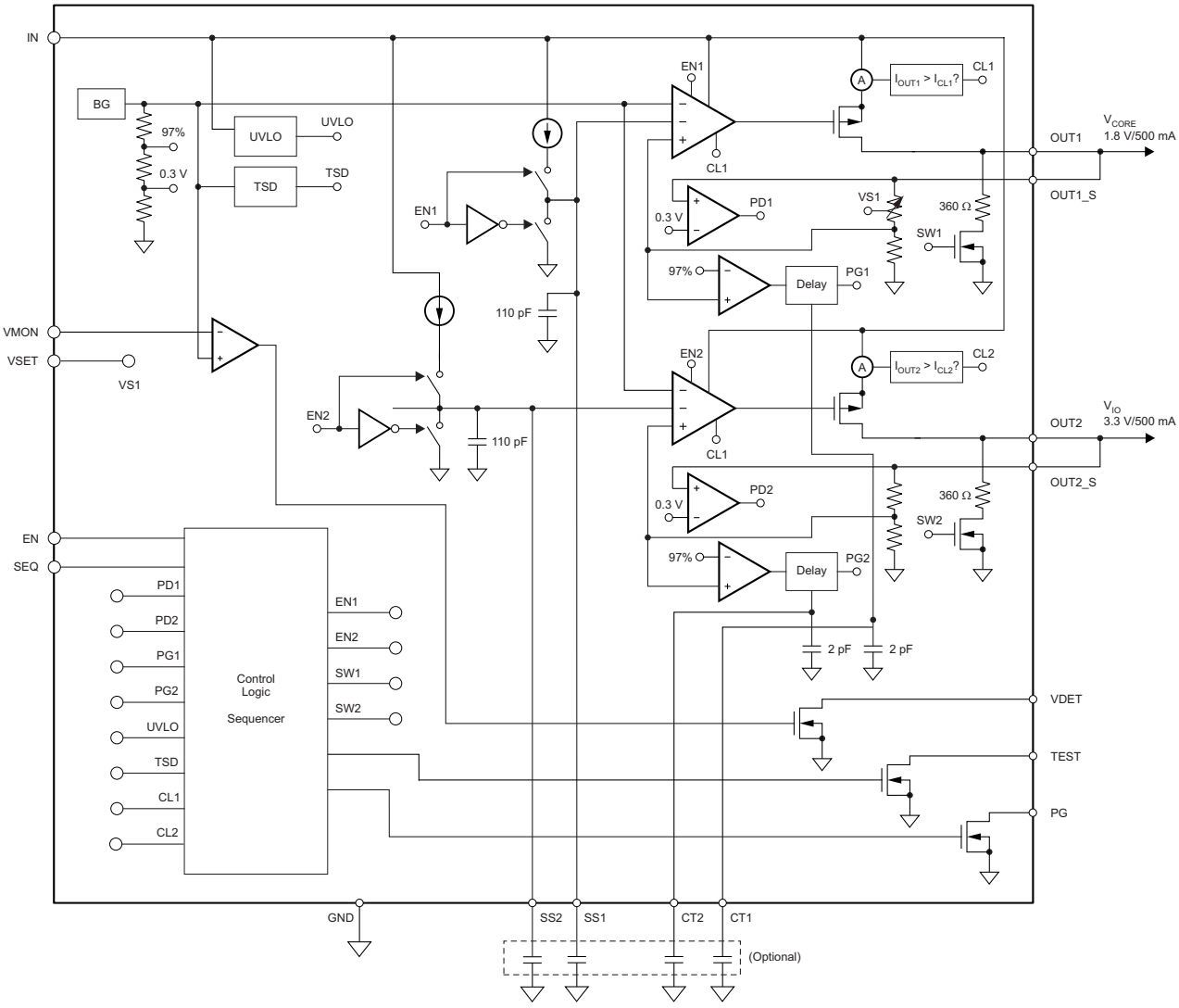


Figure 1. Functional Block Diagram

TYPICAL CHARACTERISTICS

At T_J = +25°C, V_{IN} = 5 V, $V_{(EN)} = V_{IN}$, C_{IN} = 22 µF, $C_{OUT1} = C_{OUT2}$ = 10 µF, $C_{(SS1)} = C_{(SS2)} = C_{(CT1)} = C_{(CT2)}$ = (open), V_{SET} = 0 V, $V_{SNS1} = V_{OUT1}$, $V_{SNS2} = V_{OUT2}$, PG pin pulled up to V_{OUT2} with 100-kΩ pull-up resistor, and VDET pin pulled up to VIN with 100-kΩ pull-up resistor, unless otherwise noted.

LDO1 (OUTPUT AND SVS THRESHOLD) VOLTAGE vs TEMPERATURE

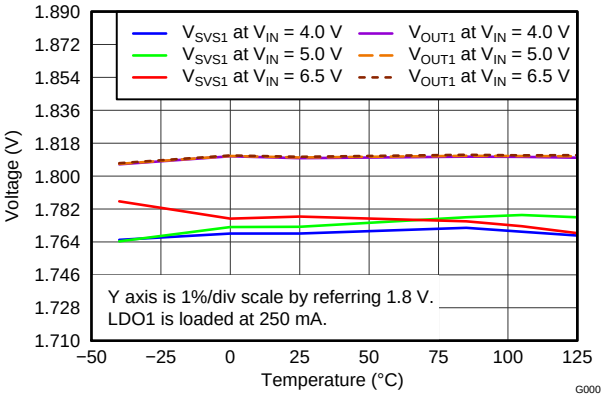


Figure 2.

LDO2 (OUTPUT AND SVS THRESHOLD) VOLTAGE vs TEMPERATURE

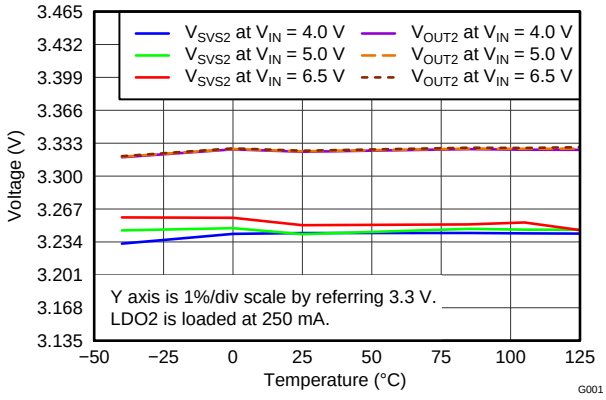


Figure 3.

LDO1 LOAD REGULATION

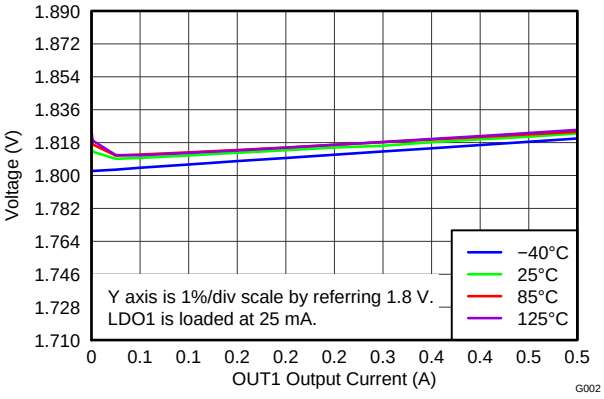


Figure 4.

LDO2 LOAD REGULATION

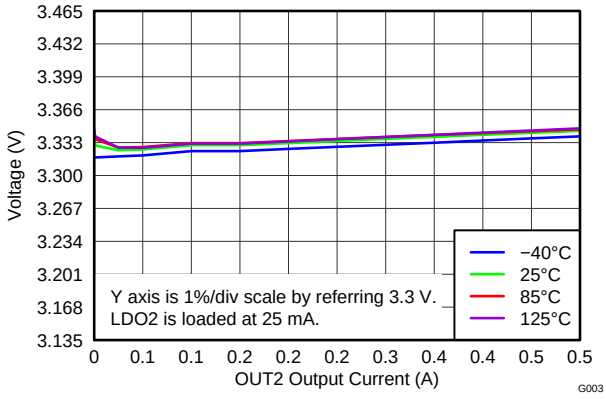


Figure 5.

SHUTDOWN GROUND CURRENT vs TEMPERATURE

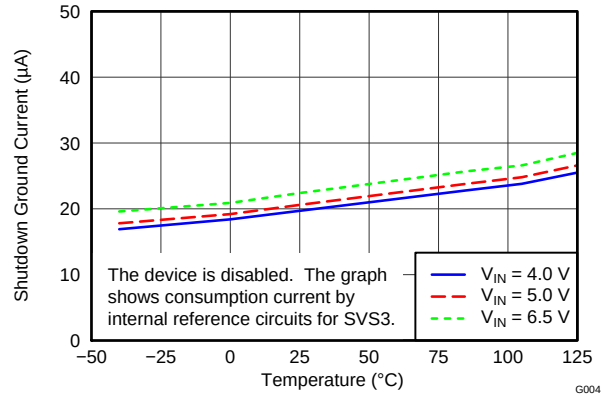


Figure 6.

QUIESCENT GROUND CURRENT vs TEMPERATURE

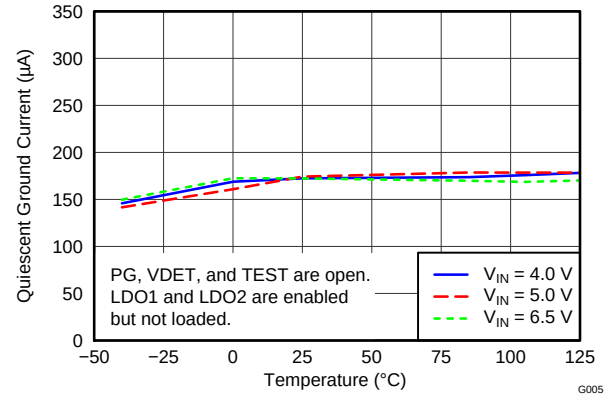


Figure 7.

TYPICAL CHARACTERISTICS (continued)

At T_J = +25°C, V_{IN} = 5 V, $V_{(EN)} = V_{IN}$, C_{IN} = 22 µF, $C_{OUT1} = C_{OUT2}$ = 10 µF, $C_{(SS1)} = C_{(SS2)} = C_{(CT1)} = C_{(CT2)}$ = (open), V_{SET} = 0 V, $V_{SNS1} = V_{OUT1}$, $V_{SNS2} = V_{OUT2}$, PG pin pulled up to V_{OUT2} with 100-kΩ pull-up resistor, and VDET pin pulled up to VIN with 100-kΩ pull-up resistor, unless otherwise noted.

LOADED GROUND CURRENT vs I_{OUT1}

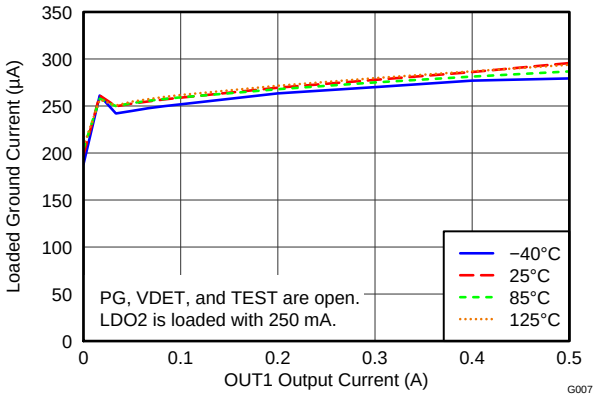


Figure 8.

LOADED GROUND CURRENT vs I_{OUT2}

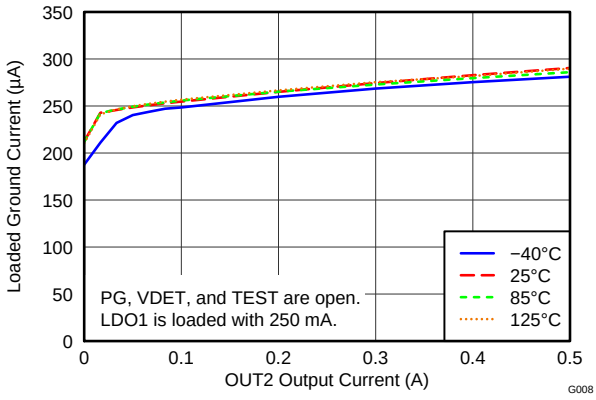


Figure 9.

LOADED GROUND CURRENT vs TEMPERATURE

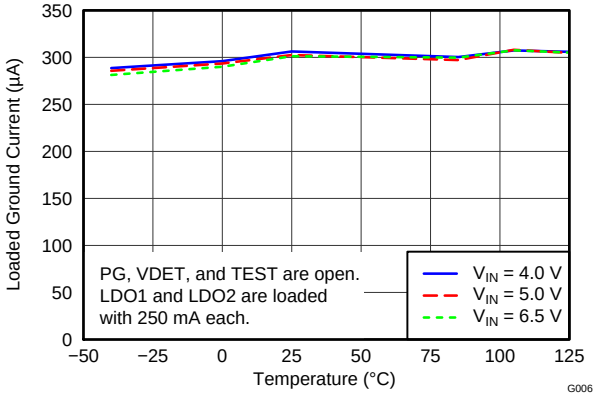


Figure 10.

UVLO VOLTAGE vs TEMPERATURE

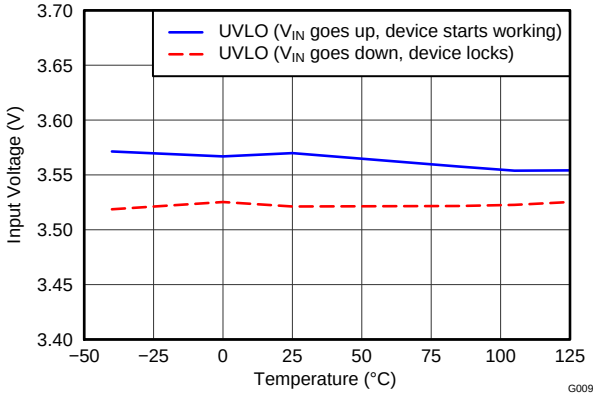


Figure 11.

LDO1 CURRENT LIMIT vs TEMPERATURE

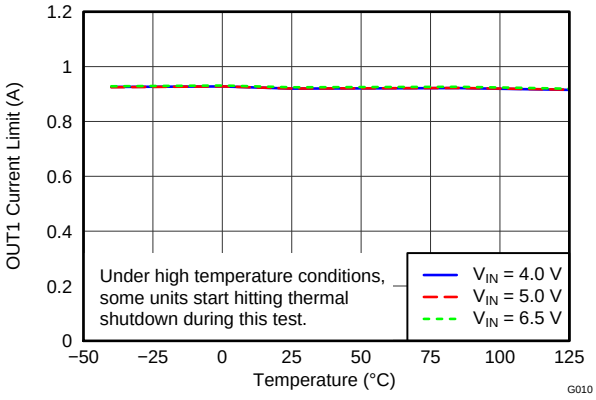


Figure 12.

LDO2 CURRENT LIMIT vs TEMPERATURE

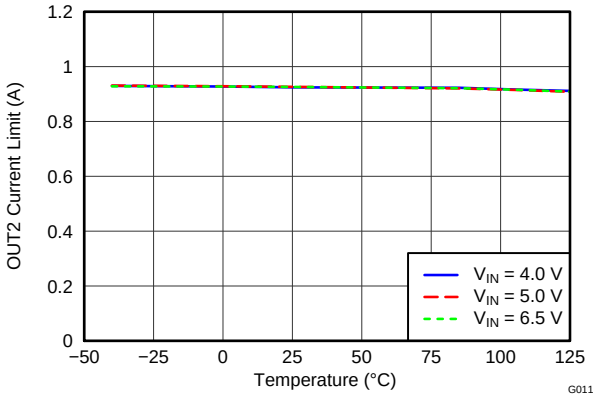


Figure 13.

TYPICAL CHARACTERISTICS (continued)

At T_J = +25°C, V_{IN} = 5 V, $V_{(EN)} = V_{IN}$, C_{IN} = 22 µF, $C_{OUT1} = C_{OUT2}$ = 10 µF, $C_{(SS1)} = C_{(SS2)} = C_{(CT1)} = C_{(CT2)}$ = (open), V_{SET} = 0 V, $V_{SNS1} = V_{OUT1}$, $V_{SNS2} = V_{OUT2}$, PG pin pulled up to V_{OUT2} with 100-kΩ pull-up resistor, and VDET pin pulled up to VIN with 100-kΩ pull-up resistor, unless otherwise noted.

EN PIN THRESHOLD vs TEMPERATURE

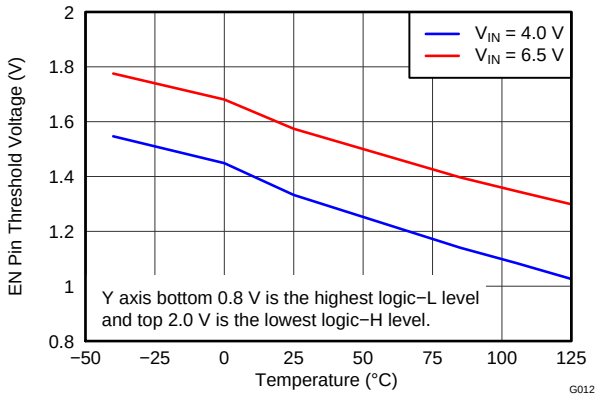


Figure 14.

SVS3 (VMON) THRESHOLD vs TEMPERATURE

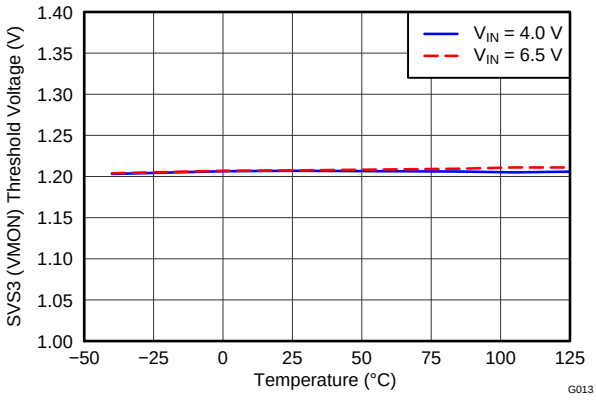


Figure 15.

LDO1 PULL DOWN RESISTANCE vs V_{OUT1}

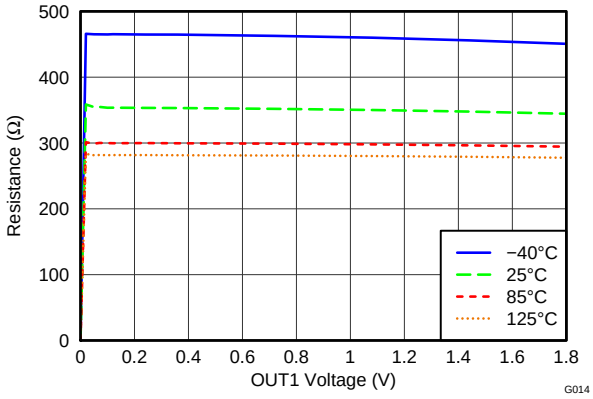


Figure 16.

LDO2 PULL DOWN RESISTANCE vs V_{OUT2}

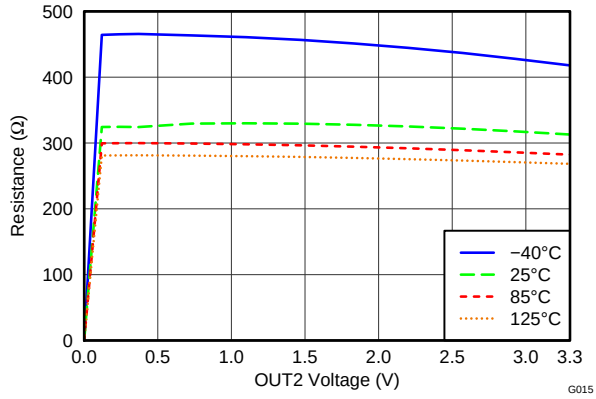


Figure 17.

OPEN DRAIN OUTPUT (PG and VDET) DRIVE CAPABILITY vs TEMPERATURE

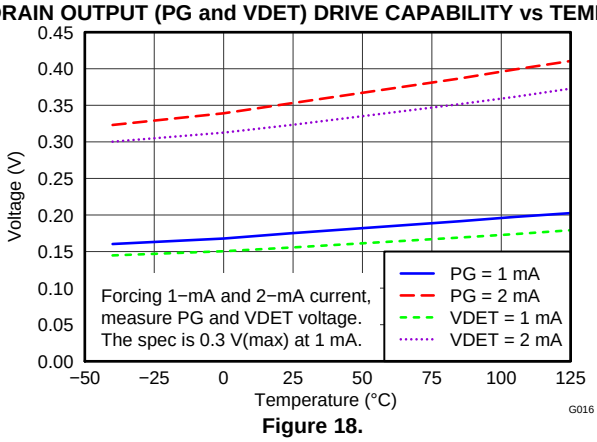


Figure 18.

TYPICAL CHARACTERISTICS (continued)

At T_J = +25°C, V_{IN} = 5 V, $V_{(EN)} = V_{IN}$, C_{IN} = 22 µF, $C_{OUT1} = C_{OUT2}$ = 10 µF, $C_{(SS1)} = C_{(SS2)} = C_{(CT1)} = C_{(CT2)}$ = (open), V_{SET} = 0 V, $V_{SNS1} = V_{OUT1}$, $V_{SNS2} = V_{OUT2}$, PG pin pulled up to V_{OUT2} with 100-kΩ pull-up resistor, and VDET pin pulled up to VIN with 100-kΩ pull-up resistor, unless otherwise noted.

LINE TRANSIENT RESPONSE

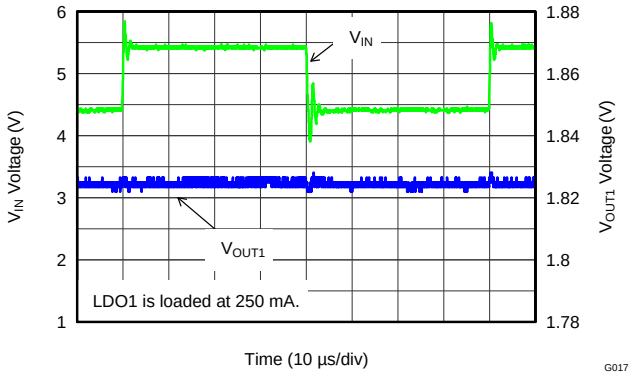


Figure 19.

LINE TRANSIENT RESPONSE

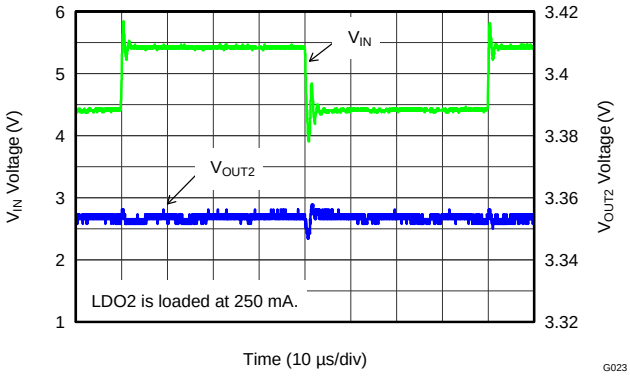


Figure 20.

LDO1 LOAD TRANSIENT RESPONSE

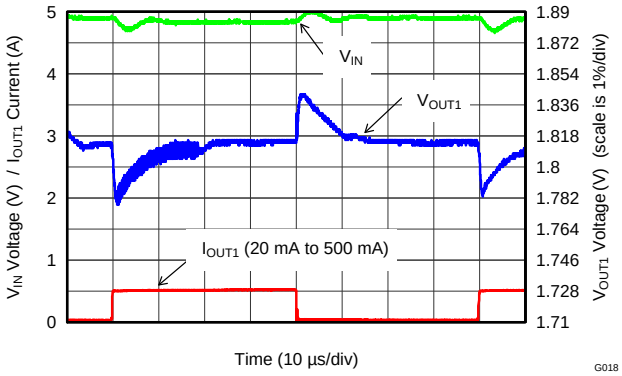


Figure 21.

LDO2 LOAD TRANSIENT RESPONSE

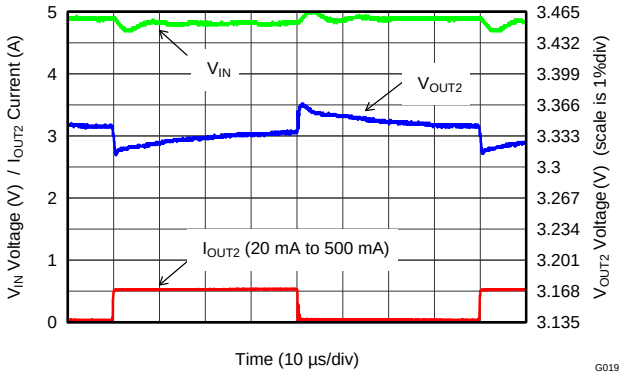


Figure 22.

V_{OUTX} RAMP-UP TIME vs C_{SSX}

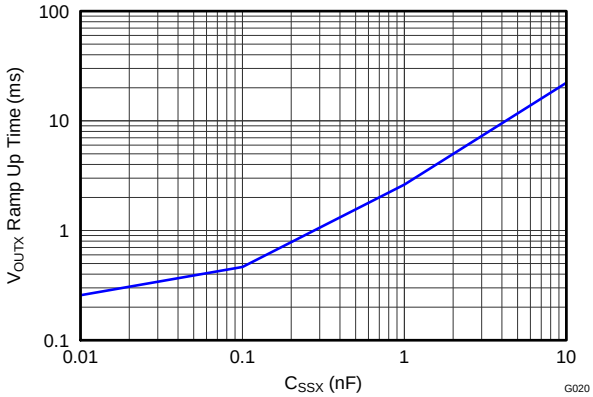


Figure 23.

DELAY TIME (TO NEXT SEQUENCER EVENT) vs C_{CTX}

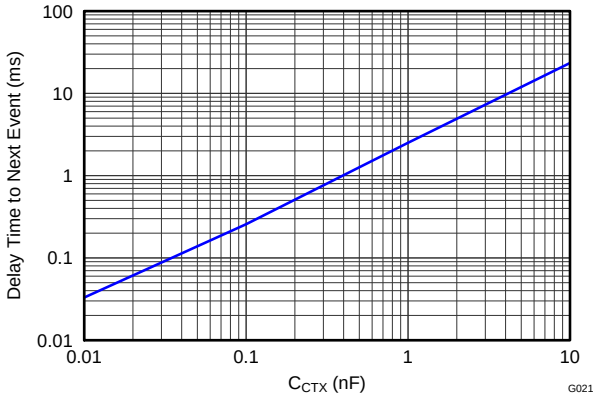


Figure 24.

APPLICATION INFORMATION

Design Guidelines

Figure 25 and Figure 26 show a basic schematic and PCB layout for applications using the internal default settings for power-good delay and rise time of the LDO1 and LDO2 outputs at turn on. This configuration is typical for applications involving the targeted C2000 microcontrollers. The unused adjustment pins, CT1, CT2, SS1, and SS2, are left open or floating. Connecting the SEQ and VSET pins to ground selects the turn-on sequence and the output voltage of LDO1. The open-drain outputs at PG and VDET are pulled up to the input voltage through 100-kΩ resistors. VDET is connected to enable the TPS75005 when the input voltage exceeds the SVS voltage set by resistor divider R1 and R2 to VMON. For highly dynamic loads, like that of the C2000 microcontroller, the input capacitor, C2, and the output capacitors, C3 and C8, are specified to be 10-µF, X5R or X7R, 10-V, ceramic capacitors in order to meet transient performance requirements.

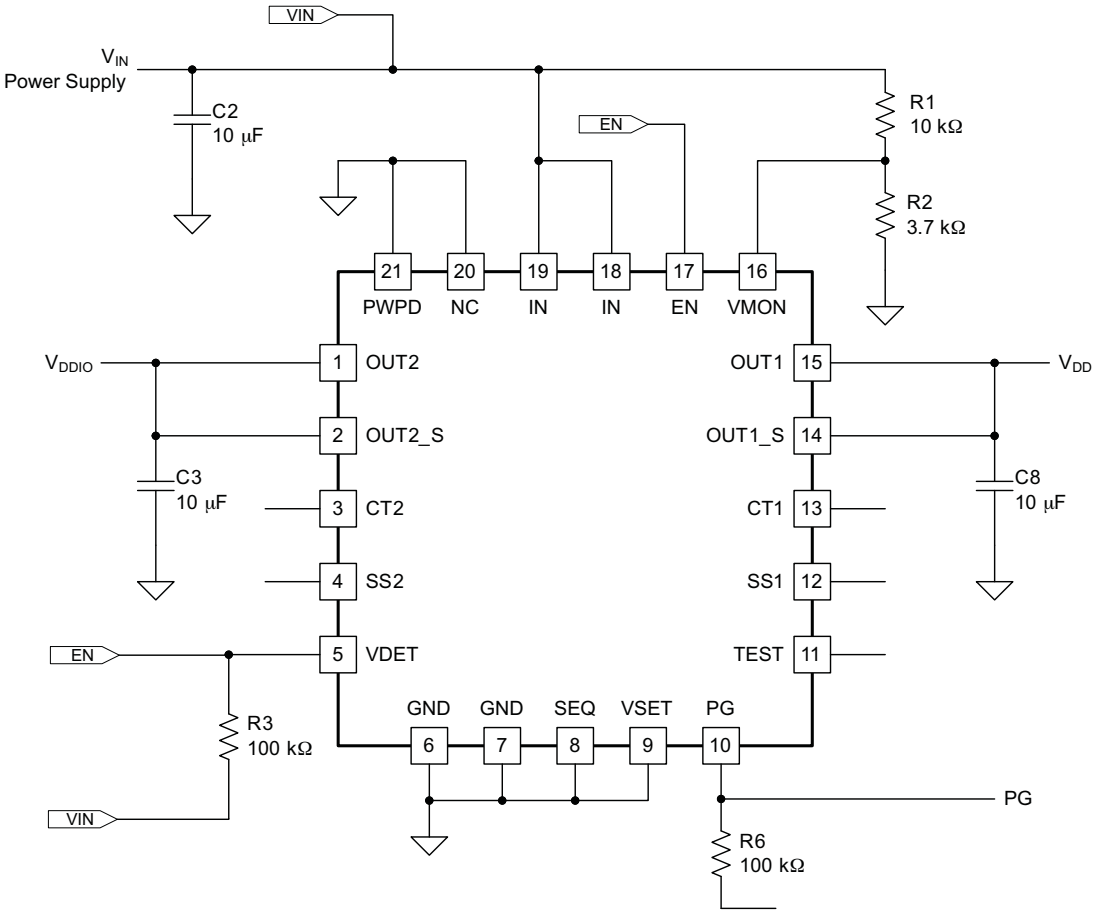


Figure 25. Configuration for F280x, F281x, F223x and F2833x Controllers (Set to automatically sequence C2000 when V_{IN} > 4.5 V) (C2, C3, C8 / 10-µF X5R ceramic capacitors)

The PCB layout of Figure 26 shows that the input and output capacitors C2, C3, and C8 are located near the respective pins and interconnected with a wide, low-inductance, ground plane that includes the device ground and the thermal pad ground of the device.

NOTE

The input capacitor ground is routed under the device package through NC, pin-20.

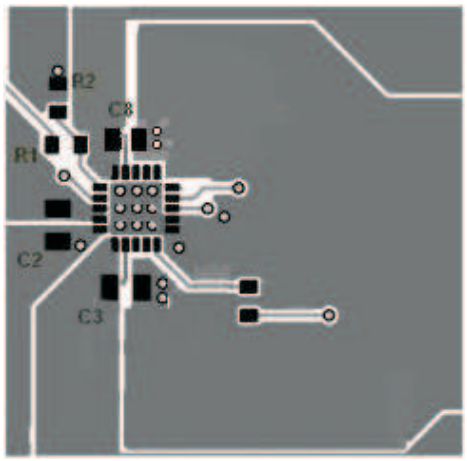


Figure 26. TPS75005EVM-023 Recommended Layout

The PCB typically consists of four layers, minimum. The top (surface) layer and one internal layer are used for trace/signal routing. One internal layer as well as the bottom layer are devoted to be ground planes that also function as *spreading* planes for dissipating heat away from the TPS75005 device. It is very important for proper function of the device and long-term reliability to conduct heat away from the device. The PowerPAD is soldered to a ground pad on the PCB that conducts heat away from the device through nine plated vias to the spreading planes beneath. The internal spreading layer in this case consists of four square inches of 1-ounce copper, and the bottom layer consists of an equal area of 2-ounce copper. Additional spreading layers should be added, if necessary, to a given application.

LDO BLOCKS

The TPS75005 integrates two high-bandwidth LDOs for powering the V_{DD} and V_{DDIO} pins of the C2000 controllers.

Input Capacitor

Although an input capacitor is not required for LDO stability, it is recommended to connect a 10-µF capacitor across the input supply near the device. In addition to input capacitor consideration, pay attention to the printed circuit board (PCB) design in order to reduce source impedance.

X5R- and X7R-type capacitors are highly recommended because they have minimal variation in value and ESR over temperature. Maximum ESR should be less than 1.0 Ω.

Output Capacitors

The TPS75005 is designed to be stable using standard ceramic capacitors with capacitance values 4.7 µF or greater. In order to meet C2000 transient requirements, a 10-µF output capacitor at each of OUT1 and OUT2 is recommended.

X5R- and X7R-type capacitors are highly recommended because they have minimal variation in value and ESR over temperature. Maximum ESR should be less than 1.0 Ω.

See the Sense Pins (OUT1_S AND OUT2_S) section for more details.

Sense Pins (OUT1_S AND OUT2_S)

The TPS75005 has output voltage sensing pins OUT1_S and OUT2_S. OUT1_S should be connected to OUT1 at the output capacitor of LDO1, and OUT2_S to OUT2 at the output capacitor of LDO2. Both output capacitors should be placed close to the device to minimize OUT1_S and OUT2_S trace. Figure 27 shows capacitor placement.

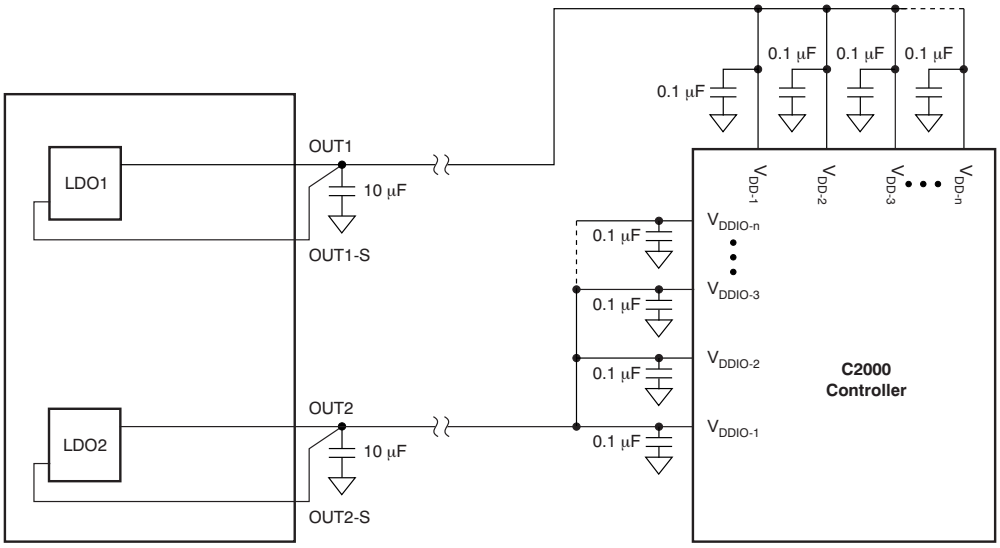


Figure 27. Output Capacitors Placement and Sense Pins

When the C2000 controller is placed far from the TPS75005 on a PCB, it is recommended to connect the output capacitors of OUT1 and OUT2 as close as possible to the TPS75005 device in order to route OUT1 and OUT2 node to a C2000 controller, and to place 0.1-µF ceramic capacitors for each of the V_{DD} and V_{DDIO} pins.

Soft-Start (SS1 and SS2)

The TPS75005 has a soft-start (or slow-start) function for LDO1 and LDO2 that work independently of one another. The ramp-up time for LDO1 and LDO2 is by default 260 µs due to the internal 110-pF capacitors. By connecting an external capacitor(s) at the SS1 and/or SS2 pins, the ramp-up time for the LDOs increases proportionately by following this equation:

$$t_{RAMPUP}\ (s) = \frac{C_{SSx}\ (F) + 110 \times 10^{-12}\ (F)}{0.5 \times 10^{-6}\ (A)} \times 1.2\ (V) \quad (1)$$

where:

t_{RAMPUP} = ramp up time

C_{SSx} = external capacitor value at SS1 or SS2 pin

See Figure 23 for an actual measurement curve.

To ensure that these circuits are discharged during power down, the capacitors used can have a maximum value of 10 nF approximately 24 ms of ramping time. When an application circuit must control a much larger timing period, use the supervisor delay setting in addition to the soft-start mechanism. See and find T_{SSx} and $T_{d(SVSx)}$ in Figure 32. See the Delay Setting (CT1 and CT2) section for details.

All supported C2000 controllers work well with the TPS75005 default setting (without external soft-start capacitors). In case a large number of output capacitors are connected for a specific application reason, it is recommended to connect capacitors at SS1 and/or SS2 so that inrush current (into the TPS75005) does not cause a large input voltage droop. This can be mitigated by increasing the bulk capacitance at V_{IN}.

NOTE

SS1 and SS2 are very high impedance nodes with very low values of constant current source. These two terminals cannot be monitored by regular oscilloscope probes. Connecting such regular probes to SS1 or SS2 changes the behavior of the soft-start function and no valid waveform can be monitored.

To monitor these terminals, use high-impedance probes, such as *active FET probes*.

Internal Enable Signals and Pull-Down Switches

As shown in Figure 1, LDO1 is controlled by the internal signal EN1, and LDO2 is controlled by EN2. SW1 and SW2 are the inverse signals of EN1 and EN2, respectively. Whenever LDO1 and LDO2 are disabled, that means EN1 and EN2 are logic-L, respectively. The corresponding output node(s) is discharged by an internal MOSFET and 360-Ω resistor controlled by SW1 and SW2.

These pull-down switches ensure that every power-down sequence is completed in a reasonable, finite time. See the Power-Down Monitoring section for a very important notice.

LDO1 Voltage Setting (VSET)

LDO1 can be configured as either a 1.8-V regulator or a 1.9-V regulator by the configuration of the VSET pin. When VSET is connected to ground, LDO1 outputs 1.8 V; when VSET is connected to the level of logic-H, LDO1 outputs 1.9 V.

Current Limit

The TPS75005 internal current limit helps protect the regulator during unexpected fault conditions. During current limit, the output sources a fixed 900mA. If kept in current limit for an extended period of time, the device will thermally shutdown.

MONITOR BLOCKS

Supply Voltage Supervisors (SVS1 and SVS2)

The TPS75005 integrates two supply voltage supervisors (SVSs) to monitor the V_{DD} and V_{DDIO} pins of the C2000 controllers.

Delay Setting (CT1 and CT2)

The TPS75005 has a programmable delay function for both SVS1 and SVS2 that work independently of each other. By default, both CT1 and CT2 are open, and both SVS1 and SVS2 take approximately 33 µs of delay time from the comparator trip event to its output. By connecting an external capacitor(s) at the CT1 and/or CT2 pins, the SVS delay time increases proportionately, as shown in the following equation:

$$t_d\ (s) = \frac{C_{SSx}\ (F)}{0.5 \times 10^{-6}\ (A)} \times 1.2\ (V) \quad (2)$$

where:

t_d = delay time

C_{CTx} = external capacitor value at CT1 or CT2 pin

See Figure 24 for an actual measurement curve.

For a long delay setting, use a very low leakage current capacitor such as X5R- or X7R-type to minimize calculation errors from the previous equation.

All supported C2000 controllers work well with the TPS75005 default settings (without external delay capacitors).

NOTE

As with the SS1 and SS2 terminals, CT1 and CT2 are very high-impedance nodes with very low values of constant current source. These two terminals cannot be monitored by regular oscilloscope probes. Connecting such regular probes to CT1 or CT2 changes the behavior of the soft-start function and no valid waveform can be monitored.

To monitor these terminals, use high-impedance probes, such as *active FET probes*.

Spike Noise Sensitivity

Application Report SBVA033, *TPS75005 Advanced Information: Voltage Monitor Noise Immunity*, explains TPS75005 noise immunity performance.

Power-Down Monitoring

The TPS75005 monitors both OUT1 and OUT2 to become 0.3 V in power-down sequence so that next power-up sequence starts from below 0.3 V.

See the SEQUENCER BLOCK section for more details.

NOTE

In any application circuit, a diode or two diodes in series should not be placed from OUT1 (anode, 1.8 V) to OUT2 (cathode, 3.3 V). Such diode(s) prevent the TPS75005 from pulling OUT2 below 0.3 V; the device stays in a power-down sequence and will not power up again.

Auxiliary Voltage Monitor (SVS3)

The TPS75005 has an independent supply voltage supervisor (SVS3) for an auxiliary purpose. The input voltage to the VMON pin is compared with the 1.206 V internal reference and VDET is the output.

One of the most common uses of this feature is to monitor the input voltage. For example, many applications may need to monitor the input voltage at a level higher than the UVLO. Figure 28 shows this type of example. At the VMON pin, use a proper voltage divider to set a target voltage, calculated by the following equation:

$$(\text{SVS3 Detection Voltage Target}) = 1.206\ (\text{V}) \times \frac{R_1 + R_2}{R_2} \quad (3)$$

By pulling up VDET to VIN, the VDET output can be connected to the EN pin.

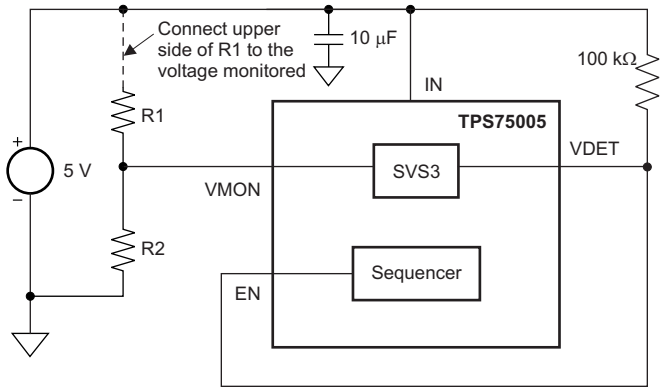


Figure 28. SVS (VMON and VDET) Connection

Thermal Shutdown (TSD)

The thermal protection feature disables the device outputs when the junction temperature rises to approximately +165°C, allowing the device to cool. When the junction temperature cools to approximately +145°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage because of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat spreading layers. For reliable operation, junction temperature should be limited to +125°C maximum by using the appropriate area of heat spreading layers.

The internal protection circuitry of the TPS75005 is designed to protect against overload conditions, and is not intended to replace proper PCB design. Continuously running the TPS75005 into thermal shutdown degrades device reliability.

This thermal shutdown function disables both LDO1 and LDO2, regardless of sequencer status. Releasing the TSD restarts the power-up sequence.

Undervoltage Lockout (UVLO)

The TPS75005 uses an undervoltage lockout (UVLO) circuit to keep the output shut off until the internal circuitry is operating properly. The UVLO circuit has a hysteresis feature so that short undershoot transients are typically ignored.

See Figure 11 for the actual measurement. See the section for how to set a custom threshold voltage for the input voltage.

Within the TPS75005, UVLO is combined with EN to create an internal enable signal. A logic AND operation of the EN input signal and internal UVLO signal is used to control the sequencer. By connecting EN to VIN, a logic input buffer for the EN and UVLO circuit refer to the same electric node and the device can be controlled by UVLO function because V_{UVLO} is greater than $V_{IH(EN)}$. Figure 29 shows how to control the TPS75005 without a signal source to the EN pin.

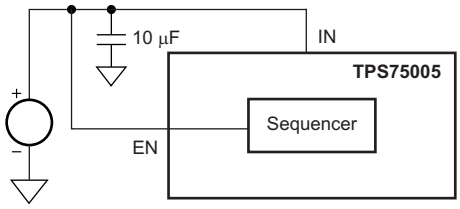


Figure 29. TPS75005 without EN Signal Control

SEQUENCER BLOCK

The TPS75005 integrates a sequencer logic circuit to control the power-up and power-down sequences of the two output voltage rails (V_{DD} and V_{DDIO}) for C2000 controllers.

Application Report SBVA031, *TPS75005 Advanced Information: Sequencer and State Machine*, explains a state machine of this sequencer logic in detail.

C2000 Power Sequencing

Depending on the C2000 controller series, the required power-up and power-down order of V_{DD} and V_{DDIO} can be different, as shown in Table 1. Figure 30 and Figure 31 shows the typical waveforms of two different sequencing cycles set by the SEQ pin.

Table 1. Required Power-Up and Power-Down Sequence of C2000 Controllers

C2000 CONTROLLER	POWER-UP ORDER		POWER-DOWN ORDER		TPS75005 SEQ SETTING	TYPICAL WAVEFORM
	1ST CHANNEL TURNED ON	2ND CHANNEL TURNED ON	1ST CHANNEL TURNED OFF	2ND CHANNEL TURNED OFF		
F280x/F2801x	V_{DD}	V_{DDIO}	V_{DDIO}	V_{DD}	Logic-L	Figure 30
F281x	V_{DDIO}	V_{DD}	V_{DD}	V_{DDIO}	Logic-H	Figure 31
F2823x	V_{DD}	V_{DDIO}	V_{DDIO}	V_{DD}	Logic-L	Figure 30
F2833X	V_{DD}	V_{DDIO}	V_{DDIO}	V_{DD}	Logic-L	Figure 30

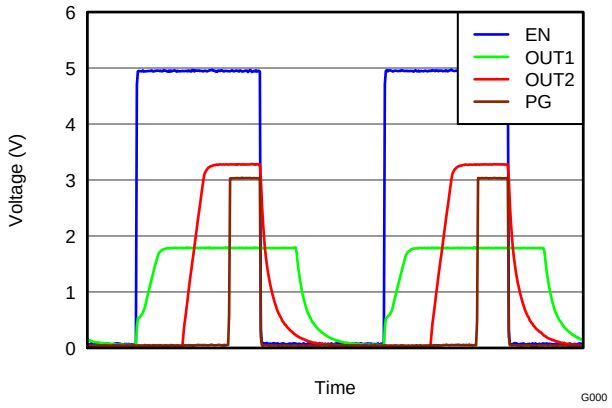


Figure 30. Power Sequence with SEQ = L

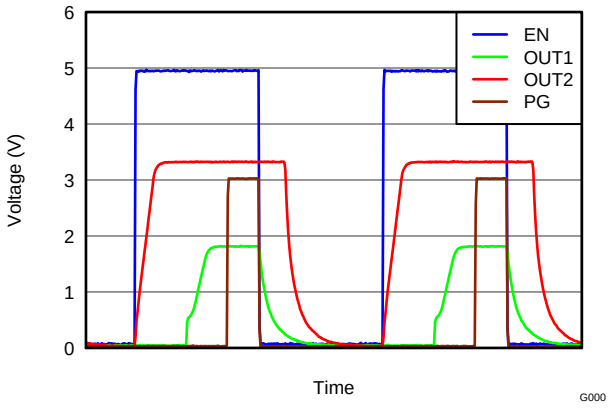


Figure 31. Power Sequence with SEQ = H

Normal Power-Up and Power-Down Sequence

Figure 32 shows oscilloscope waveforms of the TPS75005 in a normal power-up and power-down sequence with SEQ = L. Refer to the time lines labeled Event A through Event H.

1. Before Event A, the TPS75005 is idle, waiting for an enable event.

(Power-Up Sequence Begins)

2. At Event A, EN goes to logic-H and the device immediately discharges a soft-start capacitor (C_{SS1}) by using a one-shot circuit. Then, the LDO1 soft-start circuit starts charging C_{SS1}. The OUT1 voltage follows the SS1 voltage. Time between Event A and Event B is defined as t_{SS1} and can be programmed by C_{SS1}.
3. At Event B, the OUT1 voltage exceeds the V_{SVS1} threshold and the SVS1 delay circuit starts charging C_{CT1}. Time between Event B and Event C is defined as $t_{d(SVS1)}$ and can be programmed by C_{CT1}.
4. At Event C, the CT1 voltage exceeds the V_{CT1} threshold to discharge a soft-start capacitor (C_{SS2}) using a one-shot circuit. Then, the LDO2 soft-start circuit starts charging C_{SS2}. The OUT2 voltage follows the SS2 voltage. Time between Event C and Event D is defined as t_{SS2} and can be programmed by C_{SS2}.
5. At Event D, the OUT2 voltage exceeds the V_{SVS2} threshold and the SVS2 delay circuit starts charging C_{CT2}. Time between Event D and Event E is defined as $t_{d(SVS2)}$ and can be programmed by C_{CT2}.

(Power-Up Sequence Ends)

6. At Event E, the CT2 voltage exceeds the V_{CT2} threshold and PG goes high to enable the C2000 controller. The TPS75005 is up and running as long as a disable or an error event occurs.

(Power-Down Sequence Begins)

7. At Event F, EN goes to logic-L and the device immediately turns PG to logic-L so that the C2000 controller is disabled. Then, an internal signal $\underline{EN2}$ goes to logic-L in order to disable LDO2. Because the active pull-down switch is enabled by SW2 (= $\overline{EN2}$) signal, the OUT2 voltage starts decreasing (note that this ramp-down speed depends on the application circuits).
8. At Event G, the OUT2 voltage underruns the V_{DOWN2} threshold and an internal signal EN1 goes into logic-L in order to disable LDO1. Because the active pull-down switch is enabled by SW1 (= $\overline{EN1}$) signal, the OUT1 voltage starts decreasing (note that this ramp-down speed is depends on the application circuits).
9. At Event H, the OUT1 voltage underruns the V_{DOWN1} threshold to return back to the idle state.

(Power-Down Sequence Ends)

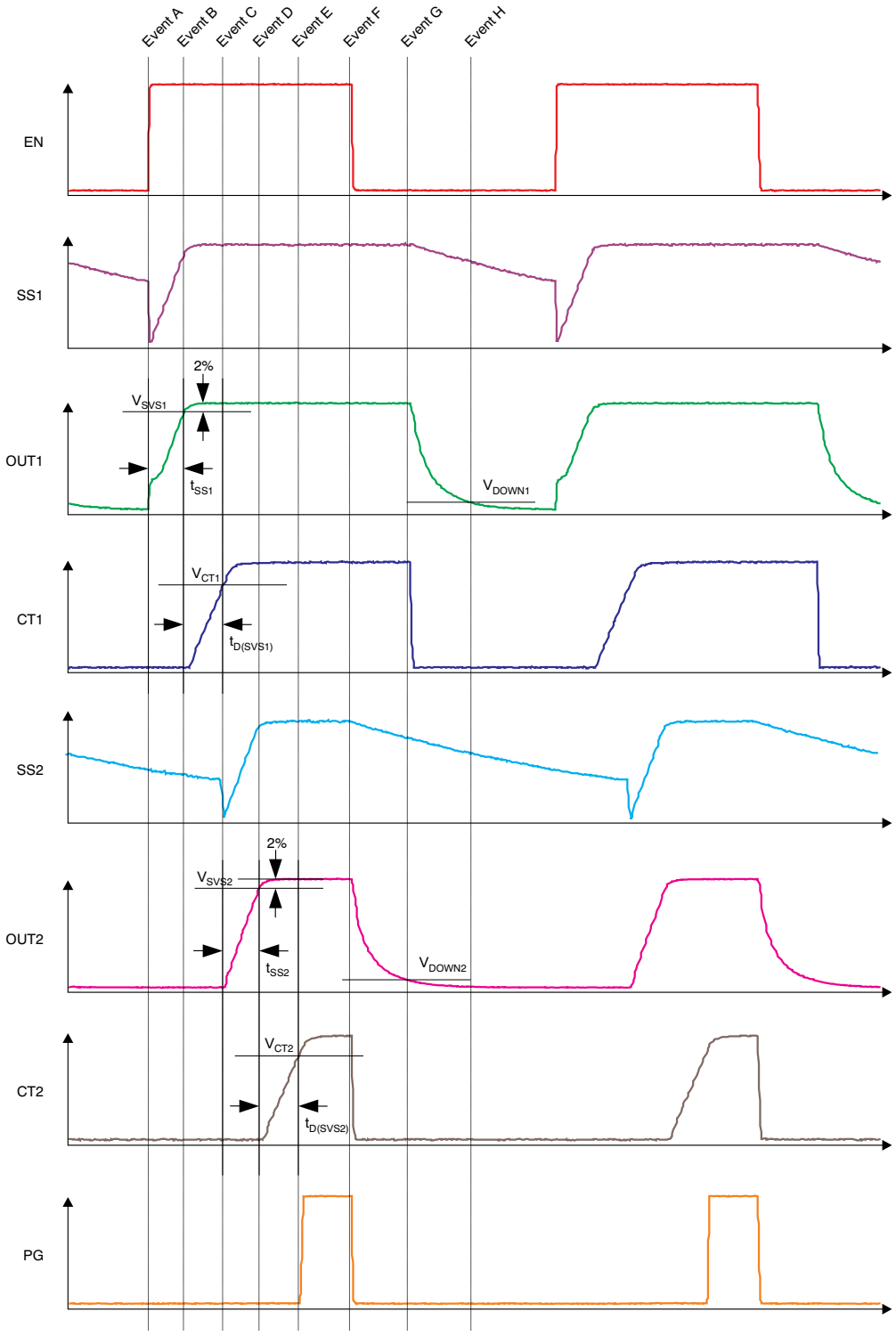


Figure 32. Normal Power-Up and Power-Down Timing

THERMAL INFORMATION

Power Dissipation

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the tab or pad is critical to avoiding thermal shutdown and ensuring reliable operation.

Power dissipation of the device depends on input voltage and load conditions and can be calculated using Equation 4:

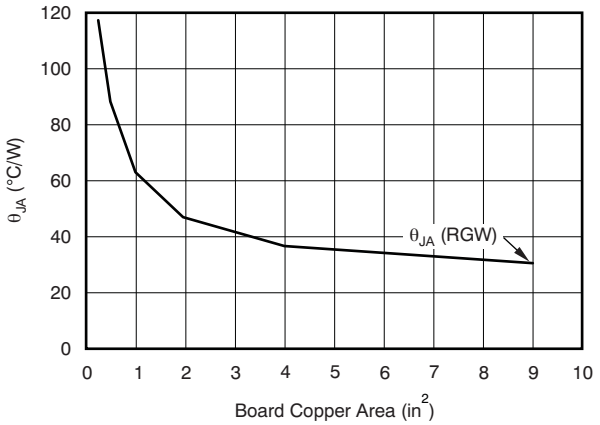
$$P_D = (V_{IN} - V_{OUT})\, I_{OUT} \quad (4)$$

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

On the QFN (RGW) package, the primary conduction path for heat is through the exposed pad to the printed circuit board (PCB). The pad can be connected to ground or be left floating; however, it should be attached to an appropriate amount of copper PCB area to ensure the device does not overheat. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device and can be calculated using Equation 5:

$$R_{\theta JA} = \left(\frac{+125^\circ C - T_A}{P_D} \right) \quad (5)$$

Knowing the maximum $R_{\theta JA}$, the minimum amount of PCB copper area needed for appropriate heat sinking can be estimated using Figure 33.



NOTE: θ_{JA} value at a board size of 9-in^2 (that is, 3-in × 3-in) is a JEDEC standard.

Figure 33. θ_{JA} vs Board Size

Figure 33 shows the variation of θ_{JA} as a function of ground plane copper area in the board. It is intended only as a guideline to demonstrate the effects of heat spreading in the ground plane and should not be used to estimate actual thermal performance in real application environments.

NOTE: When the device is mounted on an application PCB, it is strongly recommended to use Ψ_{JT} and Ψ_{JB}, as explained in the *Estimating Junction Temperature* section.

Estimating Junction Temperature

Using the thermal metrics Ψ_{JT} and Ψ_{JB}, as shown in the *Thermal Information* table, the junction temperature can be estimated with corresponding formulas (given in Equation 6). For backwards compatibility, an older $\theta_{JC,Top}$ parameter is listed as well.

Ψ_{JT}: $T_J = T_T + \Psi_{JT} \bullet P_D$

Ψ_{JB}: $T_J = T_B + \Psi_{JB} \bullet P_D$

Where:

P_D is the power dissipation shown by Equation 5

T_T is the temperature at the center-top of the device

T_B is the PCB temperature measured 1 mm away from the device *on the PCB surface* (as Figure 35 shows). (6)

NOTE: Both T_T and T_B can be measured on actual application boards using an infrared thermometer.

For more information about measuring T_T and T_B, see Application Report SBVA025, *Using New Thermal Metrics*, available for download at www.ti.com.

By looking at Figure 34, the new thermal metrics (Ψ_{JT} and Ψ_{JB}) have very little dependency on board size. That is, using Ψ_{JT} or Ψ_{JB} with Equation 6 is a good way to estimate T_J by simply measuring T_T or T_B, regardless of the application board size.

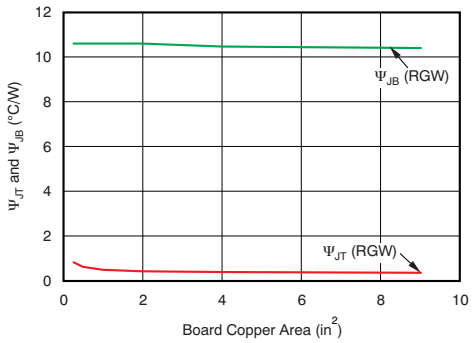
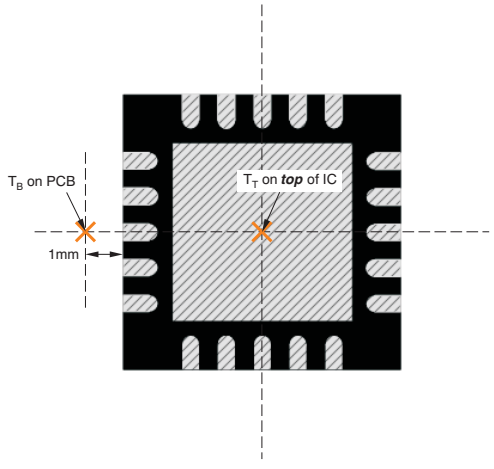


Figure 34. Ψ_{JT} and Ψ_{JB} vs Board Size

For a more detailed discussion of why TI does not recommend using $\theta_{JC(top)}$ to determine thermal characteristics, refer to Application Report SBVA025, *Using New Thermal Metrics*, available for download at www.ti.com. For further information, refer to Application Report SPRA953, *IC Package Thermal Metrics*, also available on the TI website.



(a) Example RGW (QFN) Package Measurement

Figure 35. Measuring Points for T_T and T_B

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (March 2012) to Revision C **Page**

- Changed Voltage Information table 2
- Added new note 2 to Thermal Information table 3
- Changed note 3(b) copper coverage value from 20% to 4% 3
- Changed test condition for $t_{D(SVS1)}$ parameter 4
- Changed test condition for $t_{D(SVS2)}$ parameter 5
- Changed functional block diagram 7

Changes from Revision A (February 2012) to Revision B **Page**

- Changed Thermal Information table values 3
- Changed functional block diagram 7

Changes from Original (November 2011) to Revision A **Page**

- Changed all "PowerPAD" to "thermal pad". 1
- Added application report links to *Description* section 1
- Changed "VIN" to "IN" in front page diagram 1
- Changed "V_{IN}" to "IN" 6
- Changed "VIN" to "input voltage" 12
- Changed caption for Figure 25 12
- Changed *Voltage Monitor Blocks* section title and updated subsection order 17
- Changed "VIN" to "IN" in Figure 28 18
- Changed "VIN" to "IN" in Figure 29 19

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS75005RGWR	NRND	VQFN	RGW	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PPMQ	
TPS75005RGWT	NRND	VQFN	RGW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PPMQ	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

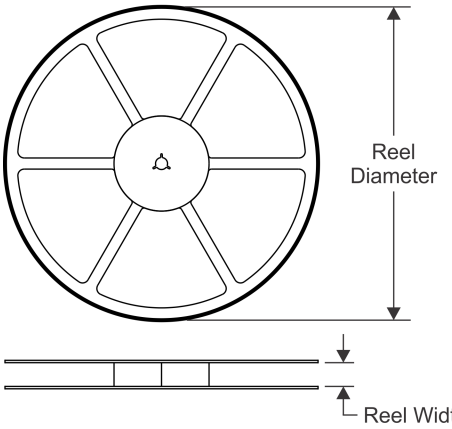
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

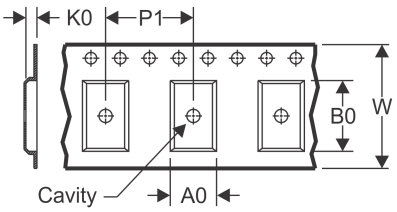
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

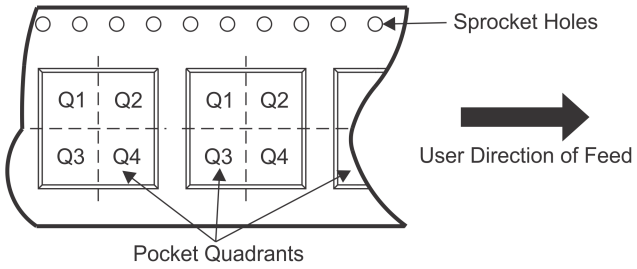


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

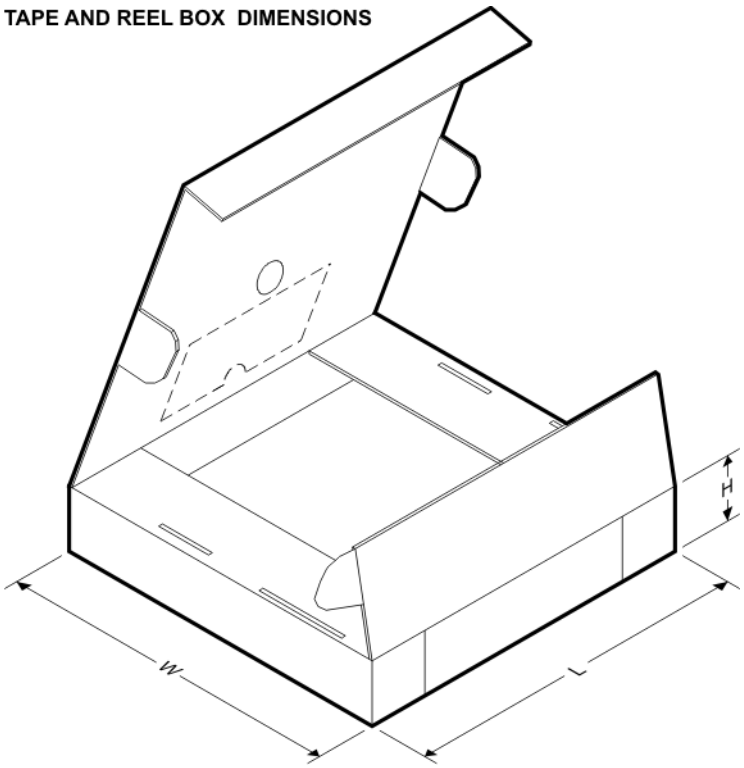
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS75005RGWR	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS75005RGWT	VQFN	RGW	20	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

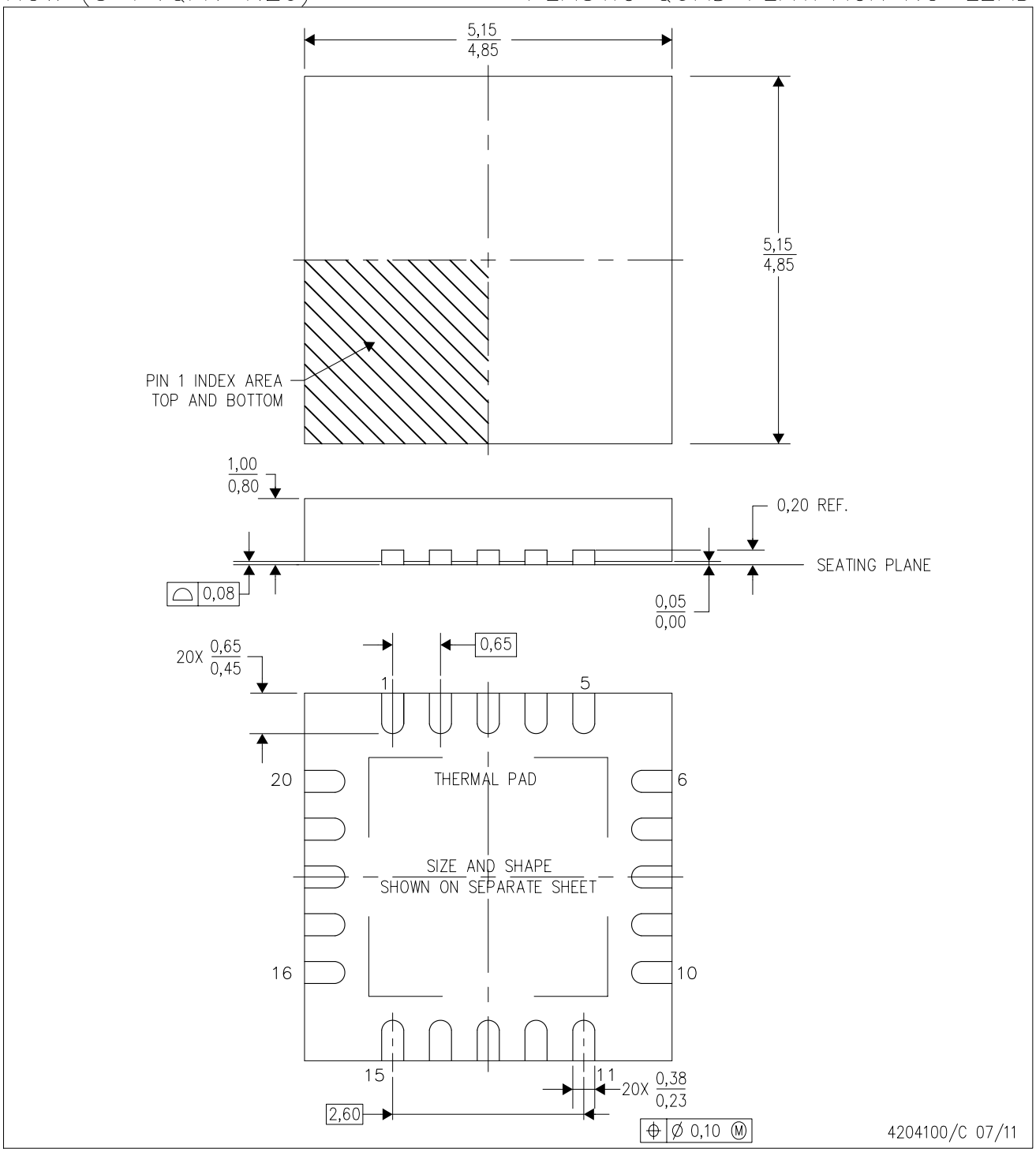
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS75005RGWR	VQFN	RGW	20	3000	367.0	367.0	35.0
TPS75005RGWT	VQFN	RGW	20	250	210.0	185.0	35.0

RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flat pack, No–leads (QFN) package configuration
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

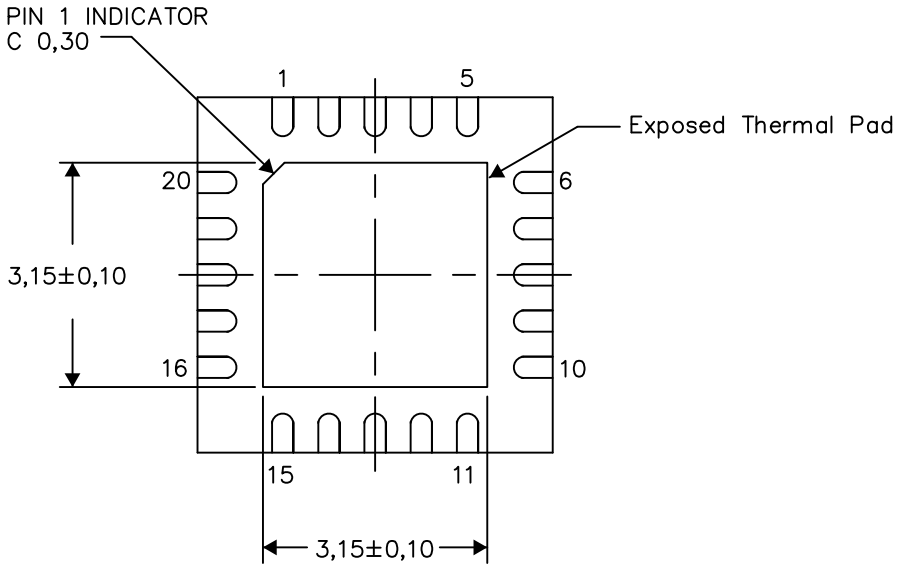
RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



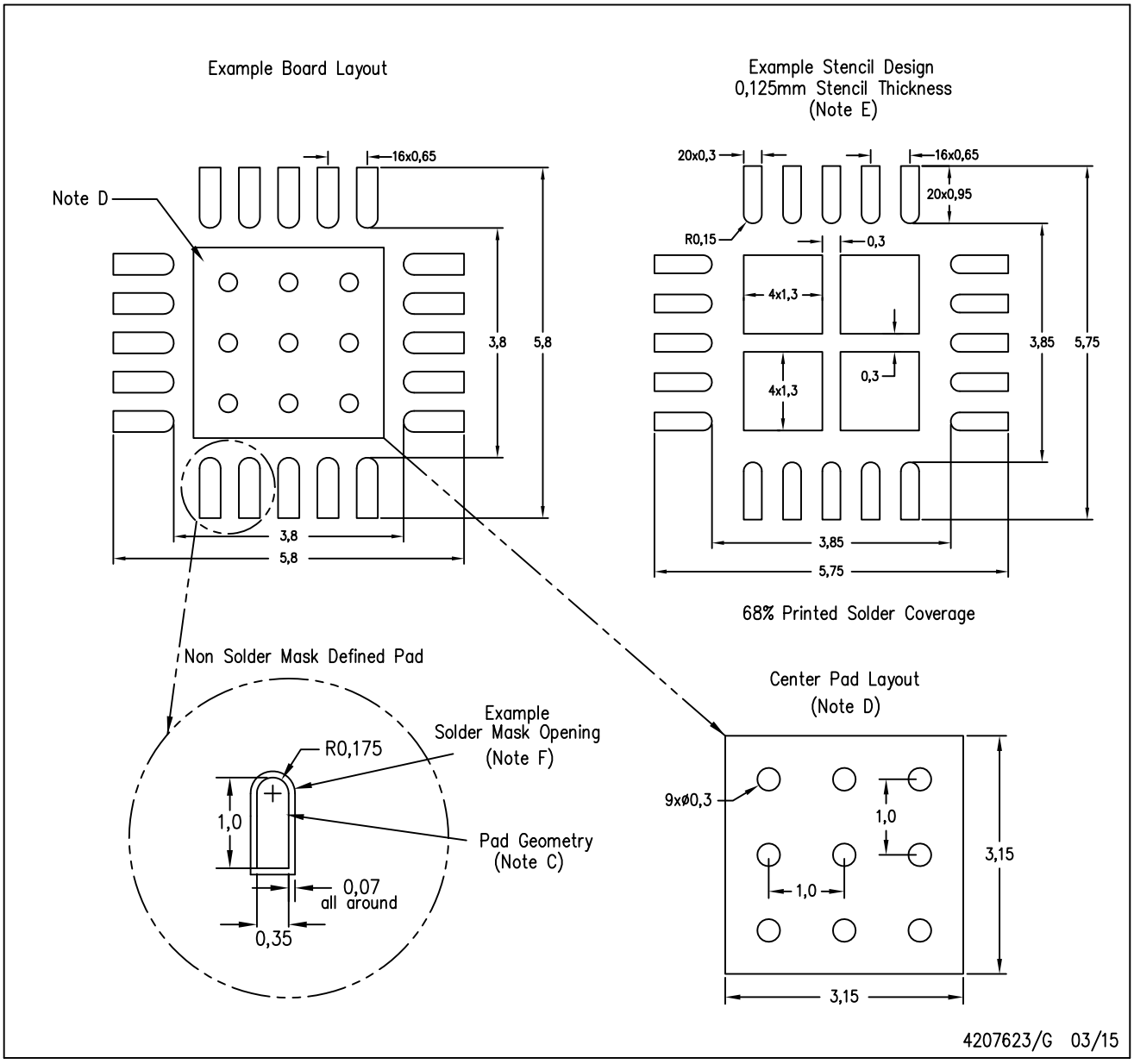
Bottom View

Exposed Thermal Pad Dimensions

4206352–2/L 03/15

NOTE: All linear dimensions are in millimeters

RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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