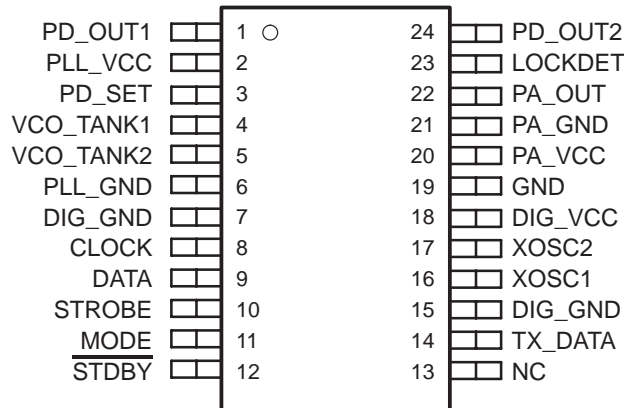


- Single-Chip RF Transmitter for 868-MHz and 915-MHz ISM Bands
- 850-MHz to 950-MHz Operation
- FM/FSK Operation for Transmit
- 24-Bit Direct Digital Synthesizer (DDS) With 11-Bit DAC
- On-Chip Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL)
- On-Chip Reference Oscillator
- Minimal External Components Required
- Low Power Consumption
- Typical Output Power of 7 dBm
- Typical Output Frequency Resolution of 230 Hz
- Ultrafast Lock Times From DDS Implementation
- Two Fully-Programmable Operational Modes
- 2.2-V to 3.6-V Operation
- Flexible Serial Interface to TI MSP430 Microcontroller
- 24-Pin Plastic Thin-Shrink Small-Outline Package (TSSOP)

PW PACKAGE  
(TOP VIEW)



## description

The TRF4900 single-chip solution is an integrated circuit intended for use as a low cost FSK transmitter to establish a frequency-agile RF link. The device is available in a 24-lead TSSOP package and is designed to provide a fully-functional multichannel transmitter. The chip is intended for linear (FM) or digital (FSK) modulated applications in the new 868-MHz European band and the North American 915-MHz ISM band. The single chip transmitter operates down to 2.2 V and is expressly designed for low power consumption. The synthesizer has a typical channel spacing of approximately 230 Hz to allow narrow-band as well as wide-band applications. Due to the narrow channel spacing of the direct digital synthesizer (DDS), the DDS can be used to adjust the TX frequency and allows the use of inexpensive reference crystals.

Two fully-programmable operation modes, Mode0 and Mode1, allow extremely fast switching between two preprogrammed settings (e.g., TX\_frequency\_0/TX\_frequency\_1) without reprogramming the device. Each functional block of the transmitter can be specifically enabled or disabled via the serial interface.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# TRF4900 SINGLE-CHIP RF TRANSMITTER

SLWS092G – JULY 2000 – REVISED FEBRUARY 2005

## ISM band standards

Europe has assigned a new unlicensed frequency band of 868 MHz to 870 MHz. This new band is specifically defined for short range devices with duty cycles from 0.1% to 100% in several sub-bands. The existing 433-MHz band for short-range devices in Europe has the great disadvantage of very high usage. The new European frequency band, due to the duty cycle assignment, allows a reliable RF link and makes many new applications possible.

The North American unlicensed ISM (industrial, scientific, and medical) band covers 902 MHz to 928 MHz (center frequency of 915 MHz) and is suitable for short range RF links.

## transmitter

The transmitter consists of an integrated VCO, a complete fully-programmable direct digital synthesizer, and a power amplifier. The internal VCO can be used with an external tank circuit or an external VCO. The divider, prescaler, and reference oscillator require only the addition of an external crystal and a loop filter to provide a complete DDS with a typical frequency resolution of 230 Hz.

The 8-bit FSK frequency deviation register determines the frequency deviation in FSK mode. The modulation itself is done in the direct digital synthesizer, hence no additional external components are necessary.

Since the typical RF output power is approximately 7 dBm, no additional external RF power amplifier is necessary in most applications.

The TRF4900 RF transmitter is suitable for use in applications that include the TRF6900 RF transceiver.

## baseband interface

The TRF4900 can easily be interfaced to a baseband processor such as the Texas Instruments MSP430 ultralow-power microcontroller (see Figure 1). The TRF4900 serial control registers are programmed by the MSP430 and the MSP430 performs baseband operations in software.

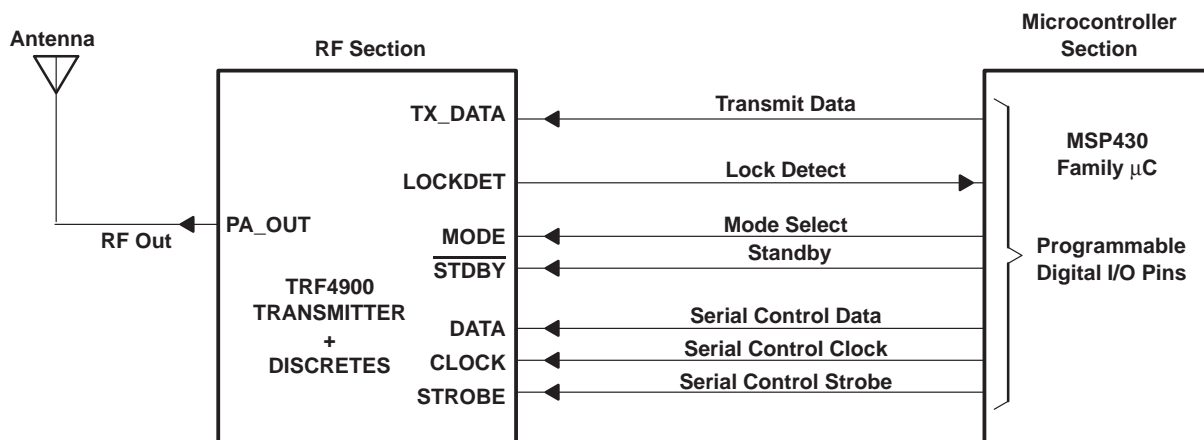
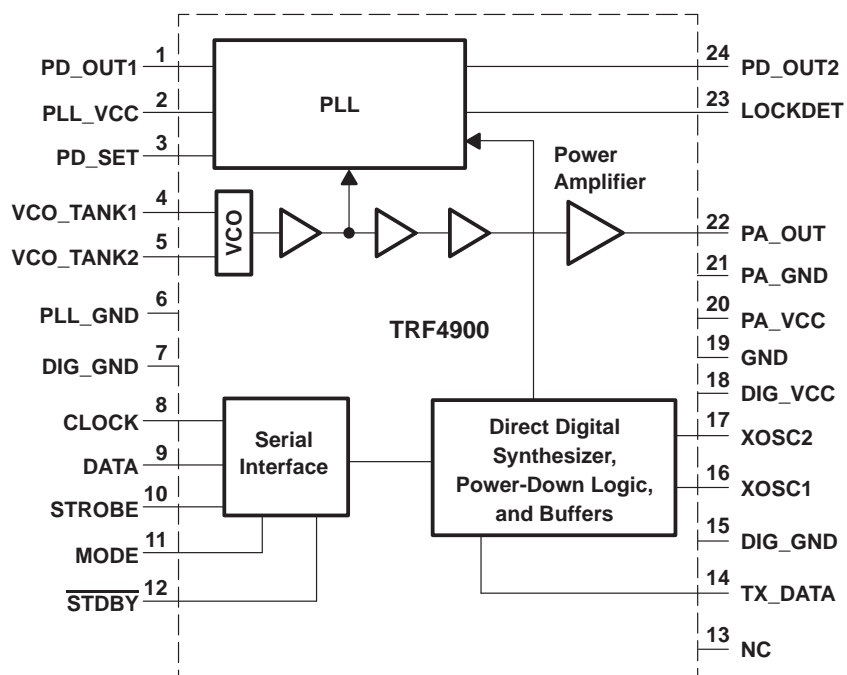


Figure 1. System Block Diagram for Interfacing to the MSP430 Microcontroller

## functional block diagram



# TRF4900

## SINGLE-CHIP RF TRANSMITTER

SLWS092G – JULY 2000 – REVISED FEBRUARY 2005

### Terminal Functions

| TERMINAL NAME | NO.   | I/O | DESCRIPTION  |
|---------------|-------|-----|--|
| CLOCK         | 8     | I   | Serial interface clock signal  |
| DATA          | 9     | I   | Serial interface data signal   |
| DIG_GND       | 7, 15 |     | Digital ground   |
| DIG_VCC       | 18    |     | Digital supply voltage   |
| GND           | 19    |     | Ground   |
| LOCKDET       | 23    | O   | PLL lock detect output, active high. PLL locked when LOCKDET = 1.  |
| MODE          | 11    | I   | Mode select input. The functionality of the device in Mode0 or Mode1 can be programmed via the A-, B-, C-, and D-words of the serial control interface.  |
| NC            | 13    |     | No connection  |
| PA_GND        | 21    |     | Power amplifier ground   |
| PA_OUT        | 22    | O   | Power amplifier output, open collector   |
| PA_VCC        | 20    |     | Power amplifier supply voltage   |
| PD_OUT1       | 1     | O   | Charge pump output – PLL in locked condition   |
| PD_OUT2       | 24    | O   | Charge pump output – PLL in unlocked condition   |
| PD_SET        | 3     |     | Charge pump current setting terminal. An external resistor, $R_{PD}$ , is connected to this terminal to set the nominal charge pump current.   |
| PLL_GND       | 6     |     | PLL ground   |
| PLL_VCC       | 2     |     | PLL supply voltage   |
| STDBY         | 12    | I   | Standby control for the TRF4900, active low. While $\overline{\text{STDBY}} = 0$ , the contents of the control registers are still valid and can be programmed via the serial control interface. |
| STROBE        | 10    | I   | Serial interface strobe signal   |
| TX_DATA       | 14    | I   | Digital modulation buffered input for FSK/FM modulation of the carrier, active high  |
| VCO_TANK1     | 4     | I   | VCO tank circuit connection. Should be left open if an external VCO is used.   |
| VCO_TANK2     | 5     | I   | VCO tank circuit connection. May also be used to input an external VCO signal.   |
| XOSC1         | 16    | O   | Reference crystal oscillator connection  |
| XOSC2         | 17    | I   | Reference crystal oscillator connection. May be used as a single-ended clock input if an external crystal is not used.   |



**absolute maximum ratings over operating free-air temperature (unless otherwise noted)†**

|  |                 |
|--|-----------------|
| Supply voltage range, PA_VCC, PLL_VCC, DIG_VCC, VCC (see Note 1) | –0.6 to 4.5 Vdc |
| Input voltage, logic signals                                     | –0.6 to 4.5 Vdc |
| Storage temperature range  | –65°C to 150°C  |
| ESD integrity‡   | 2 kV HBM        |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ RF terminal 22, PA\_OUT, is not protected against voltage stress higher than 800 V HBM.

NOTE 1: All GND and VCC terminals must be connected to either ground or supply, respectively, even if the function block is not used.

**recommended operating conditions**

|   | MIN                  | TYP | MAX | UNIT |
|---|----------------------|-----|-----|------|
| Supply voltage, PA_VCC, PLL_VCC, DIG_VCC, DDS_VCC, VCC  | 2.2                  |     | 3.6 | V    |
| Operating temperature   | –20                  |     | 60  | °C   |
| High-level input voltage, V <sub>IH</sub> (DATA, CLOCK, STROBE, TX_DATA, MODE, <u>STDBY</u> ) | V <sub>CC</sub> –0.5 |     |     | V    |
| Low-level input voltage, V <sub>IL</sub> (DATA, CLOCK, STROBE, TX_DATA, MODE, <u>STDBY</u> )  |                      |     | 0.5 | V    |
| High-level output voltage, V <sub>OH</sub> (LOCKDET); I <sub>OH</sub> = 0.5 mA                | V <sub>CC</sub> –0.5 |     |     | V    |
| Low-level output voltage, V <sub>OL</sub> (LOCKDET); I <sub>OL</sub> = 0.5 mA                 |                      |     | 0.5 | V    |

**electrical characteristics over full range of operating conditions, (typical values are at PA\_VCC, PLL\_VCC, DIG\_VCC, VCC = 3 V, T<sub>A</sub> = 25°C) (unless otherwise noted)**

**supply current consumption in each mode**

| MODE                      | ACTIVE STAGES     | MIN               | TYP | MAX  | UNIT |
|---------------------------|-------------------|-------------------|-----|------|------|
| Power down (standby mode) | None              |                   | 0.5 |      | μA   |
| TX                        | <b>PA STATE</b>   |                   |     |      | mA   |
|                           | 0-dB attenuation  |                   | 58  | 75   |      |
|                           | 10-dB attenuation | DDS, PLL, VCO, PA | 27  |      |      |
|                           | 20-dB attenuation |                   | 22  |      |      |
|                           | PA disabled       |                   | 10  | 12.5 |      |

**VCO**

| PARAMETER       | TEST CONDITIONS | MIN | TYP | MAX                   | UNIT   |
|-----------------|-----------------|-----|-----|-----------------------|--------|
| Frequency range |                 | 850 |     | 950                   | MHz    |
| Phase noise     | 50-kHz offset   |     | –94 |                       | dBc/Hz |
| Tuning voltage  |                 | 0.5 |     | V <sub>CC</sub> – 0.4 | V      |

# TRF4900

## SINGLE-CHIP RF TRANSMITTER

SLWS092G – JULY 2000 – REVISED FEBRUARY 2005

electrical characteristics over full range of operating conditions, (typical values are at PA\_VCC, PLL\_VCC, DIG\_VCC, VCC = 3 V, T<sub>A</sub> = 25°C) (unless otherwise noted) (continued)

### direct digital synthesizer (DDS)

| PARAMETER                                       | TEST CONDITIONS | MIN                            | TYP | MAX     | UNIT |
|---|-----------------|--------------------------------|-----|---------|------|
| Reference oscillator input frequency, $f_{ref}$ | As oscillator   | 15                             |     | 26      | MHz  |
|   | As buffer       | 15                             |     | 26      |      |
| Programmable DDS divider ratio                  | 22 bits         | 0                              |     | 4194303 |      |
| DDS divider resolution, $\Delta f$              |                 | $N \times f_{ref} \div 2^{24}$ |     |         |      |
| FSK – modulation register ratio                 | 8 bits          | 0                              |     | 1020    |      |
| FSK – modulation resolution                     |                 | $N \times f_{ref} \div 2^{22}$ |     |         |      |

### PLL

| PARAMETER                      | TEST CONDITIONS   | MIN                            | TYP | MAX | UNIT |
|--------------------------------|---|--------------------------------|-----|-----|------|
| RF input frequency             |   | 850                            |     | 950 | MHz  |
| RF input power                 | Internal VCO bypassed; external input applied to VCO_TANK2    |                                | -10 |     | dBm  |
| RF input divider ratio, N      |   | 256                            |     | 512 |      |
| RF output frequency resolution |   | $N \times f_{ref} \div 2^{24}$ |     |     |      |
| Charge pump current            | Programmable with external resistor, 100 kΩ nominal, APLL = 0 |                                | 70  |     | μA   |

### power amplifier

| PARAMETER                           | TEST CONDITIONS                         | MIN           | TYP | MAX | UNIT |
|-------------------------------------|---|---------------|-----|-----|------|
| Frequency range                     |   | 850           |     | 950 | MHz  |
| Amplifier output power (see Note 2) | 0-dB attenuation                        |               | 7   |     | dBm  |
|                                     | 10-dB attenuation                       |               | -3  |     |      |
|                                     | 20-dB attenuation                       |               | -12 |     |      |
|                                     | Amplifier off                           |               |     | -52 |      |
| Optimal load impedance              |   | See Figure 11 |     |     | Ω    |
| 2 <sup>nd</sup> -order harmonic     | V <sub>CC</sub> = 3 V, 0-dB attenuation |               | -13 |     | dBc  |
| 3 <sup>rd</sup> -order harmonic     | V <sub>CC</sub> = 3 V, 0-dB attenuation |               | -32 |     | dBc  |

NOTE 2: The device and output matching network (see *Application Information* section) is designed to provide the output power into a 50-Ω load. The device stability was tested (no parasitic oscillations) with an output VSWR of 10:1 over all phase angles and is not tested in production.

### typical mode switching and lock times

| OPERATION                 | TEST CONDITIONS   | MIN | TYP | MAX | UNIT |
|---------------------------|---|-----|-----|-----|------|
| Standby to transmit time† | From rising edge of STDBY to valid RF signal at PA_OUT, APLL = 111b (maximum) |     | 500 |     | μs   |

† Highly dependent upon loop filter topology



timing data for serial interface (see Figure 2)

| PARAMETER                |  | MIN | MAX | UNIT |
|--------------------------|--|-----|-----|------|
| $f_{\text{(CLOCK)}}$     | CLOCK frequency  |     | 20  | MHz  |
| $t_{\text{w(CLKHI)}}$    | CLOCK high time pulse width, CLOCK high                | 25  |     | ns   |
| $t_{\text{w(CLKLO)}}$    | CLOCK low time pulse width, CLOCK low                  | 25  |     | ns   |
| $t_{\text{su(DATA)}}$    | Setup time, data valid before CLOCK high               | 25  |     | ns   |
| $t_{\text{h(DATA)}}$     | Hold time, data valid after CLOCK high                 | 25  |     | ns   |
| $t_{\text{w(STROBEHI)}}$ | Strobe high time pulse width, STROBE high (see Note 3) | 25  |     | ns   |
| $t_{\text{w(STROBELO)}}$ | Strobe low time pulse width, STROBE low                | 25  |     | ns   |

NOTE 3: CLOCK and DATA must both be low when STROBE is asserted (STROBE = 1).

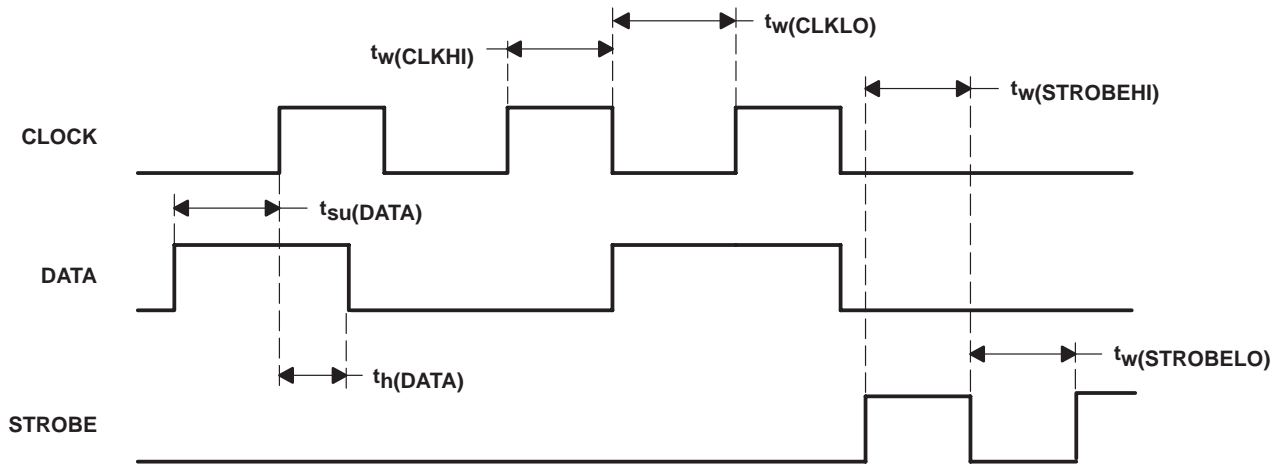


Figure 2. Serial Data Interface Timing

detailed description

reference oscillator

The reference oscillator provides the DDS system clock. It allows operation, with a suitable external crystal, between 15 MHz and 26 MHz.

An external oscillator can be used to supply clock frequencies between 15 MHz and 26 MHz. The external oscillator should be directly connected to XOSC2, terminal 17. The other oscillator terminal (XOSC1, terminal 16) should be left open or can be used as a buffered version of the signal applied at terminal 17 (see Figure 3). The same crystal or externally supplied oscillator signal is used to derive both the transmit and receive frequencies.

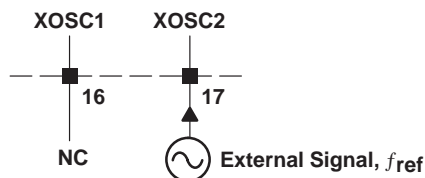


Figure 3. Applying an External Oscillator Signal

# TRF4900 SINGLE-CHIP RF TRANSMITTER

SLWS092G – JULY 2000 – REVISED FEBRUARY 2005

## detailed description (continued)

### direct digital synthesizer

#### general principles of DDS operation

In general, a direct digital synthesizer (DDS) is based on the principle of generating a sine wave signal in the digital domain. Benefits include high precision, wide frequency range, a high degree of software programmability, and extremely fast lock times.

Figure 4 shows a block diagram of a typical DDS. It generally consists of an accumulator, sine lookup table, a digital-to-analog converter, and a low-pass filter. All digital blocks are clocked by the reference oscillator.

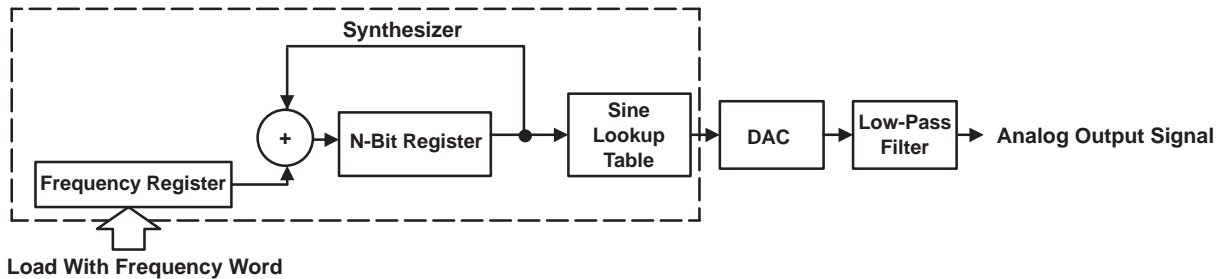


Figure 4. Typical DDS Block Diagram

The DDS constructs an analog sine waveform using an N-bit adder counting up from 0 to  $2^N$  in steps of the frequency register whereby generating a digital ramp waveform. Each number in the N-bit output register is used to select the corresponding sine wave value out of the sine lookup table. After the digital-to-analog conversion, a low-pass filter is necessary to suppress unwanted spurious responses.

The analog output signal can be used as a reference input signal for a phase-locked loop (PLL). The PLL circuit multiplies the reference frequency by a predefined factor.

#### TRF4900 direct digital synthesizer implementation

Figure 5 shows a block diagram of the DDS implemented in the TRF4900. It consists of a 24-bit accumulator clocked by the reference oscillator along with control logic settings.

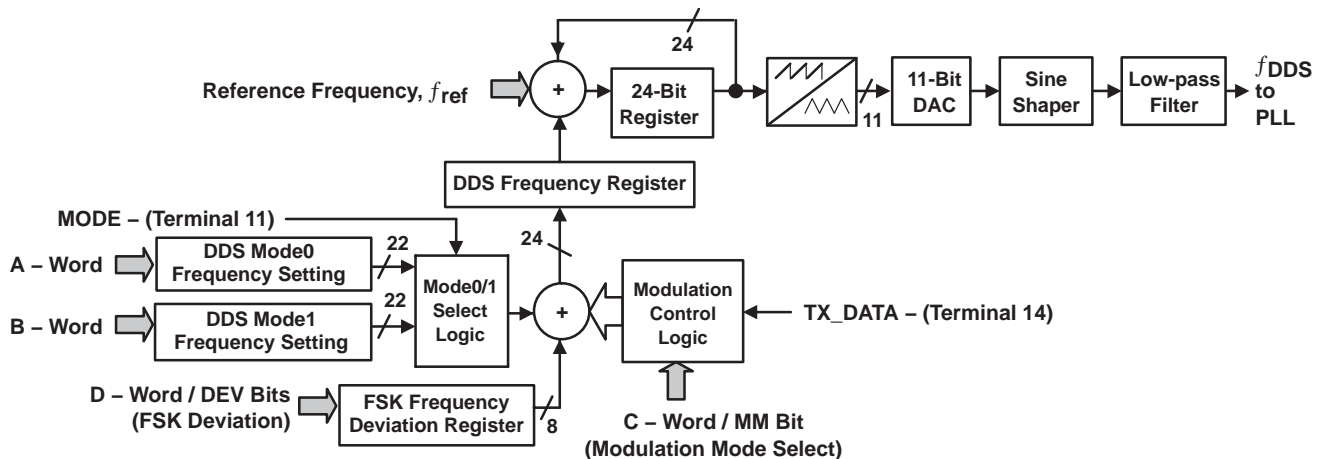


Figure 5. DDS Block Diagram as Implemented in the TRF4900

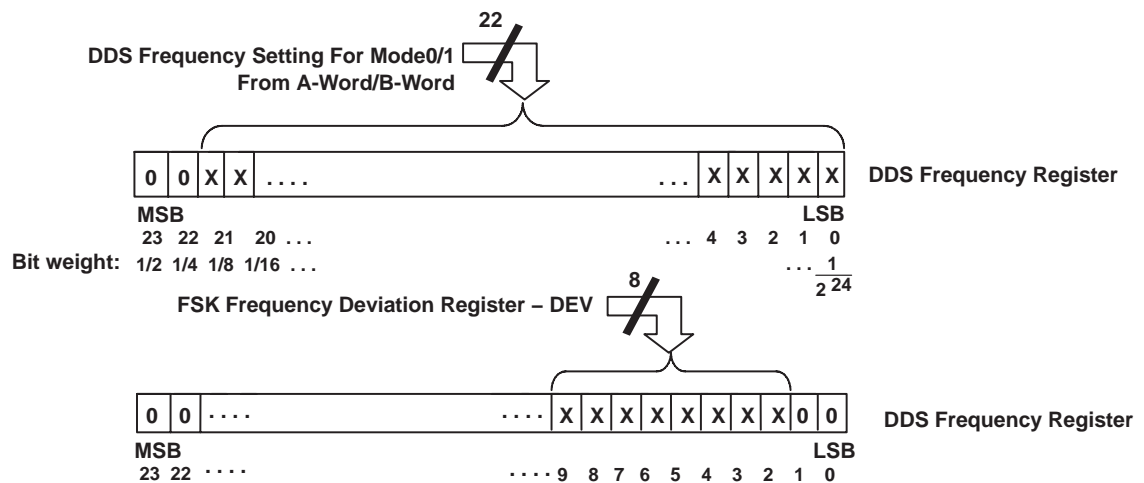


**TRF4900 direct digital synthesizer implementation (continued)**

The frequency of the reference oscillator,  $f_{ref}$ , is the DDS sample frequency, which also determines the maximum DDS output frequency. Together with the accumulator width (in bits), the frequency resolution of the DDS can be calculated. Multiplied by the divider ratio (prescaler) of the PLL, N, the minimum frequency step size of the TRF4900 is calculated as follows:

$$\Delta f = N \times \frac{f_{ref}}{2^{24}}$$

The 24-bit accumulator can be programmed via two 22-bit frequency setting registers (the A-word determines the mode0 frequency, the B-word determines the mode1 frequency) with the two MSB bits set to 0. Consequently, the maximum bit weight of the DDS system is reduced to 1/8 (see Figure 6). This bit weight corresponds to a VCO output frequency of  $(f_{ref}/8) \times N$ . Depending on the MODE terminal's (terminal 11) logic level, the internal mode select logic loads the frequency register with either the DDS\_0 or DDS\_1 frequency (see Figure 5 and Figure 6).



**Figure 6. Implementation of the DDS Frequency and FSK Frequency Deviation in the DDS Frequency Register**

The VCO output frequency,  $f_{out}$ , which is dependent on the DDS\_x frequency settings (DDS\_0 in the A-word or DDS\_1 in the B-word), can be calculated as follows:

$$f_{out} = DDS\_x \times N \times \frac{f_{ref}}{2^{24}} = N \times \frac{f_{ref} \times DDS\_x}{2^{24}}$$

If FSK modulation is selected (MM=0; C-Word, bit 16), then the 8-bit FSK deviation register can be used to program the frequency deviation of the 2-FSK modulation. Figure 6 illustrates where the 8 bits of the FSK deviation register map into the 24-bit DDS frequency register. Since the two LSBs are set to 0, the total FSK deviation can be determined as follows:

$$\Delta f_{2-FSK} = N \times \frac{DEV \times f_{ref}}{2^{22}}$$

Hence, the 2-FSK frequency, set by the level on the TX\_DATA is calculated as follows:

$$f_{out1:TX\_DATA=Low} = N \times \frac{f_{ref} \times DDS\_x}{2^{24}} \quad f_{out2:TX\_DATA=High} = N \times \frac{f_{ref} \times (DDS\_x + 4 \times DEV)}{2^{24}}$$

This frequency modulated output signal is used as a reference input signal for the PLL circuit. Channel width (frequency deviation) for 2-FSK modulation and channel spacing are software programmable. The minimum channel width and minimum channel spacing depend on the RF system frequency plan.

# TRF4900 SINGLE-CHIP RF TRANSMITTER

SLWS092G – JULY 2000 – REVISED FEBRUARY 2005

## TRF4900 direct digital synthesizer implementation (continued)

Note that the frequencies  $f_{out1}$  and  $f_{out2}$  are centered about the frequency  $f_{center} = (f_{out1} + f_{out2})/2$ . When transmitting FSK,  $f_{center}$  is considered to be the effective carrier frequency and any receiver local oscillator (LO) should be set to the same  $f_{center}$  frequency  $\pm$  the receiver's IF frequency ( $f_{IF}$ ) for proper reception and demodulation.

For the case of low-side injection, the receiver LO would be set to  $f_{LO} = f_{center} - f_{IF}$ . Conversely, for high-side injection, the receiver LO would be set to  $f_{LO} = f_{center} + f_{IF}$ .

Since the DDS registers are static, preprogrammed values are retained during standby mode. This feature greatly reduces turnon time, reduces current consumption when coming out of standby mode, and enables fast lock-times. The PLL lock-times ultimately determine when data can be transmitted or received.

## phase-locked loop

The phase-locked loop (PLL) of the TRF4900 consists of a phase detector (PD) and a frequency acquisition aid (FD) (including two charge pumps), an external loop filter, voltage-controlled oscillator (VCO), and a programmable fixed prescaler (N-divider) in the feedback loop (see Figure 7).

The PLL as implemented in the TRF4900 multiplies the DDS output frequency and further suppresses the unwanted spurious signals produced by the direct digital synthesizer.

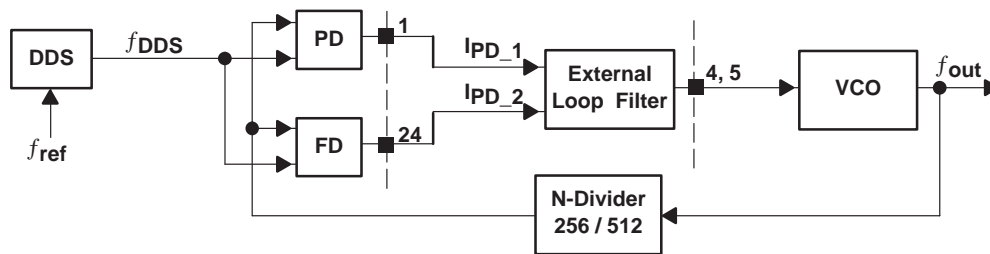


Figure 7. Basic PLL Structure

## VCO

A modified Colpitts oscillator architecture with an external resonant circuit is used for the TRF4900. The internal bias current network adjusts the signal amplitude of the VCO. This allows a wide range of Q-factors (30...60) for the external tank circuit.

The VCO can be bypassed by applying an external RF signal at VCO\_TANK2, terminal 5. To drive the internal PLL and power amplifier, a typical level of  $-10$  dBm should be applied. When an external VCO is used, the  $x\_VCO$  bit should be set to 0.

## phase detector and charge pumps

The TRF4900 contains two charge pumps for locking to the desired frequency: one for coarse tuning of the frequency differences (called the frequency acquisition aid) and one for fine tuning of the phase differences (used in conjunction with the phase detector).

The XOR phase detector and charge pumps produce a mean output current that is proportional to the phase difference between the reference frequency and the VCO frequency divided by  $N$ ;  $N = 256$  or  $512$ . The TRF4900 generates the current pulses  $I_{PD\_1}$  during normal operation (PLL locked).

An additional slip detector and acquisition aid charge pump generates current pulses at terminal PD\_OUT2 during the lock-in of the PLL. This charge pump is turned off when the PLL locks in order to reduce current consumption. The multiplication factor of the acquisition aid current  $I_{PD\_2}$  can be programmed by three bits (APLL) in the C-word.

### phase detector and charge pumps (continued)

The slip detector output, PD\_OUT2, at terminal 24 should be connected directly to the loop filter capacitor C<sub>1</sub>, as shown in Figure 10. The nominal charge pump current I<sub>0</sub> is determined by the external resistor R<sub>PD</sub>, connected to terminal 3, and can be calculated as follows:

$$I_0 = \frac{7V}{R_{PD}}$$

During normal operation (PLL locked), the acquisition aid charge pump is disabled and the maximum charge pump current I<sub>PD\_1</sub> is determined by the nominal value I<sub>0</sub> (see Figure 8).



Figure 8. Normal Operation Charge Pump Current, I<sub>PD\_1</sub>

Each time the PLL is in an unlocked condition, the acquisition aid charge pump generates current pulses I<sub>PD\_2</sub>. The I<sub>PD\_2</sub> current pulses are APLL times larger than I<sub>0</sub> (see Figure 9).

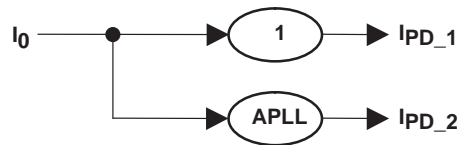


Figure 9. Acquisition Aid, I<sub>PD\_2</sub>, and Normal Operation, I<sub>PD\_1</sub>, Charge Pump Currents

### programmable divider

The internal divider ratio, N, can be set to 256 or 512 via the C-word. Since a higher divider ratio adds additional noise within the multiplication loop, the lowest divider ratio possible for the target application should be used.

### loop filter

Loop filter designs are a balance between lock-time, noise, and spurious suppression. For the TRF4900, common loop filter design rules can be used to determine an appropriate low-pass filter. Standard formulas can be used as a first approach to calculate a basic loop filter. Figure 10 illustrates a basic 3<sup>rd</sup>-order loop filter.

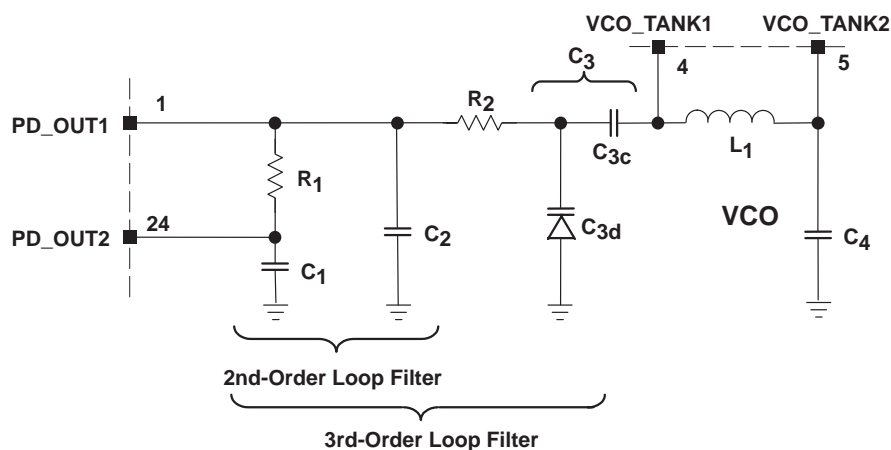


Figure 10. Basic 3<sup>rd</sup>-Order Loop Filter Structure

# TRF4900 SINGLE-CHIP RF TRANSMITTER

SLWS092G – JULY 2000 – REVISED FEBRUARY 2005

## loop filter (continued)

For maximum suppression of the unwanted frequency components, the loop filter bandwidth should generally be made as narrow as possible. At the same time, the filter bandwidth has to be wide enough to allow for the 2-FSK modulation and appropriate lock-time. A detailed simulation of the phase-locked loop should be performed and later verified on PCB implementations.

## power amplifier

The power amplifier (PA) can be programmed via two bits (P0 and P1 in the D-word) to provide varying output power levels. Several control loops are implemented internally to set the output power and to minimize the sensitivity of the power amplifier to temperature, load impedance, and power supply variations. The output stage of the PA usually operates in Class-C and enables easy impedance matching. PA\_OUT, terminal 22, is an open collector output terminal.

CH1 S22

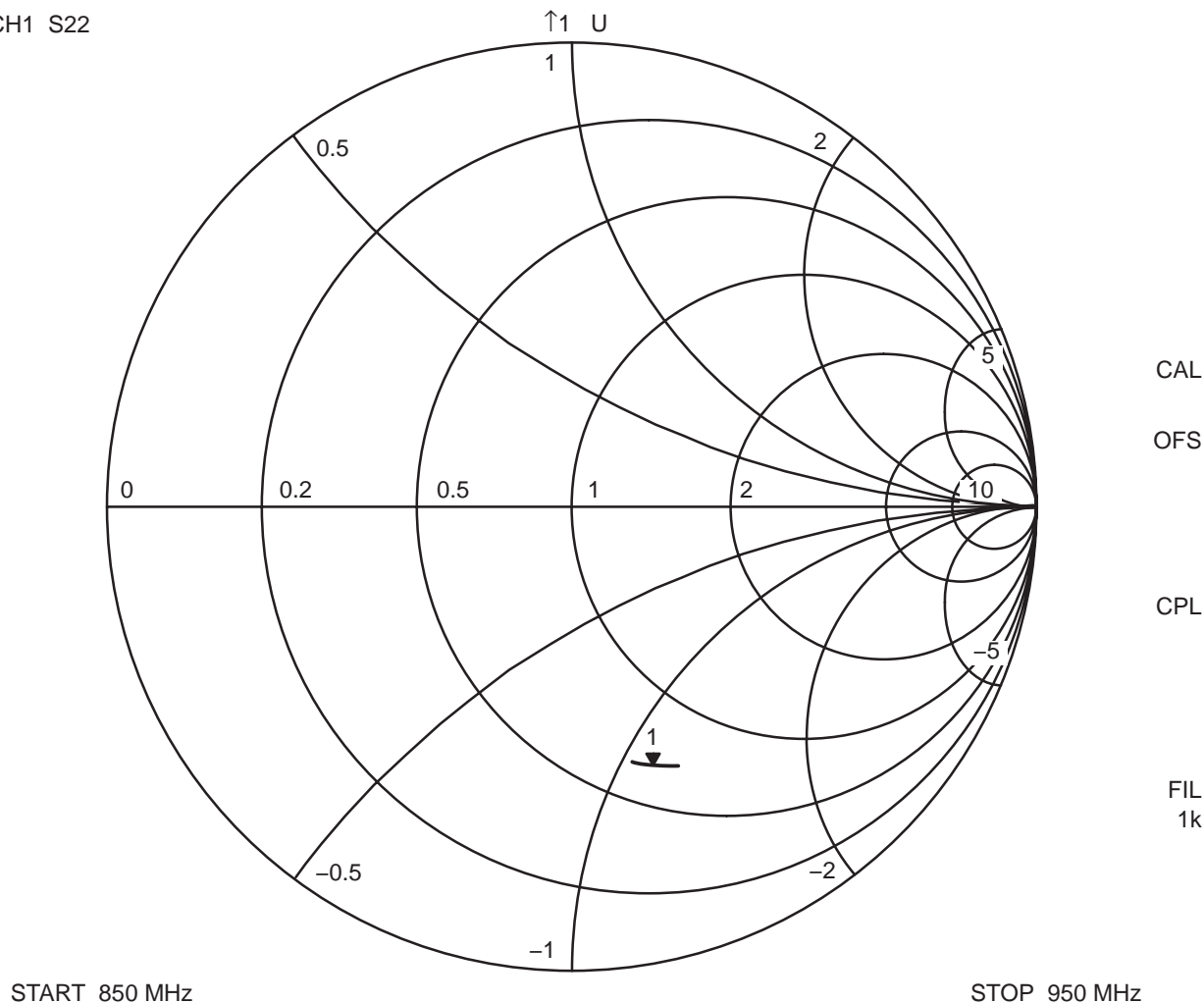


Figure 11. Power Amplifier Output Impedance (S22) at Device Terminal 22

## PRINCIPLES OF OPERATION

### serial control interface

A 3-wire unidirectional serial bus (CLOCK, DATA, STROBE) is used to program the TRF4900 (see Figure 12). The internal registers contain all user programmable variables including the DDS frequency setting registers, as well as all control registers.

At each rising edge of the CLOCK signal, the logic value on the DATA terminal is written into a 24-bit shift register. Setting the STROBE terminal high loads the programmed information into the selected latch. While the STROBE signal is high, the DATA and CLOCK lines must be low (see Figure 2). Since the CLOCK and STROBE signals are asynchronous, care should be taken to ensure the signals remain free of glitches and noise.

As additional leading bits are ignored, only the least significant 24 bits are serial-clocked into the shift register. Due to the static CMOS design, the serial interface consumes virtually no current and it can be programmed in active as well as in standby mode.

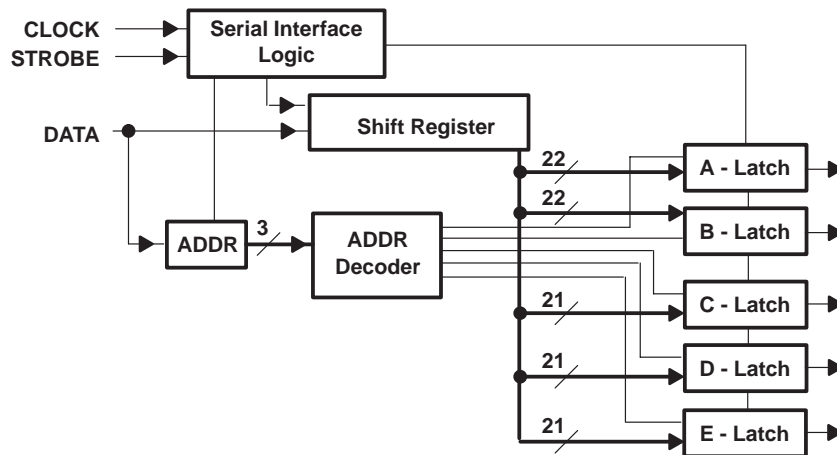


Figure 12. Serial Interface Block Diagram

The control words are 24 bits in length. The first incoming bit functions as the most significant bit (MSB).

To fully program the TRF4900, four 24-bit words must be sent: the A-, B-, C-, and D-words. If individual bits within a word are to be changed, then it is sufficient to program only the appropriate 24-bit word.

Figure 13 shows the definition of the control words. Tables 1, 2, and 3 describe the function of each parameter.

The E-Latch, addressed by an ADDR equal to 111, is reserved for test purposes and should not be used. Inadvertently addressing the E-Latch activates the test modes of the TRF4900.

If the test mode has been inadvertently activated, it can only be exited by switching  $V_{CC}$  on and off or by clearing the E-Latch. The E-Latch can be cleared by addressing it and resetting its entire contents by programming 1110 0000 0000 0000 0000 0000.

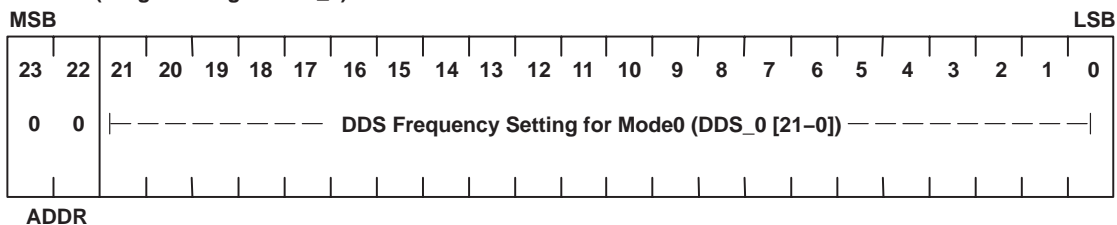
As part of a proper power-up sequence, it is recommended to clear the E-Latch each time  $V_{CC}$  is applied before starting further operations with the TRF4900.

# TRF4900 SINGLE-CHIP RF TRANSMITTER

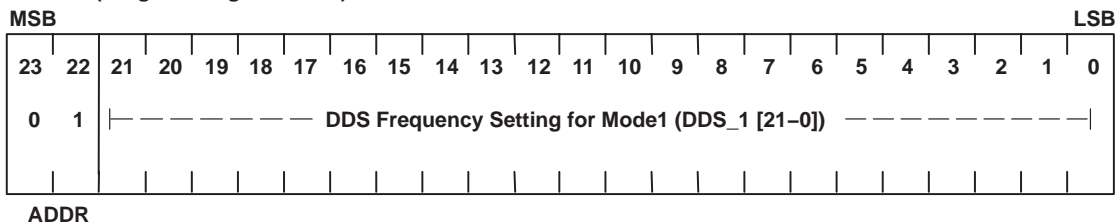
SLWS092G – JULY 2000 – REVISED FEBRUARY 2005

## PRINCIPLES OF OPERATION

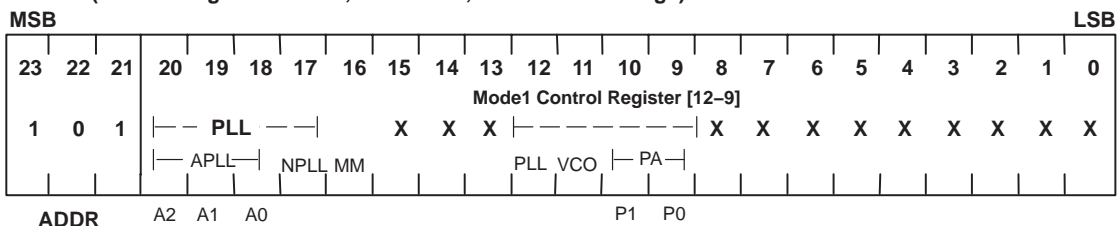
### A-Word (Programming of DDS\_0)



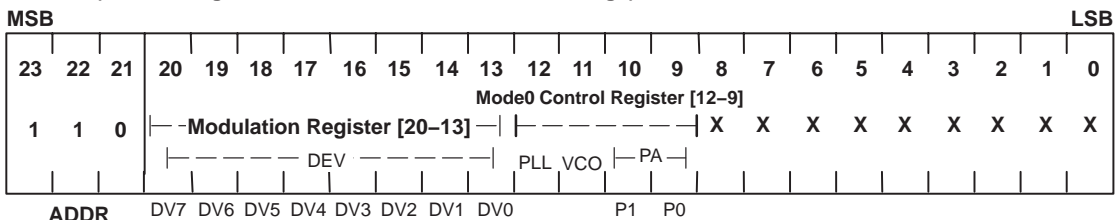
### B-Word (Programming of DDS\_1)



### C-Word (Control Register for PLL, Data Slicer, and Mode1 Settings)



### D-Word (Control Register for Modulation and Mode0 Settings)



NOTE: Start programming with MSB and ensure that the CLOCK and DATA lines are low during the rising edge of the strobe signal.

Figure 13. Serial Control Word Format



**PRINCIPLES OF OPERATION**

**Table 1. Mode0 Control Register Description (D-Word)**

| SYMBOL | BIT LOCATION | NUMBER OF BITS | DESCRIPTION   | INITIAL SETTINGS AFTER POWER UP |               |
|--------|--------------|----------------|---|---------------------------------|---------------|
|        |              |                |   | DEFAULT STATE                   | DEFAULT VALUE |
| 0_PA   | [10–9]       | 2              | Power amplifier mode<br><br><b>P1 P0</b><br>0 0 = disabled<br>0 1 = 10-dB attenuation, enable modulation via TX_DATA<br>1 0 = 20-dB attenuation, enable modulation via TX_DATA<br>1 1 = 0-dB attenuation, enable modulation via TX_DATA | Disabled                        | 00b           |
| 0_VCO  | [11]         | 1              | During operation, this bit should always be enabled (1 = enabled), unless an external VCO is used.  | Disabled                        | 0b            |
| 0_PLL  | [12]         | 1              | Enable PLL (DDS system, VCO, RF divider, phase comparator and charge pump)<br><br>1 = enabled<br>0 = disabled   | Disabled                        | 0b            |

**Table 2. Mode1 Control Register Description (C-Word)**

| SYMBOL | BIT LOCATION | NUMBER OF BITS | DESCRIPTION   | INITIAL SETTINGS AFTER POWER UP |               |
|--------|--------------|----------------|---|---------------------------------|---------------|
|        |              |                |   | DEFAULT STATE                   | DEFAULT VALUE |
| 1_PA   | [10–9]       | 2              | Power amplifier mode<br><br><b>P1 P0</b><br>0 0 = disabled<br>0 1 = 10-dB attenuation, enable modulation via TX_DATA<br>1 0 = 20-dB attenuation, enable modulation via TX_DATA<br>1 1 = 0-dB attenuation, enable modulation via TX_DATA | Disabled                        | 00b           |
| 1_VCO  | [11]         | 1              | During operation, this bit should always be enabled (1 = enabled), unless an external VCO is used.  | Disabled                        | 0b            |
| 1_PLL  | [12]         | 1              | Enable PLL (DDS system, VCO, RF divider, phase comparator and charge pump)<br><br>1 = enabled<br>0 = disabled   | Disabled                        | 0b            |

# TRF4900 SINGLE-CHIP RF TRANSMITTER

SLWS092G – JULY 2000 – REVISED FEBRUARY 2005

## PRINCIPLES OF OPERATION

**Table 3. Miscellaneous Control Register Description**

| SYMBOL    | WORD      | BIT LOCATION | NUMBER OF BITS | DESCRIPTION  | INITIAL SETTINGS AFTER POWER UP |               |           |   |  |   |   |   |   |   |   |   |   |   |    |   |   |   |   |    |   |   |   |   |    |  |  |   |  |  |   |   |   |   |     |   |      |
|-----------|-----------|--------------|----------------|--|---------------------------------|---------------|-----------|---|--|---|---|---|---|---|---|---|---|---|----|---|---|---|---|----|---|---|---|---|----|--|--|---|--|--|---|---|---|---|-----|---|------|
|           |           |              |                |  | DEFAULT STATE                   | DEFAULT VALUE |           |   |  |   |   |   |   |   |   |   |   |   |    |   |   |   |   |    |   |   |   |   |    |  |  |   |  |  |   |   |   |   |     |   |      |
| DDS_0     | A-word    | [21–0]       | 22             | DDS frequency setting in Mode0   | 0                               | All 0s        |           |   |  |   |   |   |   |   |   |   |   |   |    |   |   |   |   |    |   |   |   |   |    |  |  |   |  |  |   |   |   |   |     |   |      |
| DDS_1     | B-word    | [21–0]       | 22             | DDS frequency setting in Mode1   | 0                               | All 0s        |           |   |  |   |   |   |   |   |   |   |   |   |    |   |   |   |   |    |   |   |   |   |    |  |  |   |  |  |   |   |   |   |     |   |      |
| DEV       | D-word    | [20–13]      | 8              | FSK frequency deviation register   | 0                               | All 0s        |           |   |  |   |   |   |   |   |   |   |   |   |    |   |   |   |   |    |   |   |   |   |    |  |  |   |  |  |   |   |   |   |     |   |      |
| APLL      | C-word    | [20–18]      | 3              | Acceleration factor for the frequency acquisition aid charge pump<br><table style="margin-left: 20px; border-collapse: collapse;"> <tr> <td style="padding-right: 10px;"><b>A2</b></td> <td style="padding-right: 10px;"><b>A1</b></td> <td style="padding-right: 10px;"><b>A0</b></td> <td style="padding-left: 10px;">=</td> <td></td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>=</td> <td>1</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>=</td> <td>20</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>=</td> <td>40</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>=</td> <td>60</td> </tr> <tr> <td></td> <td></td> <td style="text-align: center;">⋮</td> <td></td> <td></td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>=</td> <td>140</td> </tr> </table> | <b>A2</b>                       | <b>A1</b>     | <b>A0</b> | = |  | 0 | 0 | 0 | = | 1 | 0 | 0 | 1 | = | 20 | 0 | 1 | 0 | = | 40 | 0 | 1 | 1 | = | 60 |  |  | ⋮ |  |  | 1 | 1 | 1 | = | 140 | 0 | 000b |
| <b>A2</b> | <b>A1</b> | <b>A0</b>    | =              |  |                                 |               |           |   |  |   |   |   |   |   |   |   |   |   |    |   |   |   |   |    |   |   |   |   |    |  |  |   |  |  |   |   |   |   |     |   |      |
| 0         | 0         | 0            | =              | 1  |                                 |               |           |   |  |   |   |   |   |   |   |   |   |   |    |   |   |   |   |    |   |   |   |   |    |  |  |   |  |  |   |   |   |   |     |   |      |
| 0         | 0         | 1            | =              | 20   |                                 |               |           |   |  |   |   |   |   |   |   |   |   |   |    |   |   |   |   |    |   |   |   |   |    |  |  |   |  |  |   |   |   |   |     |   |      |
| 0         | 1         | 0            | =              | 40   |                                 |               |           |   |  |   |   |   |   |   |   |   |   |   |    |   |   |   |   |    |   |   |   |   |    |  |  |   |  |  |   |   |   |   |     |   |      |
| 0         | 1         | 1            | =              | 60   |                                 |               |           |   |  |   |   |   |   |   |   |   |   |   |    |   |   |   |   |    |   |   |   |   |    |  |  |   |  |  |   |   |   |   |     |   |      |
|           |           | ⋮            |                |  |                                 |               |           |   |  |   |   |   |   |   |   |   |   |   |    |   |   |   |   |    |   |   |   |   |    |  |  |   |  |  |   |   |   |   |     |   |      |
| 1         | 1         | 1            | =              | 140  |                                 |               |           |   |  |   |   |   |   |   |   |   |   |   |    |   |   |   |   |    |   |   |   |   |    |  |  |   |  |  |   |   |   |   |     |   |      |
| NPLL      | C-word    | [17]         | 1              | PLL divider ratio<br>0 = divide by 256<br>1 = divide by 512  | 256                             | 0b            |           |   |  |   |   |   |   |   |   |   |   |   |    |   |   |   |   |    |   |   |   |   |    |  |  |   |  |  |   |   |   |   |     |   |      |
| MM        | C-word    | [16]         | 1              | Modulation mode select. Sets the behavior of terminal TX_DATA to FSK data input.<br>0 = FSK/FM<br>1 = do not use   | FSK mode                        | 0b            |           |   |  |   |   |   |   |   |   |   |   |   |    |   |   |   |   |    |   |   |   |   |    |  |  |   |  |  |   |   |   |   |     |   |      |

### operating modes

Table 4 and Table 5 illustrate operating modes and transmit frequencies as set by the  $\overline{\text{STDBY}}$ , MODE, and TX\_DATA terminals used in conjunction with the DDS frequency settings.

**Table 4. Transmitting Data in FSK Mode (MM bit set to 0)**

| TERMINAL                  |      |         | TRANSMIT FREQUENCY  |
|---------------------------|------|---------|---|
| $\overline{\text{STDBY}}$ | MODE | TX_DATA |   |
| 1                         | 0    | 0       | $f_{\text{out}} = f_{\text{ref}} \times N \times (\text{DDS}_0)/2^{24}$                       |
| 1                         | 0    | 1       | $f_{\text{out}} = f_{\text{ref}} \times N \times (\text{DDS}_0 + 4 \times \text{DEV})/2^{24}$ |
| 1                         | 1    | 0       | $f_{\text{out}} = f_{\text{ref}} \times N \times (\text{DDS}_1)/2^{24}$                       |
| 1                         | 1    | 1       | $f_{\text{out}} = f_{\text{ref}} \times N \times (\text{DDS}_1 + 4 \times \text{dev})/2^{24}$ |



PRINCIPLES OF OPERATION

operating modes (continued)

Table 5. Operating Mode Per  $\overline{\text{STDBY}}$  Terminal

| STDBY | OPERATING MODE                                      |
|-------|---|
| 0     | Standby/programming mode – Power down of all blocks |
| 1     | Operating mode and programming mode                 |

Two independent operating modes, Mode0 and Mode1, allow extremely fast switching between two preprogrammed settings by toggling the MODE terminal. Each mode can be viewed as a bank of configuration registers which store the frequency settings and the enable/disable settings for each functional block of the TRF4900. The MODE terminal is then used to asynchronously switch between Mode0 and Mode1 as shown in Figure 14. Table 6 shows several examples of operating sequences.

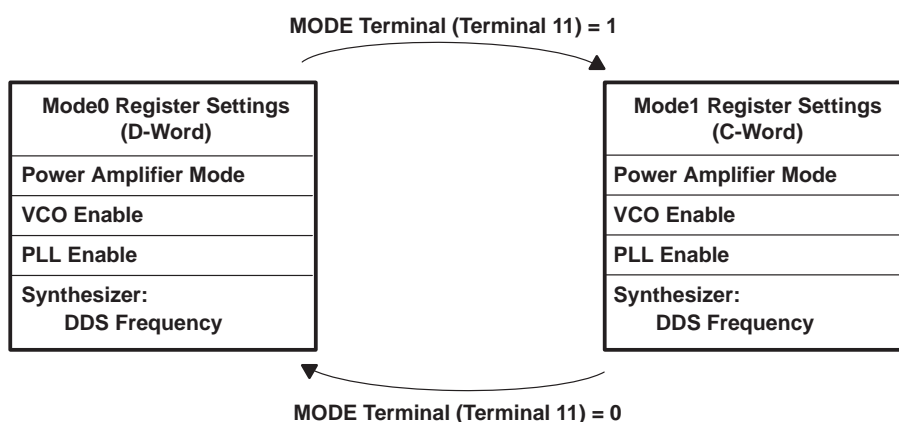


Figure 14. Interaction Between MODE Terminal and Preprogrammed Mode0 and Mode1 Control Registers

Table 6. Operating Mode Examples

| FUNCTION / DESCRIPTION  | MODE0                   | MODE1                               |
|---|-------------------------|-------------------------------------|
| Transmit on two different frequencies                                   | Transmit on frequency 0 | Transmit on frequency 1             |
| Emulate FSK transmit operation using the MODE terminal for wideband FSK | Transmit on frequency 0 | Transmit on frequency 0 + deviation |

# TRF4900 SINGLE-CHIP RF TRANSMITTER

SLWS092G – JULY 2000 – REVISED FEBRUARY 2005

## APPLICATION INFORMATION

A typical application schematic for an FSK system operating in the European 868-MHz to 870-MHz ISM band is shown in Figure 15. If the TRF4900 is left on for long periods of time without going into standby mode, a 100-Ω resistor to ground should be added at terminal 4 or terminal 5 to reduce tuning voltage drift as in Figure 16. If the 100-Ω resistor is present, C2 and C4 may be changed to adjust the tuning range as needed. Since most EU applications involve relatively short periods of transmission, the 100-Ω resistor is left off in the schematic shown in Figure 15.

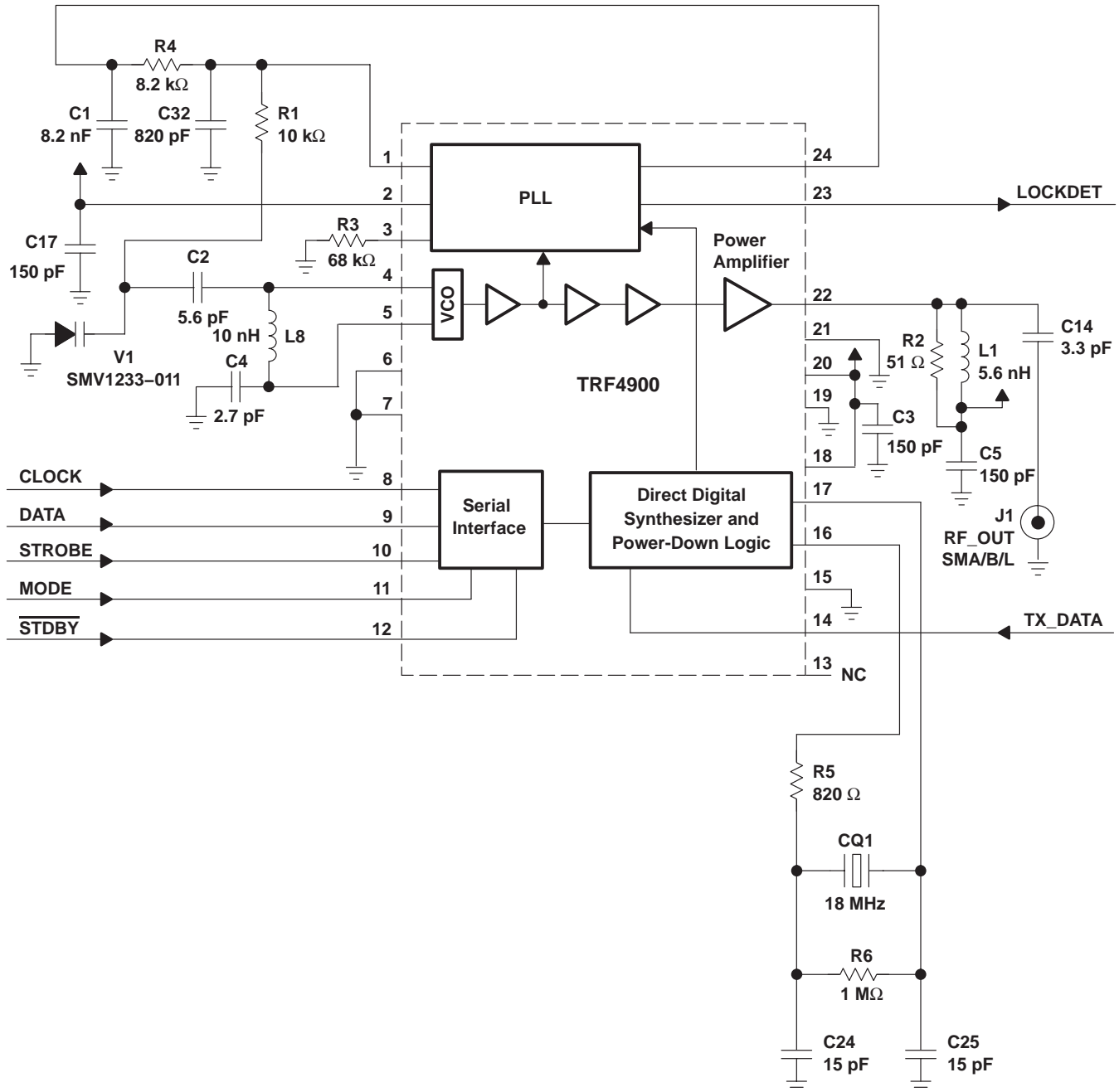


Figure 15. Typical Application Schematic for 868-MHz to 870-MHz European ISM Band

**APPLICATION INFORMATION**

**external component list for Figure 15 (5% tolerance unless otherwise noted)**

| DESIGNATOR | DESCRIPTION (SIZE) | VALUE       | MANUFACTURER            | PART NUMBER/COMMENTS |
|------------|--------------------|-------------|-------------------------|----------------------|
| C1         | Capacitor          | 8.2 pF      |                         |                      |
| C2         | Capacitor          | 5.6 pF      |                         |                      |
| C3         | Capacitor          | 150 pF      |                         |                      |
| C4         | Capacitor          | 2.7 pF      |                         |                      |
| C5         | Capacitor          | 150 pF      |                         |                      |
| C14        | Capacitor          | 3.3 pF      |                         |                      |
| C17        | Capacitor          | 150 pF      |                         |                      |
| C24        | Capacitor          | 15 pF       |                         |                      |
| C25        | Capacitor          | 15 pF       |                         |                      |
| C32        | Capacitor          | 820 pF      |                         |                      |
| L1         | Coil               | 5.6 nH      | Murata                  | LQN21A6N8D04         |
| L8         | Coil               | 10 nH       | Murata                  | LQW1608              |
| R1         | Resistor           | 10 kΩ       |                         |                      |
| R2         | Resistor           | 51 Ω        |                         |                      |
| R3         | Resistor           | 68 kΩ       |                         |                      |
| R4         | Resistor           | 8.2 kΩ      |                         |                      |
| R5         | Resistor           | 820 Ω       |                         |                      |
| R6         | Resistor           | 1 MΩ        |                         |                      |
| V1         | Varactor diode     | SMV1233-011 | Alpha Industries        |                      |
| CQ1        | Crystal            | 18 MHz      | CMAC Frequency Products | CX-1 SMI             |

# TRF4900 SINGLE-CHIP RF TRANSMITTER

SLWS092G – JULY 2000 – REVISED FEBRUARY 2005

## APPLICATION INFORMATION

A typical application schematic for an FSK system operating in the North American 902-MHz to 928-MHz ISM band as shown in Figure 16.

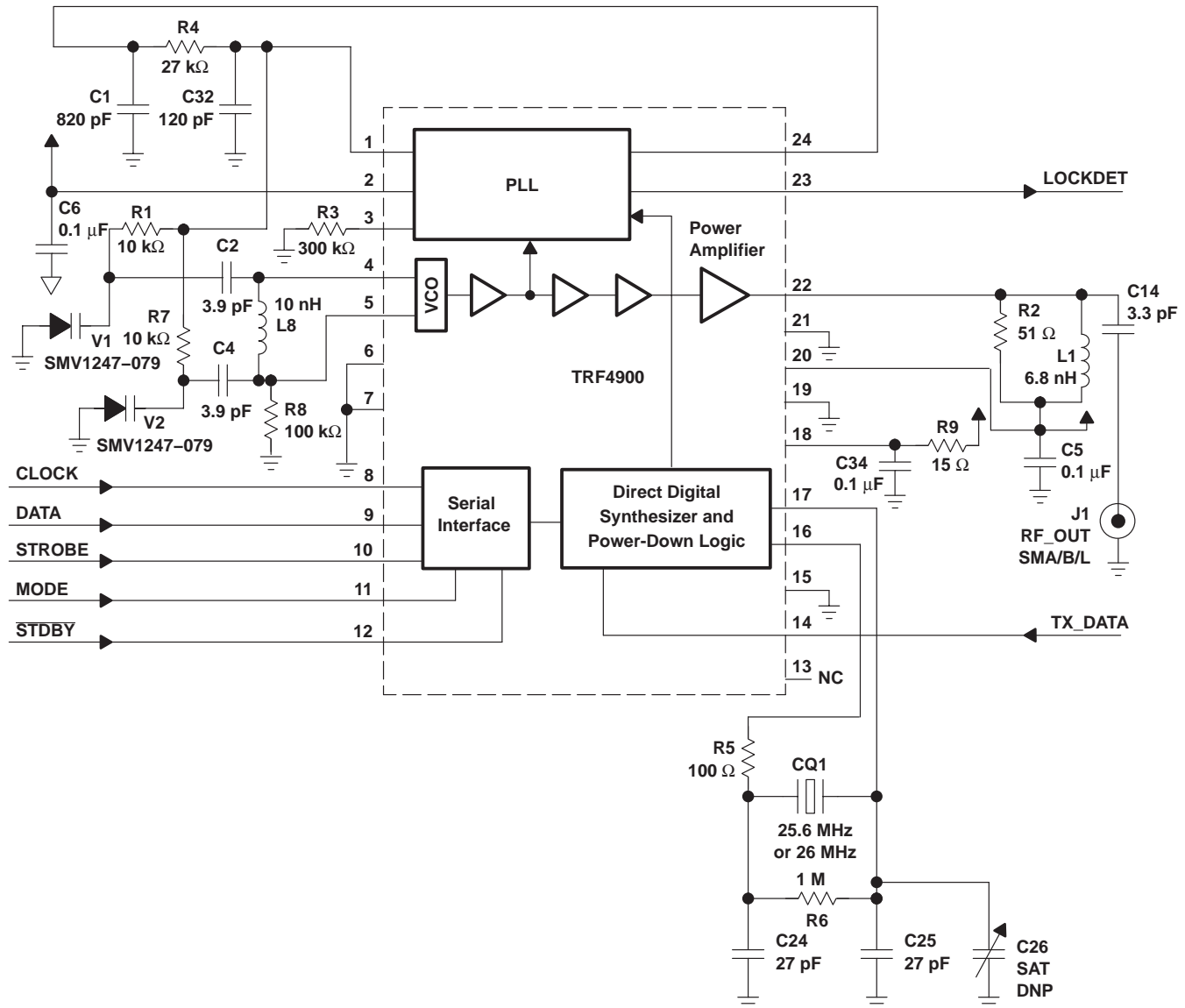


Figure 16. Typical Application Schematic for 902-MHz to 928-MHz North American ISM Band

**APPLICATION INFORMATION**

**external component list for Figure 16 (5% tolerance unless otherwise noted)**

| DESIGNATOR | DESCRIPTION (SIZE) | VALUE                 | MANUFACTURER   | PART NUMBER/COMMENTS                     |
|------------|--------------------|-----------------------|--|--|
| C1         | Capacitor          | 820 pF                |  |  |
| C2         | Capacitor          | 3.9 pF                |  |  |
| C4         | Capacitor          | 3.9 pF                |  |  |
| C5         | Capacitor          | 0.1 μF                |  |  |
| C6         | Capacitor          | 0.1 μF                |  |  |
| C14        | Capacitor          | 3.3 pF                |  |  |
| C24        | Capacitor          | 27 pF                 |  |  |
| C25        | Capacitor          | 27 pF                 |  |  |
| C26        | Capacitor          |                       |  | Select at test (SAT), Do not place (DNP) |
| C32        | Capacitor          | 120 pF                |  |  |
| C34        | Capacitor          | 0.1 μF                |  |  |
| L1         | Coil               | 6.8 nH                | Murata   | LQN21A6N8D04                             |
| L8         | Coil               | 10 nH                 | Murata   | LQW1608                                  |
| R1         | Resistor           | 10 kΩ                 |  |  |
| R2         | Resistor           | 51 Ω                  |  |  |
| R3         | Resistor           | 300 kΩ                |  |  |
| R4         | Resistor           | 27 kΩ                 |  |  |
| R5         | Resistor           | 100 Ω                 |  |  |
| R6         | Resistor           | 1 MΩ                  |  |  |
| R7         | Resistor           | 10 kΩ                 |  |  |
| R8         | Resistor           | 100 kΩ                |  |  |
| R9         | Resistor           | 15 Ω                  |  |  |
| V1, V2     | Varactor diode     | SMV1247-079           | Alpha Industries   |  |
| CQ1        | Crystal            | 25.6 MHz or<br>26 MHz | ICM (International Crystal<br>Manufacturing, Incorporated) | 865842: 25.6 MHz<br>865850: 26 MHz       |

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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| Interface        | <a href="http://interface.ti.com">interface.ti.com</a>             | Digital Control     | <a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a> |
| Logic            | <a href="http://logic.ti.com">logic.ti.com</a>                     | Military            | <a href="http://www.ti.com/military">www.ti.com/military</a>             |
| Power Mgmt       | <a href="http://power.ti.com">power.ti.com</a>                     | Optical Networking  | <a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a> |
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|                  |  | Telephony           | <a href="http://www.ti.com/telephony">www.ti.com/telephony</a>           |
|                  |  | Video & Imaging     | <a href="http://www.ti.com/video">www.ti.com/video</a>                   |
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