DUAL SUPPLY, LOW ON-STATE RESISTANCE SPST CMOS ANALOG SWITCHES

FEATURES

- **±1-V to ±6-V Dual-Supply Operation**
- **Specified ON-State Resistance:**
  - **25 Ω Max With ±5-V Supply**
  - **35 Ω Max With ±3.3-V Supply**
  - **47 Ω Max With ±1.8-V Supply**
- **Specified Low OFF-Leakage Currents:**
  - **5 nA at 25°C**
  - **10 nA at 85°C**
- **Specified Low ON-Leakage Currents:**
  - **5 nA at 25°C**
  - **10 nA at 85°C**
- **Low Charge Injection: 13 pC (±5-V Supply)**
- **Fast Switching Speed:**
  t_{ON} = 85 ns, t_{OFF} = 50 ns (±5-V Supply)
- **Break-Before-Make Operation ($t_{ON} > t_{OFF}$)**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2500-V Human-Body Model (A114-F)**
  - **1000-V Charged-Device Model (C101-C)**
  - **250-V Machine Model (A115-A)**

DESCRIPTION/ORDERING INFORMATION

The TS12A4516/TS12A4517 are single pole/single throw (SPST), low-voltage, dual-supply CMOS analog switches, with very low switch ON-state resistance. The TS12A4516 is normally open (NO). The TS12A4517 is normally closed (NC).

These CMOS switches can operate continuously with a dual supplies between ±1 V and ±6 V [(2 V < (V_+ – V_-) < 12 V]. Each switch can handle rail-to-rail analog signals. The OFF-leakage current maximum is only 5 nA at 25°C or 10 nA at 85°C.

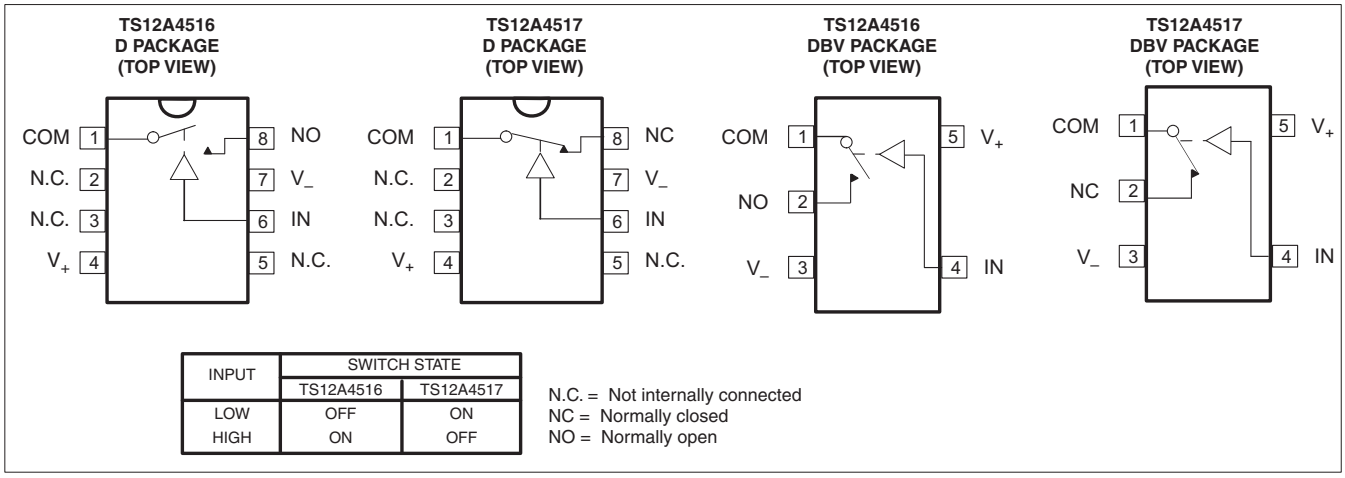
For pin-compatible parts for use with single supply, see the TS12A4514/TS12A4515.

ORDERING INFORMATION

T_A	PACKAGE(1)(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – D	Reel of 1500	TS12A4516D	YD516
		Reel of 2500	TS12A4516DR	
	SOP (SOT-23) – DBV	Reel of 3000	TS12A4516DBVR	9CL_
	SOIC – D	Reel of 1500	TS12A4517D	YD517
		Reel of 2500	TS12A4517DR	
	SOP (SOT-23) – DBV	Reel of 3000	TS12A4517DBVR	9CM_

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

PIN CONFIGURATIONS



INPUT	SWITCH STATE	
	TS12A4516	TS12A4517
LOW	OFF	ON
HIGH	ON	OFF

N.C. = Not internally connected
NC = Normally closed
NO = Normally open

Absolute Minimum and Maximum Ratings(1)(2)

voltages referenced to 0 V

			MIN	MAX	UNIT
V_+	Supply voltage range		–0.3	13	V
V_{NC} V_{NO} V_{COM}	Analog voltage range(3)		V_- –0.3	V_+ + 0.3	V
V_{IN}	Logic input range		V_- –0.3	V_+ + 0.3	V
	Continuous current into any terminal			±20	mA
	Peak current, NO or COM (pulsed at 1 ms, 10% duty cycle)			±30	mA
	ESD per method 3015.7			>2000	V
	Continuous power dissipation (T_A = 70°C)	8-pin SOIC (derate 5.88 mW/°C above 70°C)		471	mW
		5-pin SOT23-5 (derate 7.1 mW/°C above 70°C)		571	
T_A	Operating temperature range		–40	85	°C
T_{stg}	Storage temperature range		–65	150	°C
	Lead temperature (soldering, 10 s)			300	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(3) Voltages exceeding V_+ or GND on any signal terminal are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Electrical Characteristics for ±5-V Supply(1)

V_+ = 4.5 V to 5.5 V, V_- = –4.5 V to –5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	MIN	TYP(2)	MAX	UNIT
Analog Switch							
Analog signal range	V_{COM}, V_{NO}, V_{NC}			V_-		V_+	V
ON-state resistance	r_{on}	V_+ = 4.5 V, V_- = –4.5 V, V_{COM} = 3.5 V, I_{COM} = 20 mA	25°C		12	20	Ω
			Full			25	
ON-state resistance flatness	$r_{on(flat)}$	V_+ = 4.5 V, V_- = –4.5 V, V_{COM} = –3.5 V, 0 V, 3.5 V, I_{COM} = 20 mA	25°C		1.2	2.5	Ω
			Full			3	
NO, NC OFF leakage current(3)	$I_{NO(OFF)}$, $I_{NC(OFF)}$	V_+ = 5.5 V, V_- = –5.5 V, V_{COM} = 4.5 V, V_{NO} or V_{NC} = –4.5 V	25°C			5	nA
			Full			10	
COM OFF leakage current(3)	$I_{COM(OFF)}$	V_+ = 5.5 V, V_- = –5.5 V, V_{COM} = –4.5 V, V_{NO} or V_{NC} = 4.5 V	25°C			5	nA
			Full			10	
COM ON leakage current(3)	$I_{COM(ON)}$	V_+ = 5.5 V, V_- = –5.5 V, V_{COM} = 5.5 V, V_{NO} or V_{NC} = open	25°C			5	nA
			Full			10	
Digital Control Input (IN)							
Input logic high	V_{IH}		Full	V_+ – 1.5			V
Input logic low	V_{IL}		Full	V_-		V_+ – 3.5	V
Input leakage current	I_{IH}, I_{IL}	V_{IN} = V_+, 0 V	Full			0.010	µA
Dynamic							
Turn-on time	t_{ON}	See Figure 2	25°C		58	75	ns
			Full			85	
Turn-off time	t_{OFF}	See Figure 2	25°C		28	45	ns
			Full			50	
Charge injection(4)	Q_C	C_L = 1 nF, V_{NO} = 0 V, R_S = 0 Ω, See Figure 1	25°C		–13		pC
NO, NC OFF capacitance	$C_{NO(OFF)}$, $C_{NC(OFF)}$	f = 1 MHz, See Figure 4	25°C		5.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	f = 1 MHz, See Figure 4	25°C		5.5		pF
COM ON capacitance	$C_{COM(ON)}$	f = 1 MHz, See Figure 4	25°C		16		pF
Digital input capacitance	C_I	V_{IN} = V_+, 0 V	25°C		1.5		pF
Bandwidth	BW	R_L = 50 Ω, C_L = 15 pF, V_{NO} = 1 V_{RMS}, f = 100 kHz	25°C		464		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, C_L = 15 pF, V_{NO} = 1 V_{RMS}, f = 1 MHz	25°C		–83		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 15 pF, V_{NO} = 1 V_{RMS}, f = 20 kHz	25°C		0.07		%
Supply							
V_+ supply current	I_+	V_{IN} = 0 V or V_+	25°C			70	µA
			Full			80	
V_- supply current	I_-	V_{IN} = 0 V or V_+	25°C	–70			µA
			Full	–80			

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(2) Typical values are at T_A = 25°C.
(3) Leakage parameters are 100% tested at maximum-rated hot operating temperature, and are ensured by correlation at 25°C.
(4) Specified by design, not production tested

Electrical Characteristics for ±3.3-V Supply(1)

V_+ = 3.0 V to 3.6 V, V_- = –3.0 V to –3.6, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	MIN	TYP(2)	MAX	UNIT
Analog Switch							
Analog signal range	V_{COM}, V_{NO}, V_{NC}			V_-		V_+	V
ON-state resistance	r_{on}	V_+ = 3.0 V, V_- = –3.0 V, V_{COM} = 3 V, I_{COM} = 20 mA	25°C		17	25	Ω
			Full			35	
ON-state resistance flatness	$r_{on(flat)}$	V_{COM} = –2 V, 0 V, 2 V, I_{COM} = 20 mA	25°C		1.5	3	Ω
			Full			4	
NO, NC OFF leakage current(3)	$I_{NO(OFF)}$, $I_{NC(OFF)}$	V_+ = 3.6 V, V_- = –3.6 V, V_{COM} = 3 V, V_{NO} or V_{NC} = –3 V	25°C			5	nA
			Full			10	
COM OFF leakage current(3)	$I_{COM(OFF)}$	V_+ = 3.6 V, V_- = –3.6 V, V_{COM} = –3 V, V_{NO} or V_{NC} = 3 V	25°C			5	nA
			Full			10	
COM ON leakage current(3)	$I_{COM(ON)}$	V_+ = 3.6 V, V_- = –3.6 V, V_{COM} = 3.6 V, V_{NO} or V_{NC} = open	25°C			5	nA
			Full			10	
Digital Control Input (IN)							
Input logic high	V_{IH}		Full	V_+ – 1.5			V
Input logic low	V_{IL}		Full	V_-		V_+ – 3.5	V
Input leakage current	I_{IH}, I_{IL}	V_{IN} = V_+, 0 V	Full			0.01	µA
Dynamic							
Turn-on time	t_{ON}	see Figure 2	25°C		65	85	ns
			Full			95	
Turn-off time	t_{OFF}	see Figure 2	25°C		37	60	ns
			Full			70	
Charge injection(4)	Q_C	C_L = 1 nF, V_{NO} = 0 V, R_S = 0 Ω, See Figure 1	25°C		–7.5		pC
NO, NC OFF capacitance	$C_{NO(OFF)}$ $C_{NC(OFF)}$	f = 1 MHz, See Figure 4	25°C		5.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	f = 1 MHz, See Figure 4	25°C		5.5		pF
COM ON capacitance	$C_{COM(ON)}$	f = 1 MHz, See Figure 4	25°C		16		pF
Digital input capacitance	C_I	V_{IN} = V_+, 0 V	25°C		1.5		pF
Bandwidth	BW	R_L = 50 Ω, C_L = 15 pF, V_{NO} = 1 V_{RMS}, f = 100 kHz	25°C		464		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, C_L = 15 pF, V_{NO} = 1 V_{RMS}, f = 100 kHz	25°C		–83		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 15 pF, V_{NO} = 1 V_{RMS}, f = 20 kHz	25°C		0.10		%
Supply							
V_+ supply current	I_+	V_{IN} = 0 V or V_+	25°C			40	µA
			Full			45	
V_- supply current	I_-	V_{IN} = 0 V or V_+	25°C	–40			µA
			Full	45			

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(2) Typical values are at T_A = 25°C.
(3) Leakage parameters are 100% tested at maximum-rated hot operating temperature, and are ensured by correlation at 25°C.
(4) Specified by design, not production tested

Electrical Characteristics for ±1.8-V Supply(1)

V_+ = 1.65 V to 1.95 V, V_- = –1.65 V to –1.95 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	MIN	TYP(2)	MAX	UNIT
Analog Switch							
Analog signal range	V_{COM}, V_{NO}, V_{NC}			V_-		V_+	V
ON-state resistance	r_{on}	V_+ = 1.65 V, V_- = –1.65 V, V_{COM} = 0 V, I_{COM} = 20 mA	25°C		28	40	Ω
			Full			47	
ON-state resistance flatness	$r_{on(flat)}$	V_+ = 1.65 V, V_- = –1.65 V, V_{COM} = –1.8 V, 0 V, 1.5 V, I_{COM} = 20 mA	25°C		9	13	Ω
			Full			15	
NO, NC OFF leakage current(3)	$I_{NO(OFF)}$, $I_{NC(OFF)}$	V_+ = 1.95 V, V_- = –1.95 V, V_{COM} = 1.65 V, V_{NO} or V_{NC} = –1.65 V	25°C			5	nA
			Full			10	
COM OFF leakage current(3)	$I_{COM(OFF)}$	V_+ = 1.95 V, V_- = –1.95 V, V_{COM} = –1.65 V, V_{NO} or V_{NC} = 1.65 V	25°C			5	nA
			Full			10	
COM ON leakage current(3)	$I_{COM(ON)}$	V_+ = 1.95 V, V_- = –1.95 V, V_{COM} = 1.95 V, V_{NO} or V_{NC} = open	25°C			5	nA
			Full			10	
Digital Control Input (IN)							
Input logic high	V_{IH}		Full	V_+ – 1.5			V
Input logic low	V_{IL}		Full	V_-		V_+ – 3.5	V
Input leakage current	I_{IH}, I_{IL}	V_{IN} = V_+, 0 V	Full			0.01	µA
Dynamic							
Turn-on time(4)	t_{ON}	See Figure 2	25°C		90	120	ns
			Full			150	
Turn-off time(4)	t_{OFF}	See Figure 2	25°C		95	150	ns
			Full			200	
Charge injection(4)	Q_C	C_L = 1 nF, See Figure 1	25°C		–3.5		pC
NO, NC OFF capacitance	$C_{NO(OFF)}$, $C_{NC(OFF)}$	f = 1 MHz, See Figure 4	25°C		6		pF
COM OFF capacitance	$C_{COM(OFF)}$	f = 1 MHz, See Figure 4	25°C		6		pF
COM ON capacitance	$C_{COM(ON)}$	f = 1 MHz, See Figure 4	25°C		14.5		pF
Digital input capacitance	C_I	V_{IN} = V_+, 0 V	25°C		1.5		pF
Bandwidth	BW	R_L = 50 Ω, C_L = 15 pF, V_{NO} = 1 V_{RMS}, f = 100 kHz	25°C		464		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, C_L = 15 pF, V_{NO} = 1 V_{RMS}, f = 1 MHz	25°C		–83		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF, V_{NO} = 1 V_{RMS}, f = 20 kHz	25°C		0.37		%
Supply							
V_+ supply current	I_+	V_{IN} = 0 V or V_+	25°C			20	µA
			Full			30	
V_- supply current	I_-	V_{IN} = 0 V or V_+	25°C	–20			µA
			Full	–30			

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(2) Typical values are at T_A = 25°C.
(3) Leakage parameters are 100% tested at maximum-rated hot operating temperature, and are ensured by correlation at 25°C.
(4) Specified by design, not production tested

PIN DESCRIPTION(1)

PIN NO.				NAME	DESCRIPTION
TS12A4516		TS12A4517			
D, P	SOT23-5	D, P	SOT23-5		
1	1	1	1	COM	Common
2, 3, 5	–	2, 3, 5	–	N.C.	No connect (not internally connected)
4	5	4	5	V_+	Positive power supply
6	4	6	4	IN	Digital control to connect COM to NO or NC
7	3	7	3	V_-	Negative power supply
8	2	–	–	NO	Normally open
–	–	8	2	NC	Normally closed

(1) NO, NC, and COM pins are identical and interchangeable. Any may be considered as an input or an output; signals pass in both directions.

APPLICATION INFORMATION

Power-Supply Considerations

The TS12A4516 and TS12A4517 operate with power-supply voltages from ±1 V to ±6 V [(2 V < (V_+ – V_-) < 12 V], but are tested and specified at ±5V, ±3.3V, and ±1.8V supplies. The pin-compatible TS12A4514 and TS12A4515 are recommended for use when only a single supply is desirable.

The TS12A4516 and TS12A4517 construction is typical of most CMOS analog switches, except that they have only two supply pins: V_+ and V_-. V_+ and V_- drive the internal CMOS switches and set their analog voltage limits. Reverse ESD-protection diodes are internally connected between each analog-signal pin and both V_+ and V_-. One of these diodes conducts if any analog signal exceeds V_+ or V_-.

Virtually all the analog leakage current comes from the ESD diodes to V_+ or V_-. Although the ESD diodes on a given signal pin are identical and, therefore, fairly well balanced, they are reverse biased differently. Each is biased by either V_+ or V_- and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V_+ and V_- pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity.

V_+ and V_- also power the internal logic and logic-level translators. The logic-level translators convert the logic levels to switched V_+ and V_- signals to drive the analog signal gates.

Logic-Level Thresholds

Since these parts have no ground pin, the logic-level threshold is referenced to V_+. The threshold limits are V_+ –1.5 V and V_+ –3.5 V for V_+ levels between 6 V and 3 V. When V_+ = 2 V, the logic threshold is approximately 0.6 V.

CAUTION:

Do not connect the TS12A4516/TS12A4517 V_+ to 3 V and then connect the logic-level pins to logic-level signals that operate from 5-V supply. TTL levels can exceed 3 V and violate the absolute maximum ratings, damaging the part and/or external circuits.

Test Circuits/Timing Diagrams

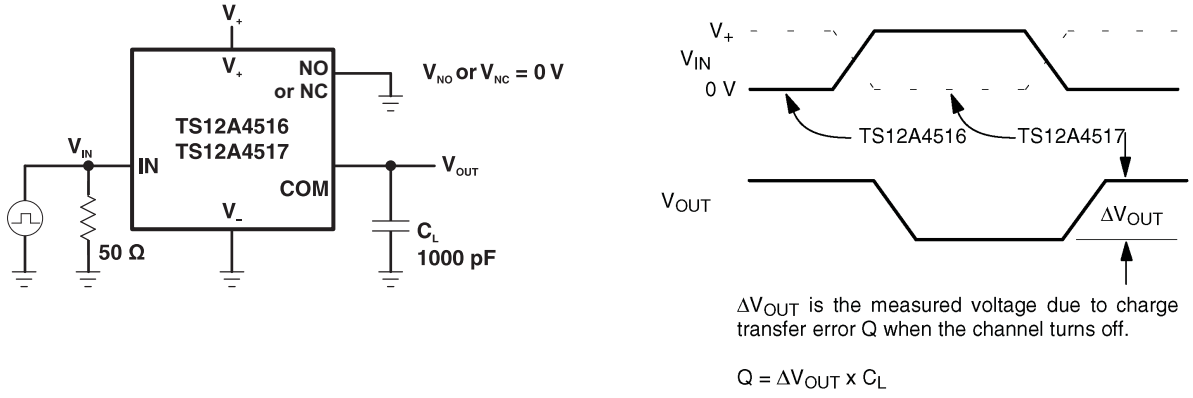


Figure 1. Charge Injection

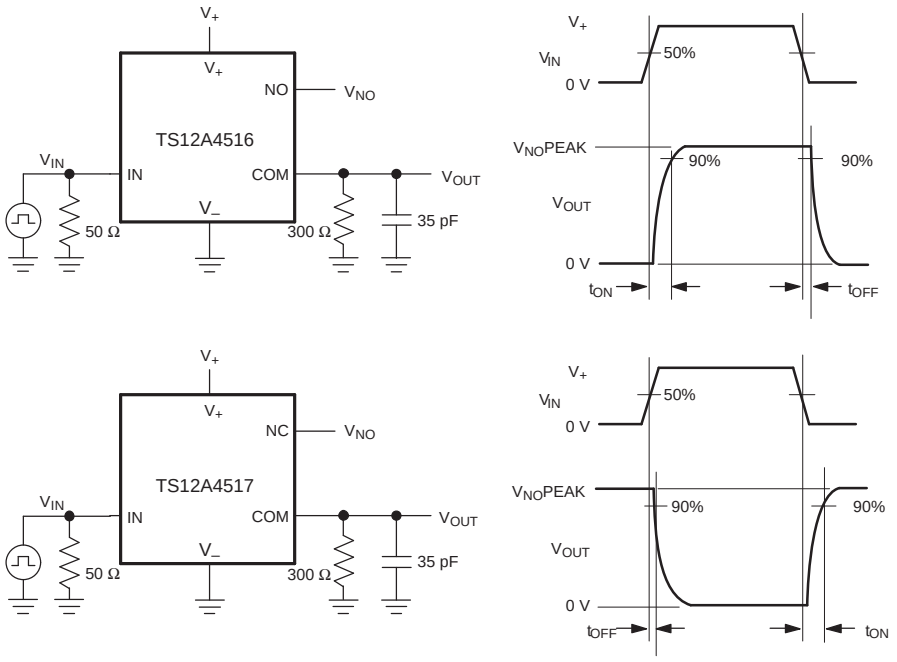
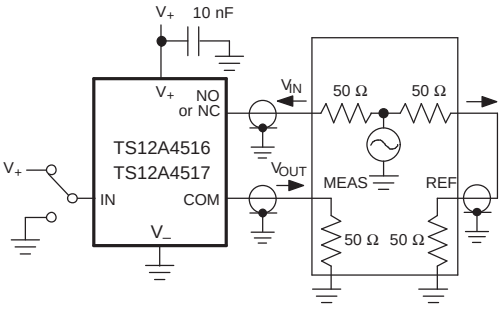


Figure 2. Switching Times



Measurements are standardized against short at socket terminals. OFF isolation is measured between COM and OFF terminals on each switch. ON loss is measured between COM and ON terminals on each switch. Signal direction through switch is reversed; worst values are recorded.

$$\text{OFF Isolation} = 20\log\frac{V_{OUT}}{V_{IN}}$$

$$\text{ON Loss} = 20\log\frac{V_{OUT}}{V_{IN}}$$

Figure 3. OFF Isolation and ON Loss

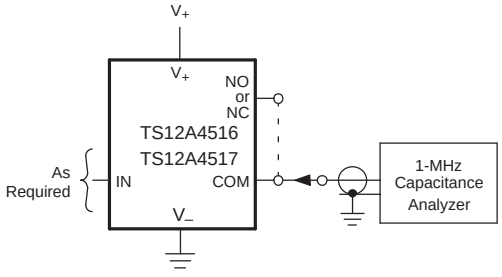


Figure 4. NO, NC, and COM Capacitance

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS12A4516D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YD516	Samples
TS12A4516DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(9CLA ~ 9CLM)	Samples
TS12A4516DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YD516	Samples
TS12A4516DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YD516	Samples
TS12A4517D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YD517	Samples
TS12A4517DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(9CMA ~ 9CMM)	Samples
TS12A4517DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YD517	Samples
TS12A4517DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YD517	Samples
TS12A4517DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	YD517	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

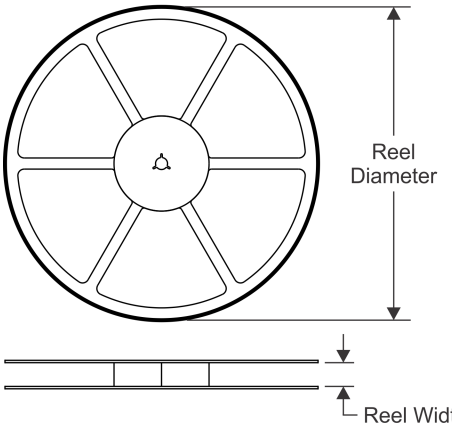
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

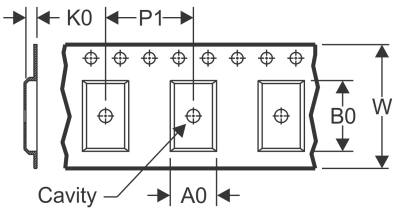
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

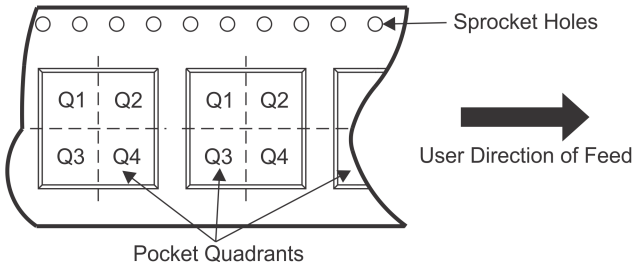


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

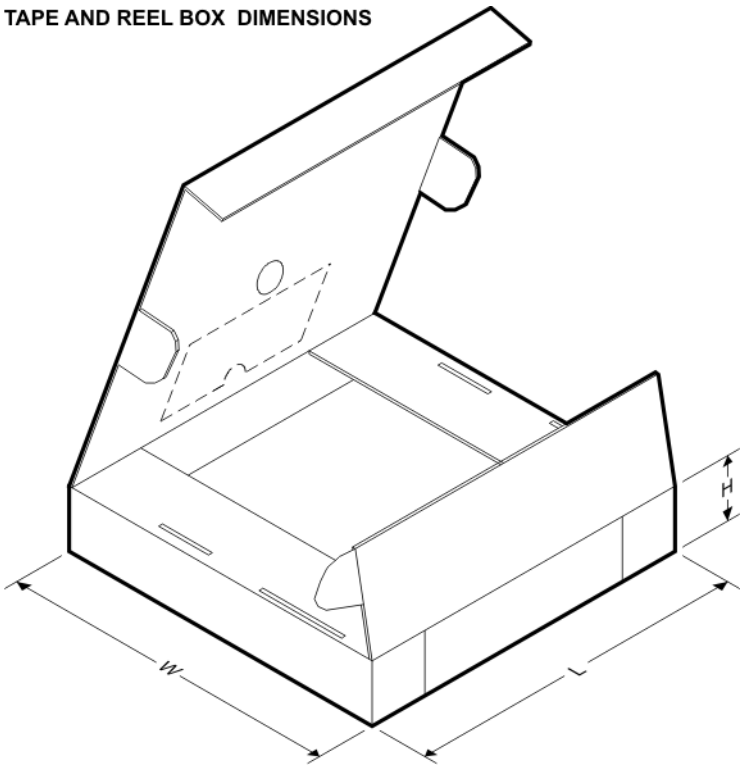
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS12A4516DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TS12A4516DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TS12A4517DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

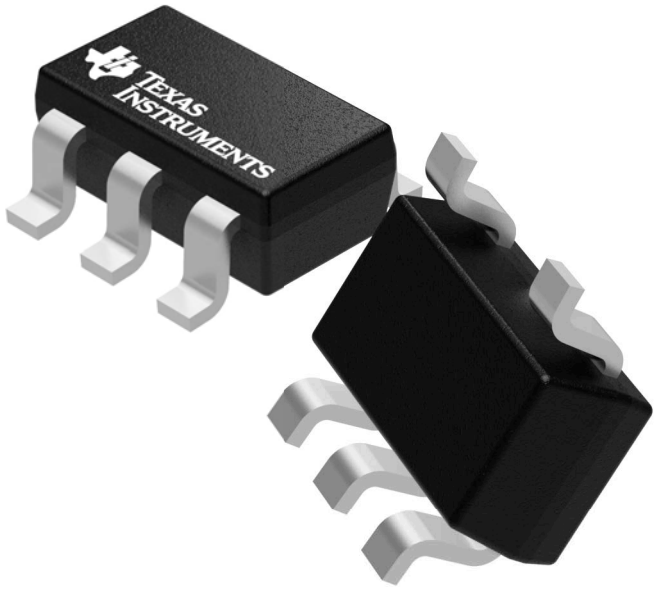


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS12A4516DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
TS12A4516DR	SOIC	D	8	2500	367.0	367.0	35.0
TS12A4517DR	SOIC	D	8	2500	367.0	367.0	35.0

DBV 5 SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



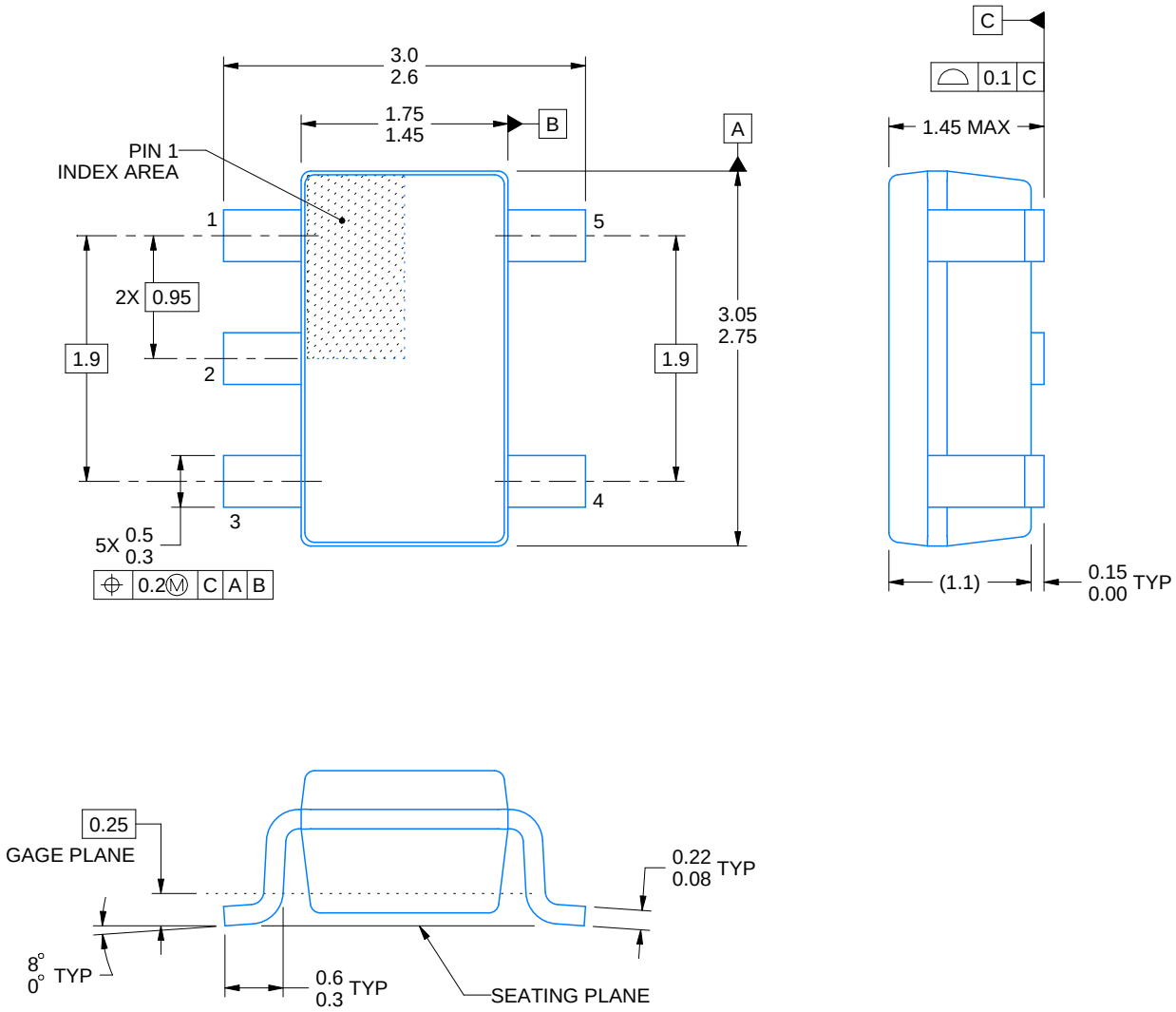
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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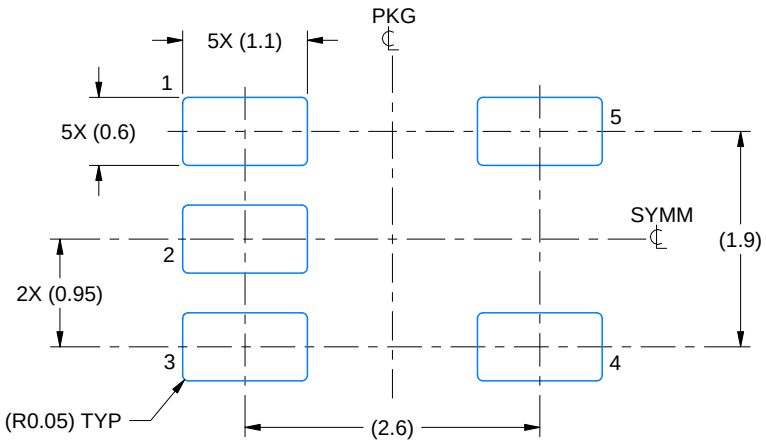
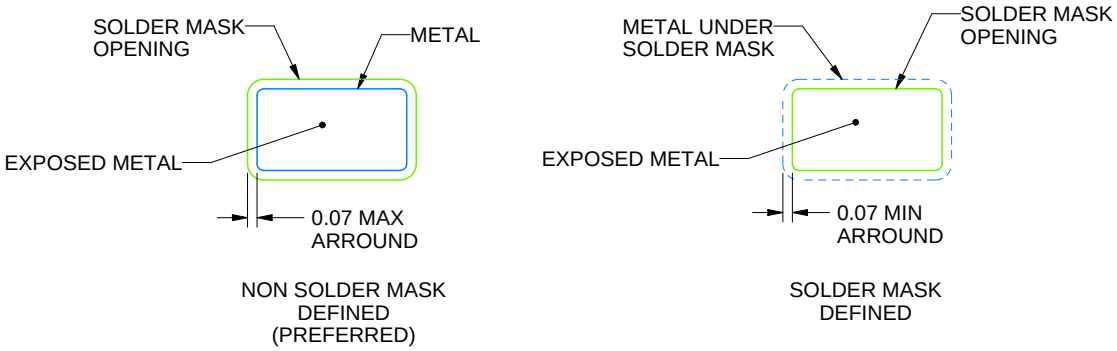
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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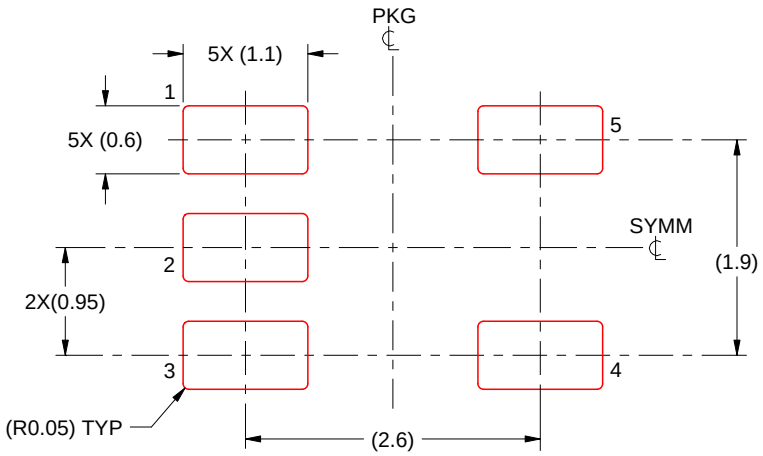
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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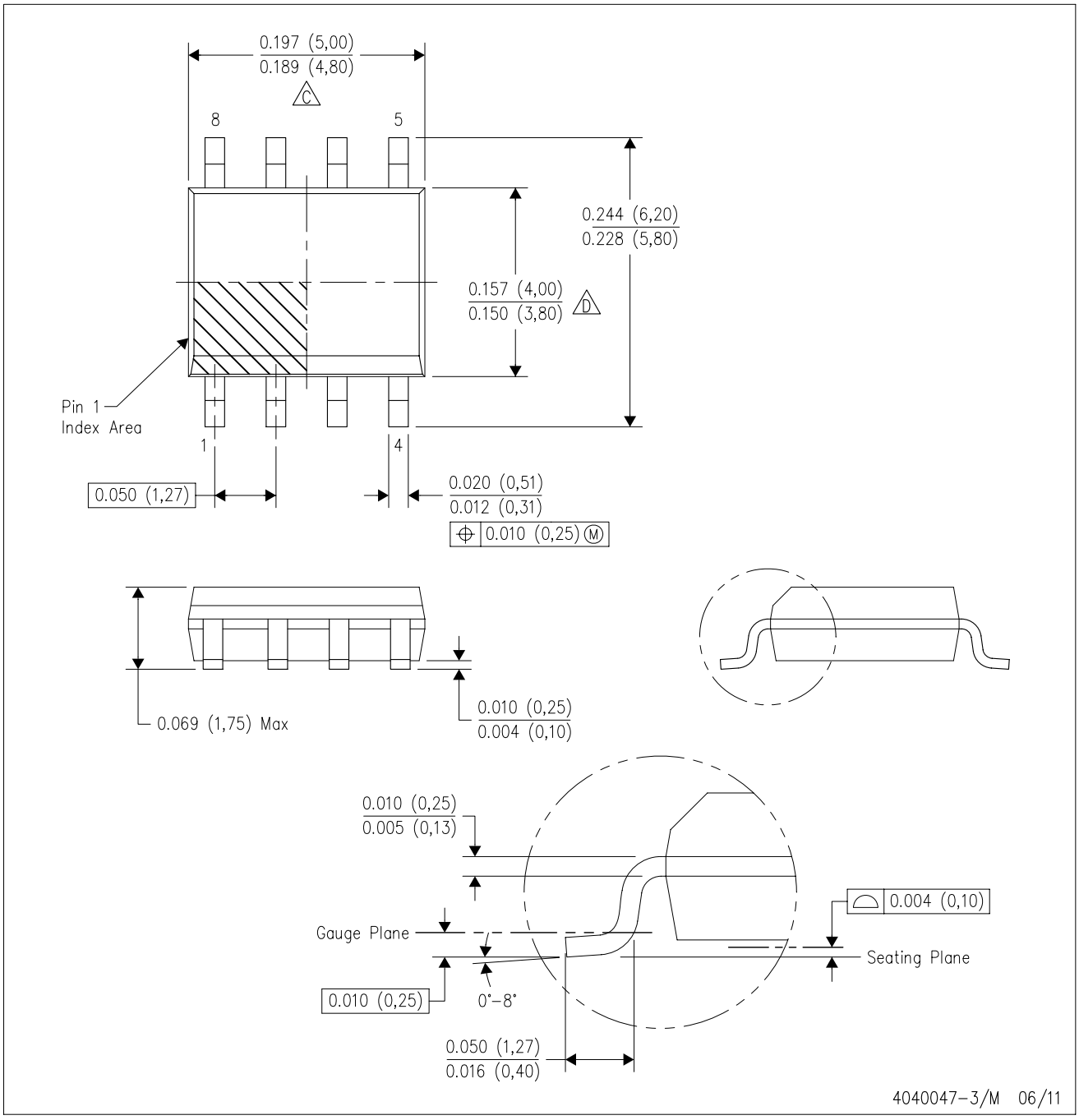
NOTES: (continued)

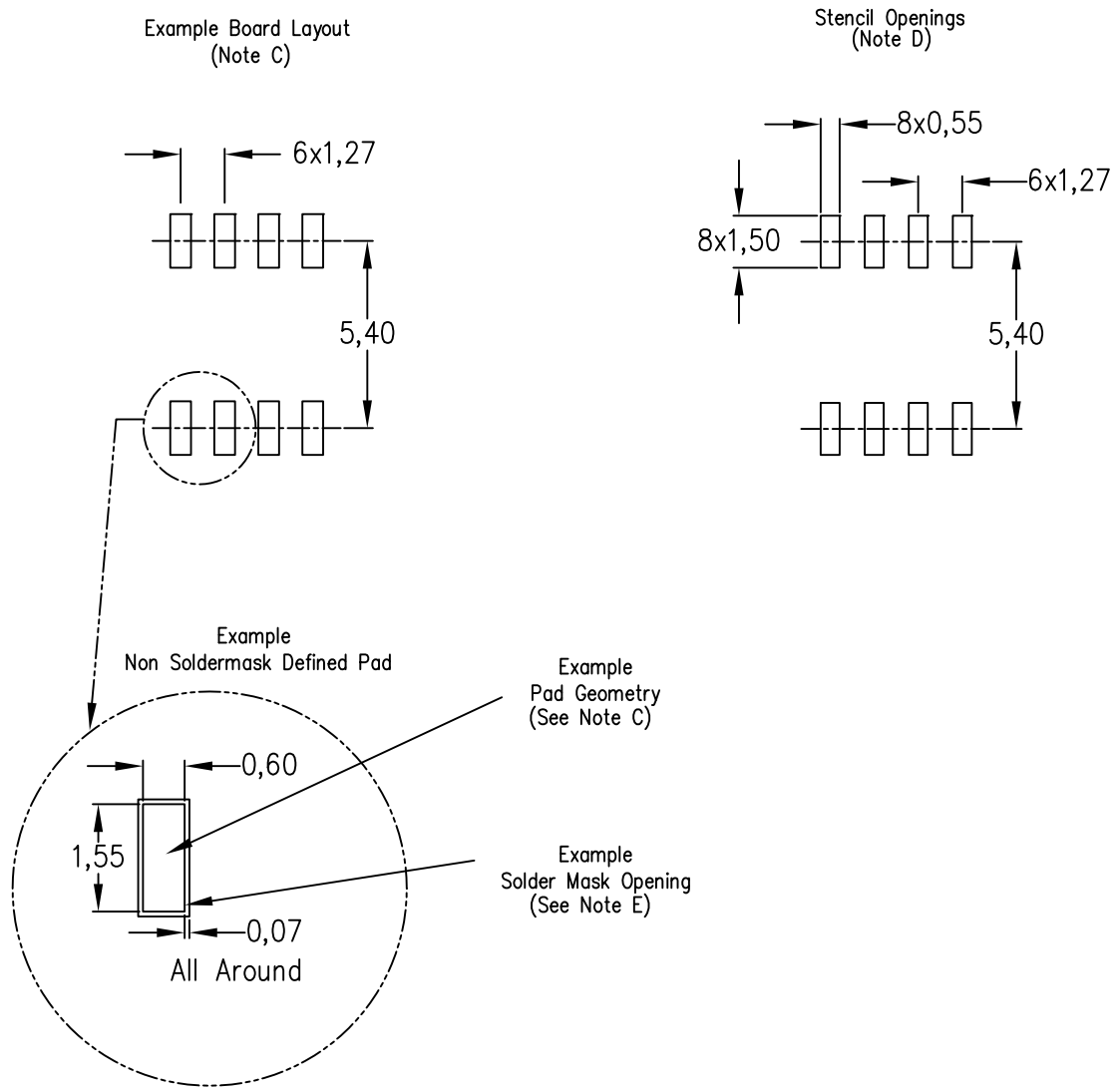
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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