TS321 Low-Power Single Operational Amplifier

1 Features

- Wide Power-Supply Range
  - Single Supply from 3 V to 30 V
  - Dual Supply from ±1.5 V to ±15 V
- Large Output Voltage Swing from 0 V to 3.5 V (Minimum) (V_{CC} = 5 V)
- Low Supply Current at 500 µA (Typical)
- Low Input Bias Current at 20 nA (Typical)
- Stable With High Capacitive Loads

2 Applications

- Desktop PCs
- HVAC: Heating, Ventilating, and Air Conditioning
- Portable Media Players
- Refrigerators
- Washing Machines: High-End and Low-End

3 Description

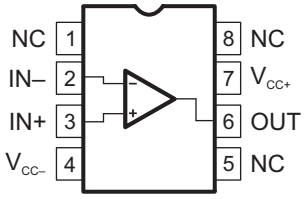
The TS321 is a bipolar operational amplifier for cost-sensitive applications in which space savings are important.

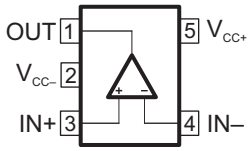
Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS321	SOIC (14)	4.90 mm × 3.90 mm
	SOT-23 (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Device Pinouts





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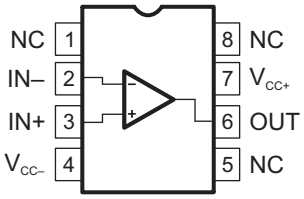
5 Revision History

Changes from Revision B (December 2013) to Revision C **Page**

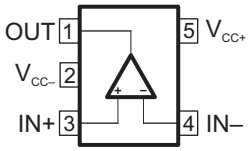
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed V_{OL} units typo from V to mV ... 5

6 Pin Configuration and Functions

D Package
8-Pin SOIC
(Top View)



DBV Package
5-Pin SOT-23
(Top View)



Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOIC NO.	SOT-23 NO.		
IN–	2	4	I	Negative input
IN+	3	3	I	Positive input
NC (1)	1	—	—	Do not connect
	5			
	8			
OUT	6	1	O	Output
V_{CC-}	4	2	—	Negative supply
V_{CC+}	7	5	—	Positive supply

(1) NC – No internal connection

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Single Supply		32	V
		Dual Supplies		±16	
V_{ID}	Differential input voltage(2)			±32	V
V_I	Input voltage range (3)		–0.3	32	V
I_{IK}	Input current			50	mA
t_{short}	Duration of output short circuit to ground			Unlimited	
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Differential voltages are at IN+ with respect to IN–.
(3) Input voltages are at IN with respect to $V_{CC–}$.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Single supply	3	30	V
		Dual supply	±1.5	±15	
T_A	Operating free-air temperature		–40	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TS321		UNIT
		D (SOIC)	DBV (SOT-23)	
		5 PIN	5 PIN	
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)(3)	97	206	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) Maximum power dissipation is a function of TJ(max), qJA, and TA. The maximum allowable power dissipation at any allowable ambient temperature is PD = (TJ(max) – TA)/qJA. Selecting the maximum of 150°C can affect reliability.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

7.5 Electrical Characteristics

V_{CC+} = 5 V, V_{CC-} = GND, V_O = 1.4 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	R_S = 0, 5 V < V_{CC+} < 30 V, 0 < V_{IC} < (V_{CC+} – 1.5 V)		25°C		0.5	4	mV
				Full range			5	
I_{IO}	Input offset current			25°C		2	30	nA
				Full range			50	
I_{IB}	Input bias current(1)			25°C		20	150	nA
				Full range			200	
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, R_L = 2 kΩ, V_O = 1.4 V to 11.4 V		25°C	50	100		V/mV
				Full range	25			
V_{ICR}	Common-mode input voltage(2)	V_{CC} = 30 V		25°C	0		V_{CC+} – 1.5	V
				Full range	0		V_{CC+} – 2	
V_{OH}	High-level output voltage	V_{CC} = 30 V	R_L = 2 kΩ	25°C	26	27		V
				Full range	25.5			
			R_L = 10 kΩ	25°C	27	28		
				Full range	26.5			
		V_{CC} = 5 V	R_L = 2 kΩ	25°C	3.5			
				Full range	3			
V_{OL}	Low-level output voltage	R_L = 10 kΩ		25°C		5	15	mV
				Full range			20	
GBP	Gain bandwidth product	V_{CC} = 30 V, V_I = 10 mV, R_L = 2 kΩ, f = 100 kHz, C_L = 100 pF		25°C		0.8		MHz
SR	Slew rate	V_{CC} = 15 V, V_I = 0.5 V to 3 V, R_L = 2 kΩ, C_L = 100 pF, unity gain		25°C		0.4		V/µs
φ_m	Phase margin			25°C		60		°
CMRR	Common-mode rejection ratio	R_S ≤ 10 kΩ		25°C	65	85		dB
I_{SOURCE}	Output source current	V_{CC} = 15 V, V_O = 2 V, V_{ID} = 1 V		25°C	20	40		mA
I_{SINK}	Output sink current	V_{CC} = 15 V, V_{ID} = 1 V	V_O = 2 V	25°C	10	20		mA
			V_O = 0.2 V	25°C	12	50		µA
I_O	Short-circuit to GND	V_{CC} = 15 V		25°C		40	60	mA
SVR	Supply-voltage rejection ratio	V_{CC} = 5 V to 30 V		25°C	65	110		dB
I_{CC}	Total supply current	No load	V_{CC} = 5 V	25°C		500	800	µA
			V_{CC} = 30 V			600	900	
			V_{CC} = 5 V	Full range		600	900	
			V_{CC} = 30 V				1000	
THD	Total harmonic distortion	V_{CC} = 30 V, V_O = 2 V_{pp}, A_V = 20 dB, R_L = 2 kΩ, f = 1 kHz, C_L = 100 pF		25°C		0.015%		
e_N	Equivalent input noise voltage	V_{CC} = 30 V, f = 1 kHz, R_S = 100 Ω		25°C		50		nV/√Hz

(1) The direction of the input current is out of the device. This current essentially is constant, independent of the state of the output, so no loading change exists on the input lines.
(2) The input common-mode voltage of either input signal should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V_{CC+} – 1.5 V, but either or both inputs can go to 32 V without damage.

7.6 Typical Characteristics

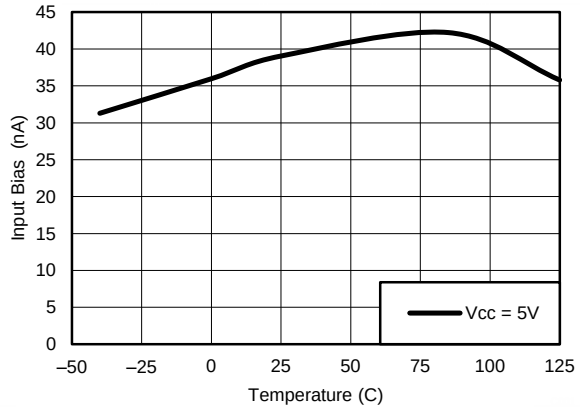


Figure 1. Input Current vs Temperature

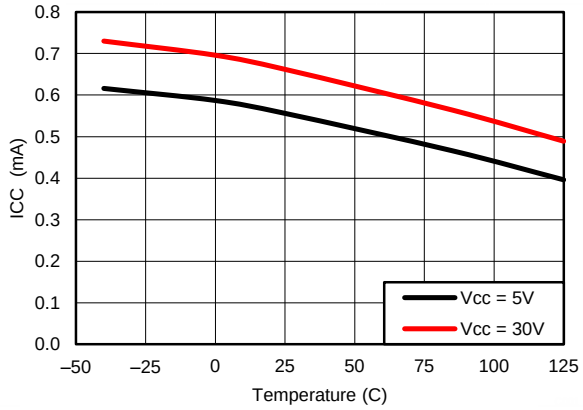


Figure 2. Supply Current vs Temperature

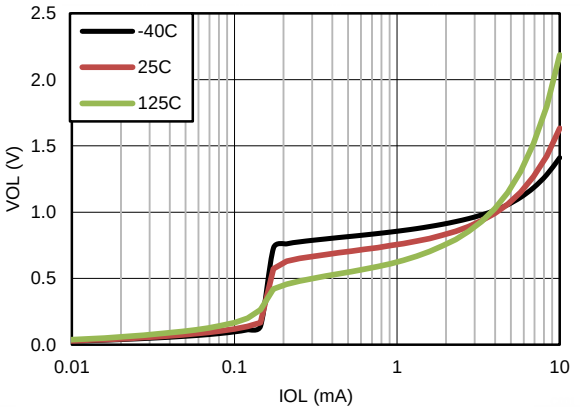


Figure 3. Output Sinking Characteristics

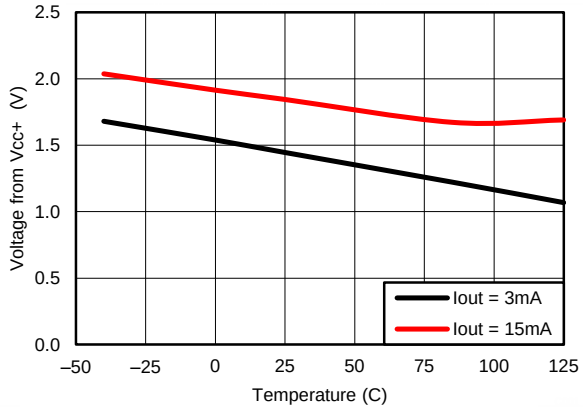


Figure 4. Output Sourcing Characteristics

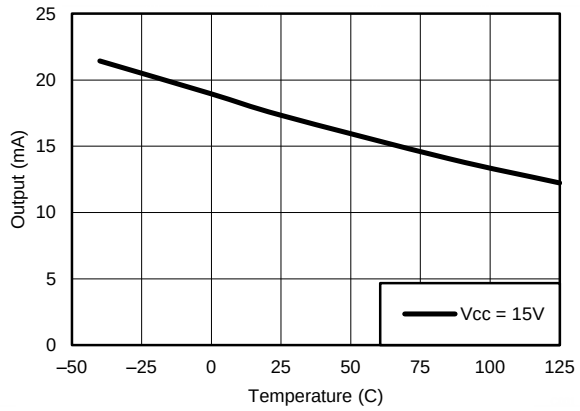


Figure 5. Short Circuit Current to Supply (1)

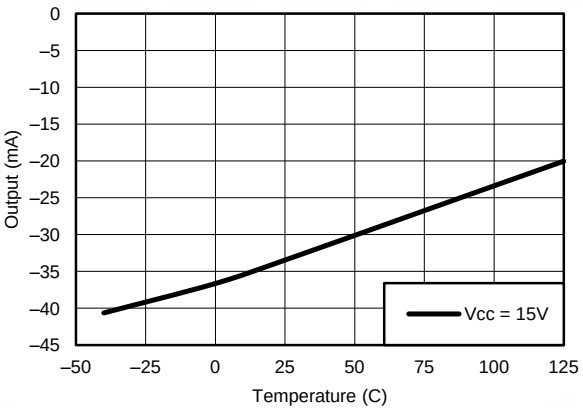


Figure 6. Short Circuit Current to Ground

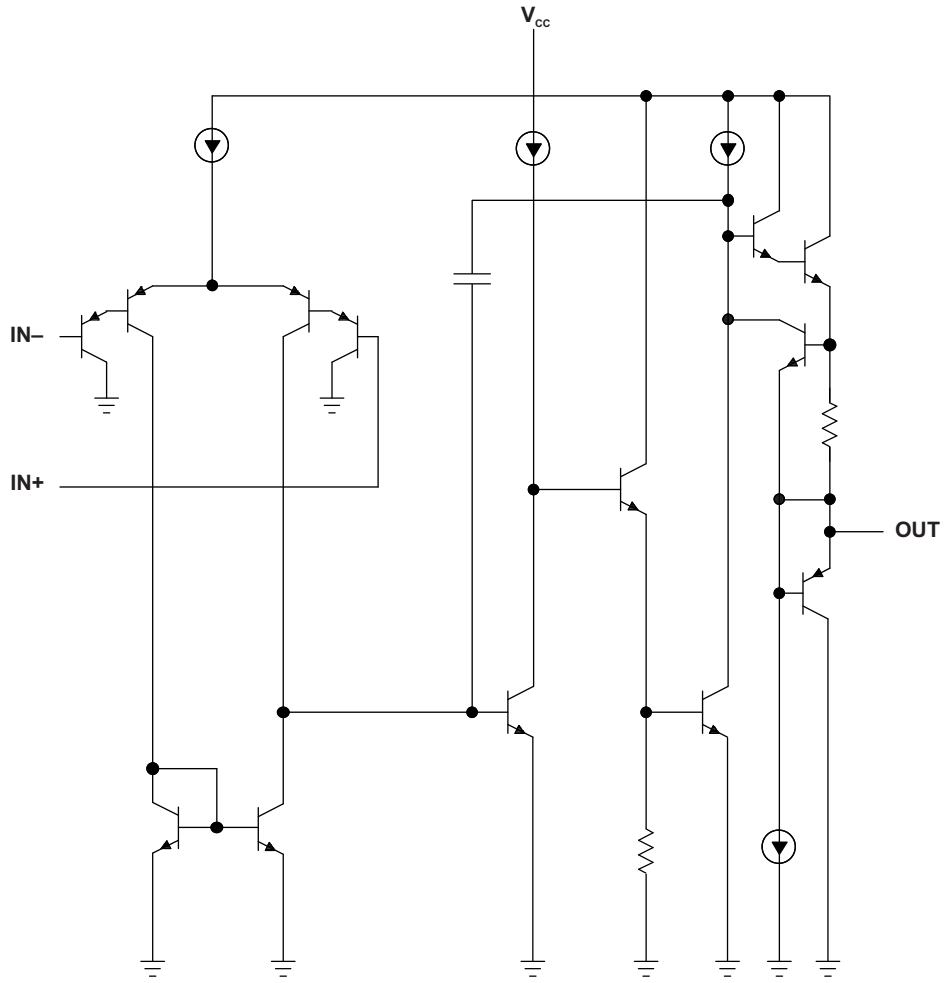
(1) Short circuits from outputs to VCC can cause excessive heating and eventual destruction.

8 Detailed Description

8.1 Overview

The TS321 is a single-channel operational amplifier. It can handle a single supply between 3 V and 30 V or a dual-supply between ±1.5 V and ±15 V. Available in the small SOT-23 package, the TS321 is great for saving space in any application.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Operating Voltage

The TS321 can be powered from a single supply between 3 V and 30 V or a dual-supply between ±1.5 V and ±15 V.

8.3.2 Gain Bandwidth Product

Gain bandwidth product is found by multiplying an amplifier's measured bandwidth by the gain at which that bandwidth was measured. The TS321 has a gain bandwidth of 0.8 MHz.

8.3.3 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. The TS321 has a 0.4-V/µs slew rate.

Feature Description (continued)

8.3.4 Input Common Mode Range

The valid common mode range is from device ground pin to VCC – 1.5 V (VCC – 2 V across temperature). Inputs may exceed VCC up to the maximum VCC without device damage. At least one input must be in the valid input common mode range for output to be correct phase. If both inputs exceed valid range then output phase is undefined. If either input is less than -0.3 V then input current should be limited to 1 mA and output phase is undefined.

8.3.5 Stability With High Capacitive Loads

Operational amplifiers have reduced phase margin when there is a direct capacitance on the output. The stability is affected most when the amplifier is set to unity gain. Small signal response to a step input of 100 mV reveals the loop stability with a range of capacitors. See application note SLVA381 to correlate response waveform to phase margin. The responses at 1 nF or less indicate acceptable phase margin. The responses at 1 uF and above indicate good phase margin.

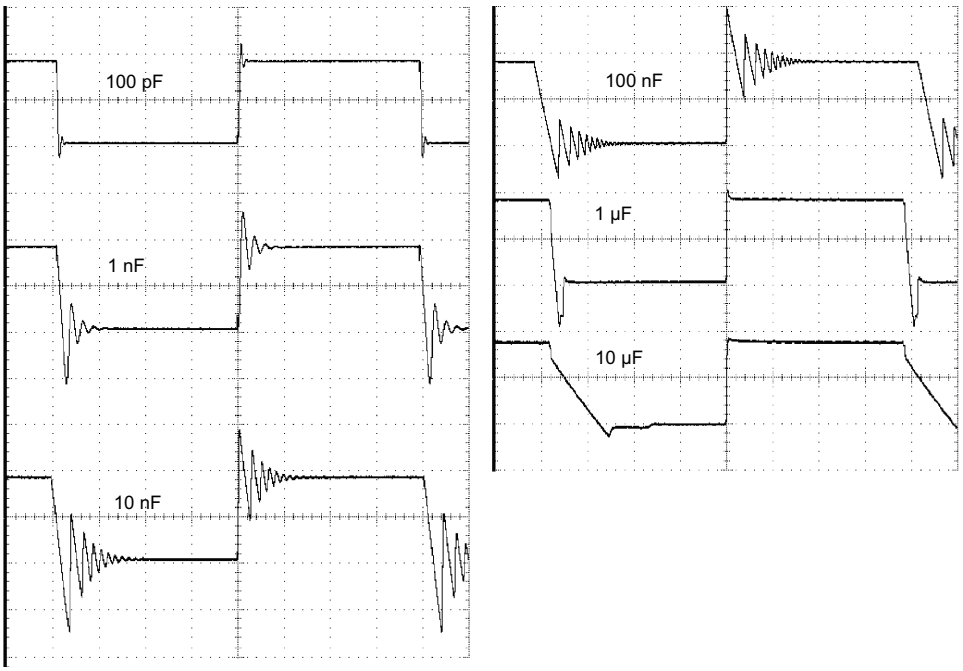


Figure 7. Small Signal Response

8.4 Device Functional Modes

The TS321 is powered on when the supply is connected. This device can be operated as a single supply operational amplifier or dual supply amplifier depending on the application.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TS321 operational amplifier is useful in a wide range of signal conditioning applications. Inputs can be powered before VCC for flexibility in multiple supply circuits.

9.2 Typical Application

A typical application for an operational amplifier in an inverting amplifier. This amplifier takes a positive voltage on the input, and makes it a negative voltage of the same magnitude. In the same manner, it also makes negative voltages positive.

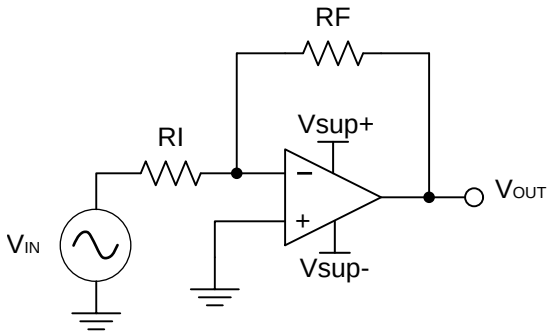


Figure 8. Typcial Application Schematic

9.2.1 Design Requirements

The supply voltage must be chosen such that it is larger than the input voltage range and output range. For instance, this application will scale a signal of ±0.5 V to ±1.8 V. Setting the supply at ±12 V is sufficient to accommodate this application.

9.2.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier:

$$A_v = \frac{VOUT}{VIN} \tag{1}$$

$$A_v = \frac{1.8}{-0.5} = -3.6 \tag{2}$$

Once the desired gain is determined, choose a value for RI or RF. Choosing a value in the kilohm range is desirable because the amplifier circuit will use currents in the milliamp range. This ensures the part will not draw too much current. This example will choose 10 kΩ for RI which means 36 kΩ will be used for RF. This was determined by Equation 3.

$$A_v = -\frac{RF}{RI} \tag{3}$$

Typical Application (continued)

9.2.3 Application Curve

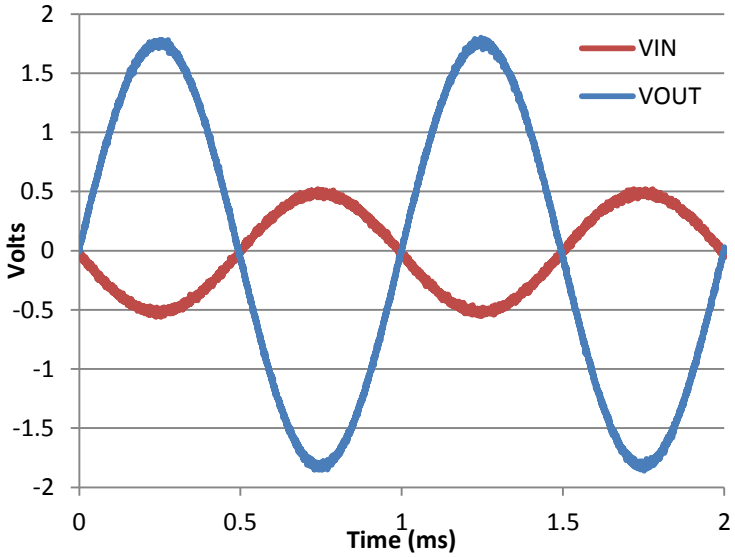


Figure 9. Input and output voltages of the inverting amplifier

10 Power Supply Recommendations

The TS321 is specified to operate between 3 V and 30 V or a dual supply between ±1.5 V and ±15 V.

CAUTION

Supply voltages larger than 32 V for a single supply, or outside the range of ±16 V for a dual supply can permanently damage the device (see the *Absolute Maximum Ratings*).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout*.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, refer to application note SLOA089.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as

Layout Guidelines (continued)

opposed to in parallel with the noisy trace.

- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in *Layout Example*.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example

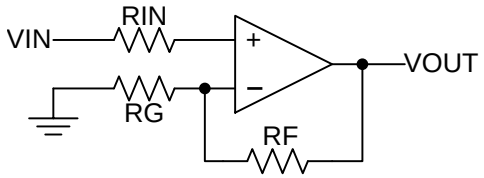


Figure 10. Operational Amplifier Schematic for Noninverting Configuration

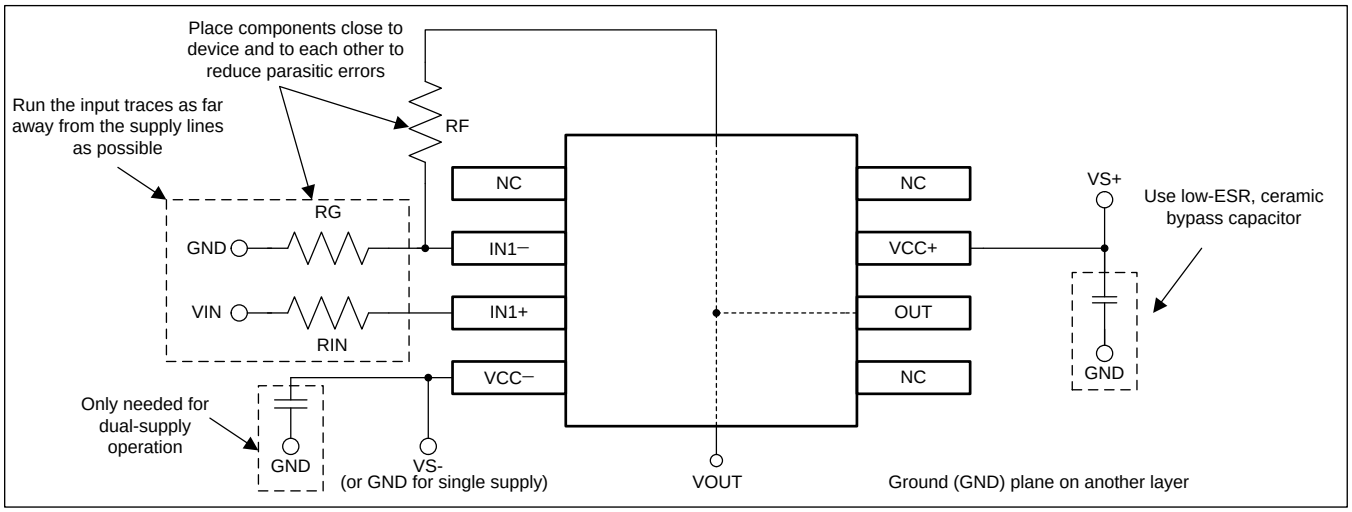


Figure 11. Operational Amplifier Board Layout for Noninverting Configuration

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For more information, see the following:

- *Simplifying Stability Checks,* SLVA381
- *Circuit Board Layout Techniques,* SLOA089

12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS321ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SR321I	Samples
TS321IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	(9C1G ~ 9C1S)	Samples
TS321IDBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	9C1G	Samples
TS321IDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	9C1G	Samples
TS321IDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	(9C1G ~ 9C1S)	Samples
TS321IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SR321I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TS321 :

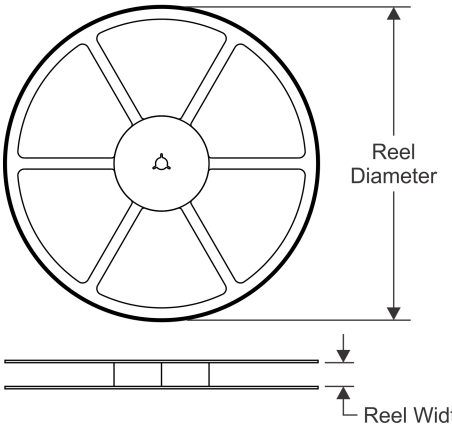
- Automotive: TS321-Q1

NOTE: Qualified Version Definitions:

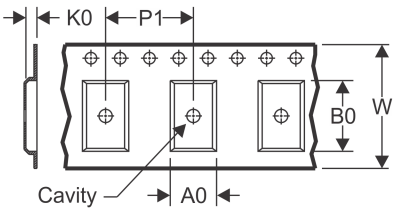
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

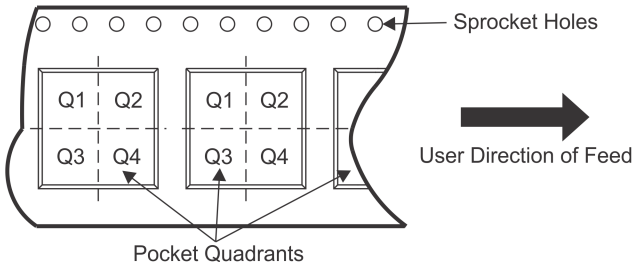


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

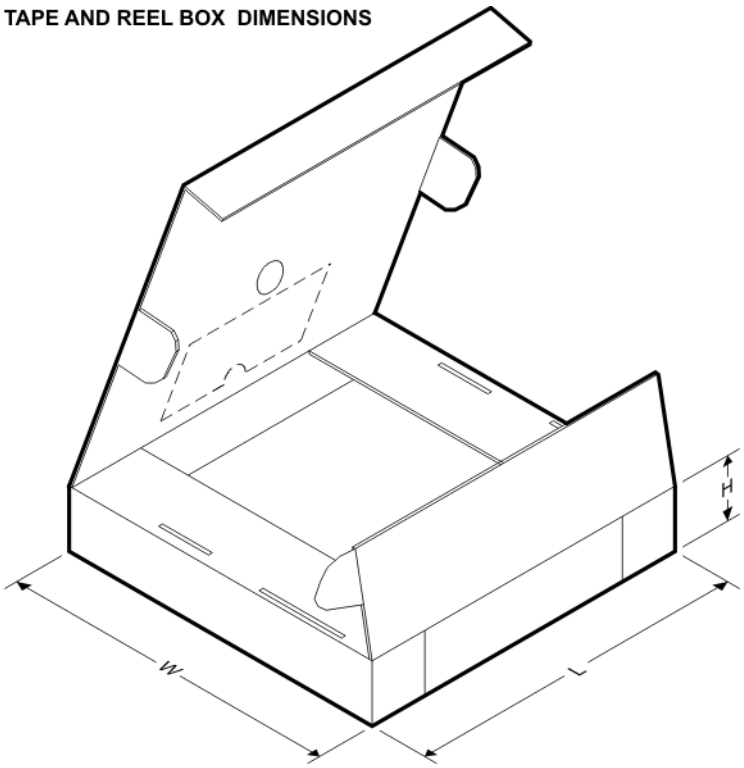
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS321IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TS321IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TS321IDBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TS321IDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TS321IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TS321IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

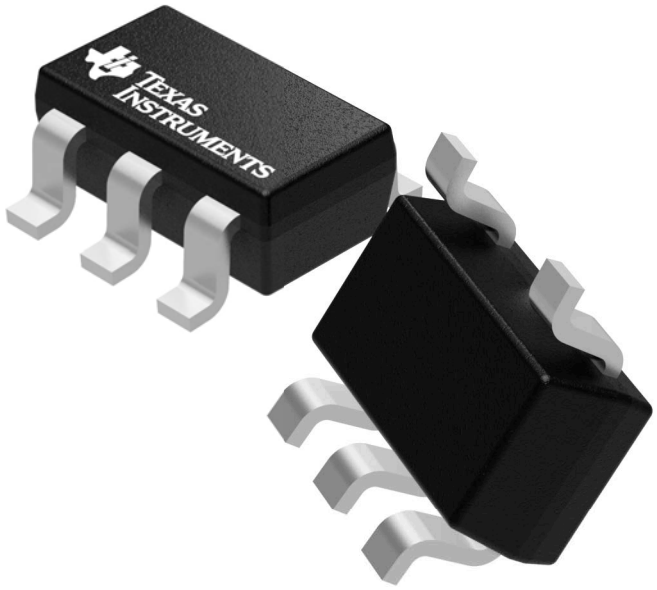


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS321IDBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
TS321IDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TS321IDBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TS321IDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TS321IDBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
TS321IDR	SOIC	D	8	2500	340.5	338.1	20.6

DBV 5 SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



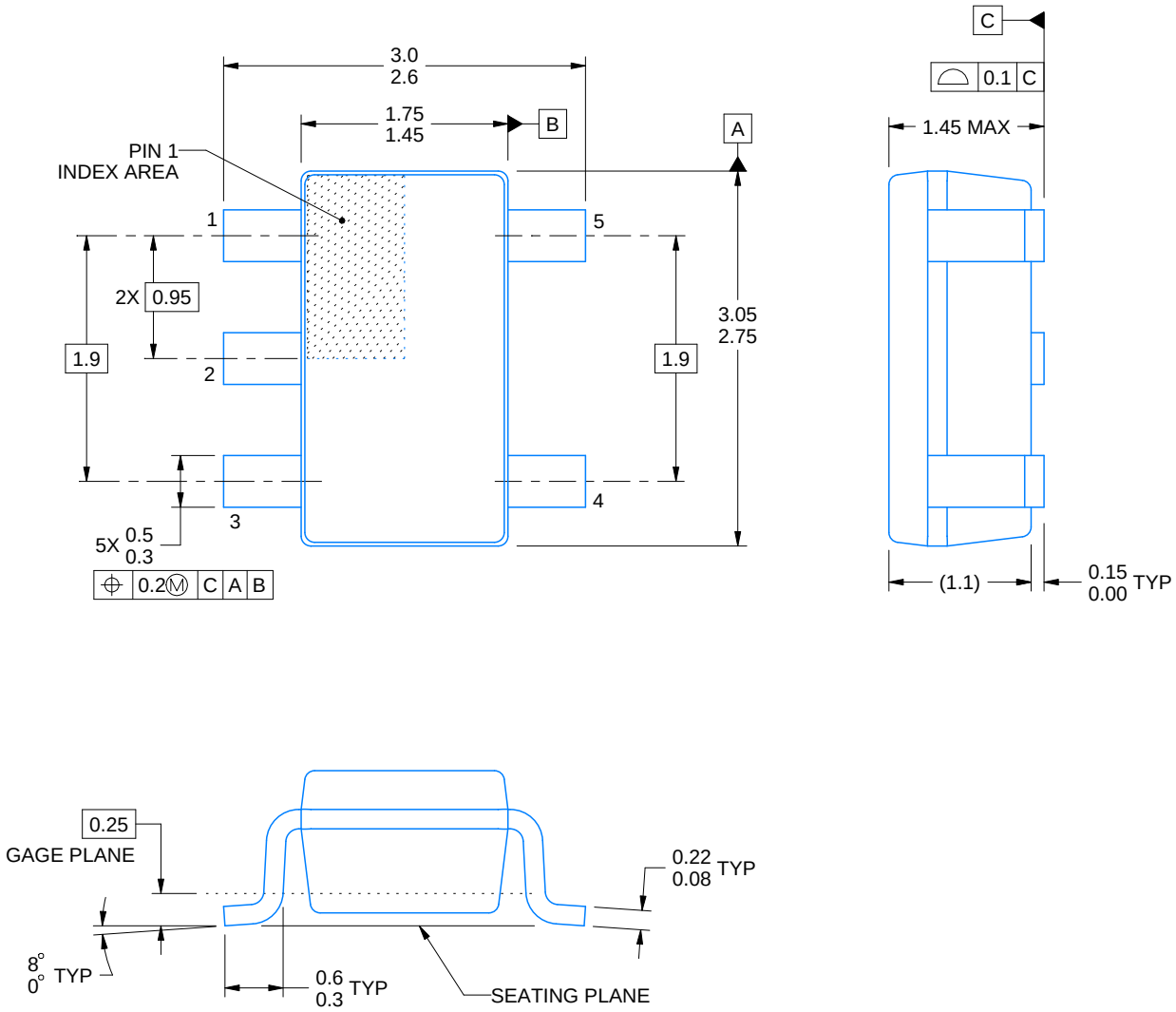
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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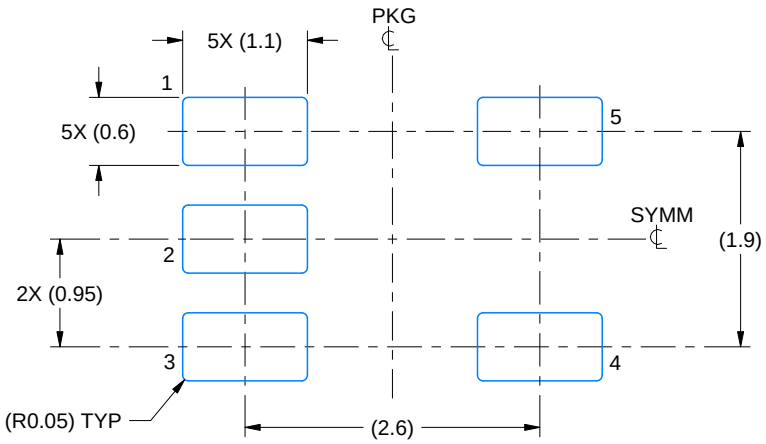
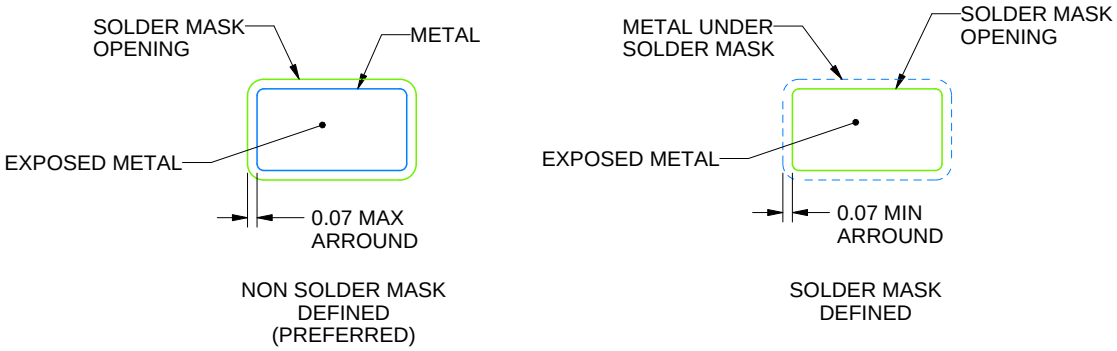
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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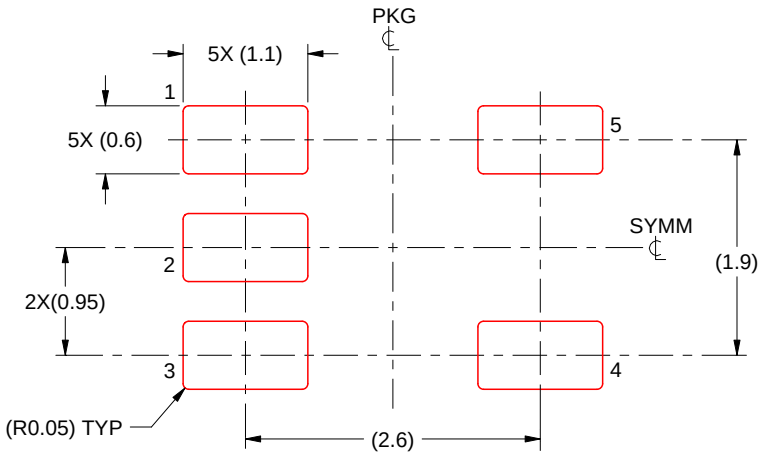
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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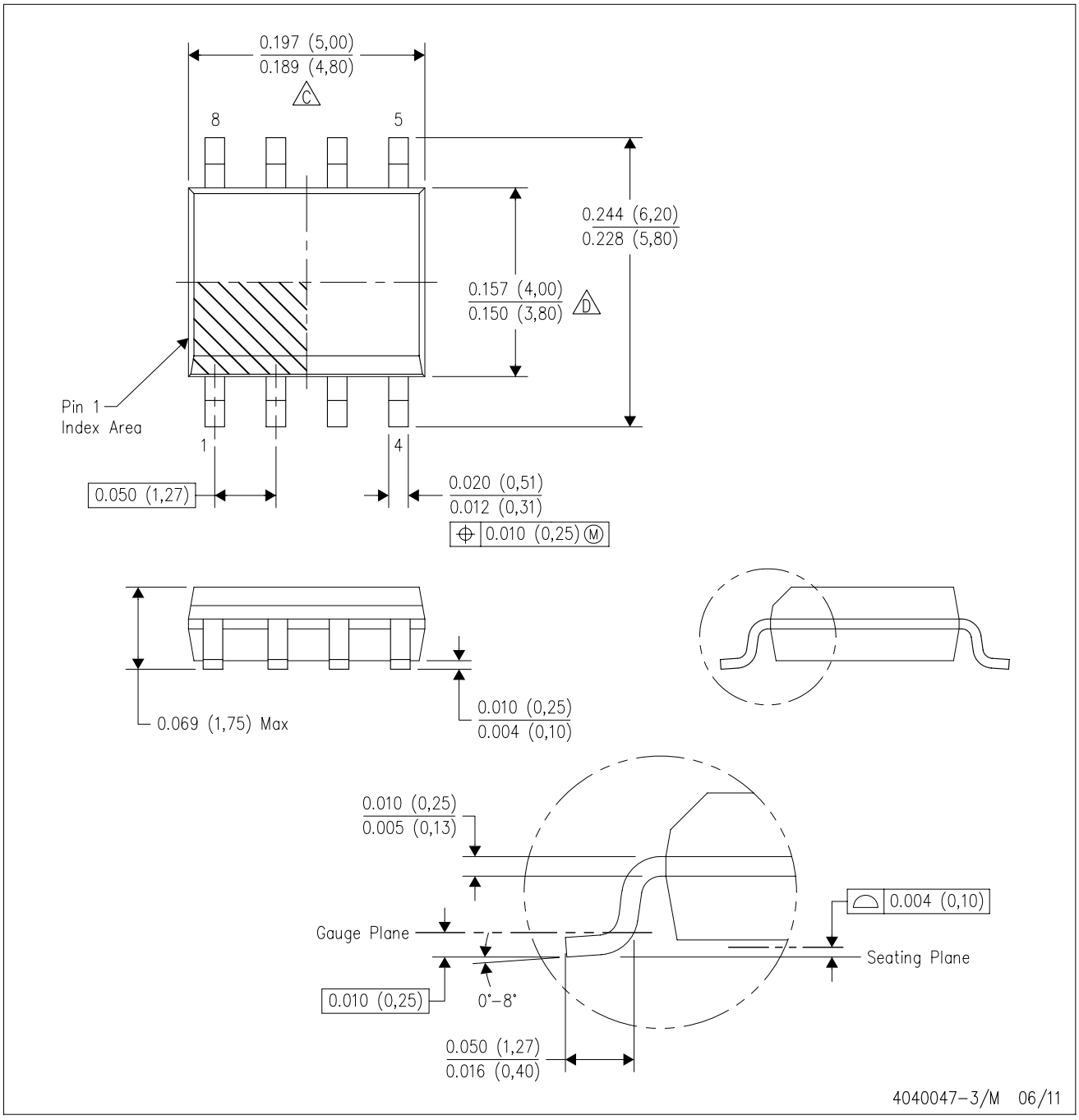
NOTES: (continued)

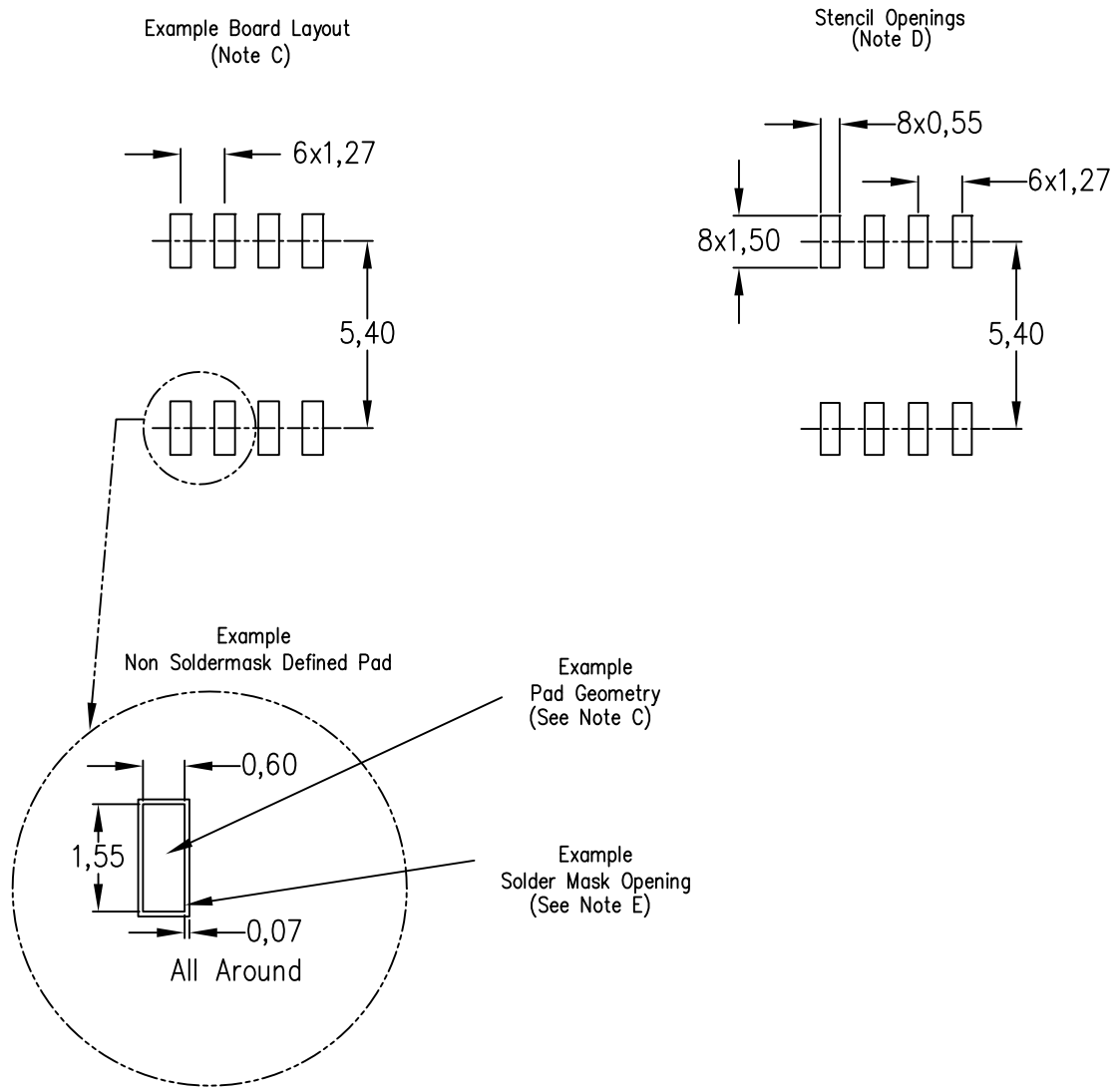
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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