TEXAS INSTRUMENTS

**TS3A27518E**

SCDS260D –MARCH 2009–REVISED MAY 2016

# TS3A27518E 6-Channel, 1:2 Multiplexer/Demultiplexer with Integrated IEC L-4 ESD and 1.8-V Logic Compatible Control Inputs

## 1 Features

- 1.65-V to 3.6-V Single-Supply Operation
- Isolation in Power-Down Mode, $V_{CC} = 0$
- Low-Capacitance Switches, 21.5 pF (Typical)
- Bandwidth Up to 240 MHz for High-Speed Rail-to-Rail Signal Handling
- Crosstalk and OFF Isolation of –62 dB
- 1.8-V Logic Threshold Compatibility for Control Inputs
- 3.6-V Tolerant Control Inputs
- Latch-Up Performance Exceeds 100-mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2500-V Human-Body Model (A114-B, Class II)
  - 1500-V Charged-Device Model (C101)
- ESD Performance: NC/NO Ports
  - ±6-kV Contact Discharge (IEC 61000-4-2)
- 24-WQFN (4.00 mm × 4.00 mm), 24-BGA (3.00 mm × 3.00 mm) and 24-TSSOP (7.90 mm × 6.60 mm) Packages

## 2 Applications

- SD-SDIO and MMC Two-Port MUX
- PC VGA Video MUX-Video Systems
- Audio and Video Signal Routing

## 3 Description

The TS3A27518E is a bidirectional, 6-channel, 1:2 multiplexer-demultiplexer designed to operate from 1.65 V to 3.6 V. This device can handle both digital and analog signals, and can transmit signals up to $V_{CC}$ in either direction. The TS3A27518E has two control pins, each controlling three 1:2 muxes at the same time, and an enable pin that put all outputs in high-impedance mode. The control pins are compatible with 1.8-V logic thresholds and are backward compatible with 2.5-V and 3.3-V logic thresholds.
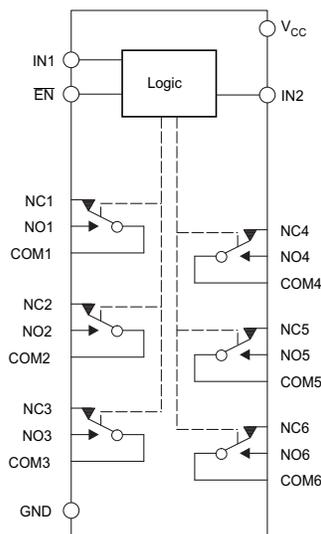
The TS3A27518E allows any SD, SDIO, and multimedia card host controllers to expand out to multiple cards or peripherals because the SDIO interface consists of 6-bits: CMD, CLK, and Data[0:3] signals. The TS3A27518E has two control pins that give additional flexibility to the user. For example, the ability to mux two different audio-video signals in equipment such as an LCD television, an LCD monitor, or a notebook docking station.

### Device Information[1]

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TS3A27518E | WQFN (24) | 4.00 mm × 4.00 mm |
| | TSSOP (24) | 7.90 mm × 6.60 mm |
| | BGA MICROSTAR JUNIOR (24) | 3.00 mm × 3.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Functional Block Diagram



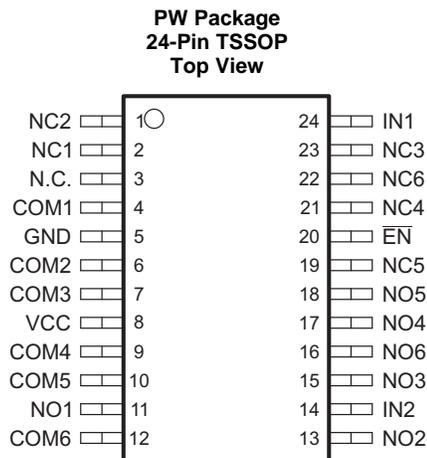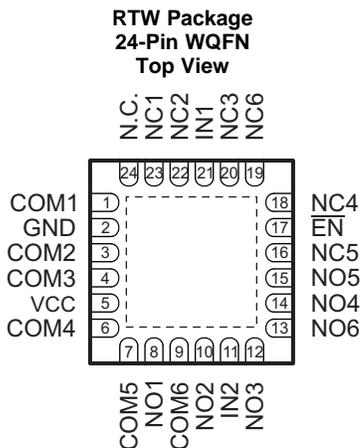Copyright © 2016, Texas Instruments Incorporated

## Table of Contents

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision C (December 2015) to Revision D**                                                                    **Page**

• Updated *Pin Functions* table ..................................................................................................................................... 1

**Changes from Revision B (May 2009) to Revision C**                                                                          **Page**

• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ................................................................................................. 1

Product Folder Links: *TS3A27518E*

# 5 Pin Configuration and Functions

**RTW Package**
**24-Pin WQFN**
**Top View**

**PW Package**
**24-Pin TSSOP**
**Top View**

**ZQS Package**
**24-Pin BGA MICROSTAR JUNIOR**
**Top View**
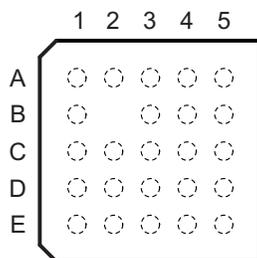
**Pin Functions**

| PIN | | | | I/O | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | RTW | ZQS | PW | | |
| COM1 | 1 | A1 | 4 | I/O | Common-signal path |
| COM2 | 3 | B1 | 6 | I/O | Common-signal path |
| COM3 | 4 | C1 | 7 | I/O | Common-signal path |
| COM4 | 6 | D1 | 9 | I/O | Common-signal path |
| COM5 | 7 | E1 | 10 | I/O | Common-signal path |
| COM6 | 9 | D2 | 12 | I/O | Common-signal path |
| $\overline{EN}$ | 17 | C4 | 20 | I | Digital control to enable or disable all signal paths |
| GND | 2 | C3 | 5 | — | Ground. |
| IN1 | 21 | B4 | 24 | I | Digital control to connect COM to NC or NO |
| IN2 | 11 | D3 | 14 | I | Digital control to connect COM to NC or NO |
| N.C. | 24 | A3 | 3 | — | Not connected |
| NC1 | 23 | B3 | 2 | I/O | Normally closed-signal path |
| NC2 | 22 | A2 | 1 | I/O | Normally closed-signal path |
| NC3 | 20 | A4 | 23 | I/O | Normally closed-signal path |
| NC4 | 18 | B5 | 21 | I/O | Normally closed-signal path |
| NC5 | 16 | C5 | 19 | I/O | Normally closed-signal path |
| NC6 | 19 | A5 | 22 | I/O | Normally closed-signal path |
| NO1 | 8 | E2 | 11 | I/O | Normally open-signal path |
| NO2 | 10 | E3 | 13 | I/O | Normally open-signal path |

## Pin Functions (continued)

| PIN | | | | I/O | DESCRIPTION |
|-----|-----|-----|-----|-----|-------------|
| NAME | RTW | ZQS | PW | | |
| NO3 | 12 | E4 | 15 | I/O | Normally open-signal path |
| NO4 | 14 | D5 | 17 | I/O | Normally open-signal path |
| NO5 | 15 | D4 | 18 | I/O | Normally open-signal path |
| NO6 | 13 | E5 | 16 | I/O | Normally open-signal path |
| $V_{CC}$ | 5 | C2 | 8 | — | Voltage supply |

Product Folder Links: *TS3A27518E*

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1] [2]

|  |  |  | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage [3] |  | −0.5 | 4.6 | V |
| $V_{NC}$ $V_{NO}$ $V_{COM}$ | Analog signal voltage [3] [4] [5] |  | −0.5 | 4.6 | V |
| $I_K$ | Analog port diode current [6] | $V_{CC} < V_{NC}, V_{NO}, V_{COM} < 0$ | −50 |  | mA |
| $I_{NC}$ $I_{NO}$ $I_{COM}$ | ON-state switch current [7] | $V_{NC}, V_{NO}, V_{COM} = 0$ to $V_{CC}$ | −50 | 50 | mA |
| $V_I$ | Digital input voltage [3] [4] |  | −0.5 | 4.6 | V |
| $I_{IK}$ | Digital input clamp current [3] [4] | $V_{IO} < V_I < 0$ | −50 |  | mA |
| $I_{CC}$ | Continuous current through $V_{CC}$ |  |  | 100 | mA |
| $I_{GND}$ | Continuous current through GND |  | −100 |  | mA |
| $T_{stg}$ | Storage temperature |  | −65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions.* Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) This value is limited to 5.5-V maximum.
(6) Requires clamp diodes on analog port to $V_{CC}$.
(7) Pulse at 1-ms duration < 10% duty cycle.

## 6.2 ESD Ratings

|  |  |  | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1] | ±2500 | V |
|  |  | Charged-device model (CDM), per JEDEC specification JESD22-C101 [2] | ±1500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|  |  | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 1.65 | 3.6 | V |
| Analog signal voltage | $V_{NC}$ | 0 | $V_{CC}$ | V |
|  | $V_{NO}$ |  |  |  |
|  | $V_{COM}$ |  |  |  |
| Digital input voltage | $V_I$ | 0 | $V_{CC}$ | V |

## 6.4 Thermal Information

|  |  | TS3A27518E | | | |
|---|---|---|---|---|---|
| THERMAL METRIC [1] |  | PW (TSSOP) | RTW (WQFN) | ZQS (BGA MICROSTAR JUNIOR) | UNIT |
|  |  | 24 PINS | 24 PINS | 24 PINS |  |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 104 | 40.7 | 155.7 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 51.6 | 42.9 | 69.9 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 57.5 | 19.2 | 94.6 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## Thermal Information (continued)

| THERMAL METRIC [1] | | TS3A27518E | | | UNIT |
|---|---|---|---|---|---|
| | | PW (TSSOP) | RTW (WQFN) | ZQS (BGA MICROSTAR JUNIOR) | |
| | | 24 PINS | 24 PINS | 24 PINS | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 9.9 | 1 | 9 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 57.1 | 19.3 | 92.2 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | — | 8 | — | °C/W |

## 6.5 Electrical Characteristics for 3.3-V Supply[1]

$V_{CC}$ = 3 V to 3.6 V, $T_A$ = –40°C to +85°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | | |
| $V_{COM}$, $V_{NO}$, $V_{NC}$ | Analog signal voltage | | | | 0 | | $V_{CC}$ | V |
| $r_{on}$ | ON-state resistance | $V_{CC}$ = 3 V | $0 \leq (V_{NC}$ or $V_{NO})$ $\leq V_{CC}$, $I_{COM}$ = –32 mA | Switch ON, see Figure 15 | $T_A$ = 25°C | | 4.4 | 6.2 | V |
| | | | | | $T_A$ = –40°C to +85°C | | | 7.6 | |
| $\Delta r_{on}$ | ON-state resistance match between channels | $V_{CC}$ = 3 V | $V_{NC}$ or $V_{NO}$ = 2.1 V, $I_{COM}$ = –32 mA | Switch ON, see Figure 15 | $T_A$ = 25°C | | 0.3 | 0.7 | Ω |
| | | | | | $T_A$ = –40°C to +85°C | | | 0.8 | |
| $r_{on(flat)}$ | ON-state resistance flatness | $V_{CC}$ = 3 V | $0 \leq (V_{NC}$ or $V_{NO})$ $\leq V_{CC}$, $I_{COM}$ = –32 mA | Switch ON, see Figure 16 | $T_A$ = 25°C | | 0.95 | 2.1 | Ω |
| | | | | | $T_A$ = –40°C to +85°C | | | 2.3 | |
| $I_{NC(OFF)}$, $I_{NO(OFF)}$ | NC, NO OFF leakage current | $V_{CC}$ = 3.6 V | $V_{NC}$ or $V_{NO}$ = 1 V, $V_{COM}$ = 3 V, or $V_{NC}$ or $V_{NO}$ = 3 V, $V_{COM}$ = 1 V | Switch OFF, see Figure 16 | $T_A$ = 25°C | –0.5 | 0.05 | 0.5 | µA |
| | | | | | $T_A$ = –40°C to +85°C | –7 | | 7 | |
| $I_{NC(PWROFF)}$, $I_{NO(PWROFF)}$ | | $V_{CC}$ = 0 V | $V_{NC}$ or $V_{NO}$ = 0 to 3.6 V, $V_{COM}$ = 3.6 V to 0, or $V_{NC}$ or $V_{NO}$ = 3.6 V to 0, $V_{COM}$ = 0 to 3.6 V | | $T_A$ = 25°C | –1 | 0.05 | 1 | |
| | | | | | $T_A$ = –40°C to +85°C | –12 | | 12 | |
| $I_{COM(OFF)}$ | COM OFF leakage current | $V_{CC}$ = 3.6 V | $V_{NC}$ or $V_{NO}$ = 3 V, $V_{COM}$ = 1 V, or $V_{NC}$ or $V_{NO}$ = 1 V, $V_{COM}$ = 3 V | Switch OFF, see Figure 16 | $T_A$ = 25°C | –1 | 0.01 | 1 | µA |
| | | | | | $T_A$ = –40°C to +85°C | –2 | | 2 | |
| $I_{COM(PWROFF)}$ | | $V_{CC}$ = 0 V | $V_{NC}$ or $V_{NO}$ = 3.6 V to 0, $V_{COM}$ = 0 to 3.6 V, or $V_{NC}$ or $V_{NO}$ = 0 to 3.6 V, $V_{COM}$ = 3.6 V to 0 | | $T_A$ = 25°C | –1 | 0.02 | 1 | |
| | | | | | $T_A$ = –40°C to +85°C | –12 | | 1 | |
| $I_{NO(ON)}$, $I_{NC(ON)}$ | NC, NO ON leakage current | $V_{CC}$ = 3.6 V | $V_{NC}$ or $V_{NO}$ = 1 V, $V_{COM}$ = open, or $V_{NC}$ or $V_{NO}$ = 3 V, $V_{COM}$ = open | Switch ON, see Figure 17 | $T_A$ = 25°C | –2.5 | 0.04 | 2.2 | µA |
| | | | | | $T_A$ = –40°C to +85°C | –7 | | 7 | |

(1)  The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

Product Folder Links: *TS3A27518E*

## Electrical Characteristics for 3.3-V Supply[1]  (continued)

$V_{CC}$ = 3 V to 3.6 V, $T_A$ = –40°C to +85°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $I_{COM(ON)}$ | COM ON leakage current | $V_{CC}$ = 3.6 V | $V_{NC}$ or $V_{NO}$ = open, $V_{COM}$ = 1 V, or $V_{NC}$ or $V_{NO}$ = open, $V_{COM}$ = 3 V | Switch ON, see Figure 17 | $T_A$ = 25°C | –2 | 0.03 | 2 | µA |
| | | | | | $T_A$ = –40°C to +85°C | –7 | | 7 | |
| **DIGITAL CONTROL INPUTS (IN1, IN2, $\overline{EN}$)** [2] | | | | | | | | | |
| $V_{IH}$ | Input logic high | $V_{CC}$ = 3.6 V | | | $T_A$ = –40°C to +85°C | 1.2 | | 3.6 | V |
| $V_{IL}$ | Input logic low | $V_{CC}$ = 3.6 V | | | $T_A$ = –40°C to +85°C | 0 | | 0.65 | V |
| $I_{IH}$, $I_{IL}$ | Input leakage current | $V_{CC}$ = 3.6 V | $V_I$ = $V_{CC}$ or 0 | | $T_A$ = 25°C | –0.1 | 0.05 | 0.1 | µA |
| | | | | | $T_A$ = –40°C to +85°C | –2.5 | | 2.5 | |
| **DYNAMIC** | | | | | | | | | |
| $t_{ON}$ | Turnon time | $V_{CC}$ = 3.3 V | $V_{COM}$ = $V_{CC}$, $R_L$ = 50 Ω | $C_L$ = 35 pF, see Figure 19 | $T_A$ = 25°C | | 18.1 | 59 | ns |
| | | $V_{CC}$ = 3 V to 3.6 V | | | $T_A$ = –40°C to +85°C | | | 60 | |
| $t_{OFF}$ | Turnoff time | $V_{CC}$ = 3.3 V | $V_{COM}$ = $V_{CC}$, $R_L$ = 50 Ω | $C_L$ = 35 pF, see Figure 19 | $T_A$ = 25°C | | 25.4 | 60.6 | ns |
| | | $V_{CC}$ = 3 V to 3.6 V | | | $T_A$ = –40°C to +85°C | | | 61 | |
| $t_{BBM}$ | Break-before-make time | $V_{CC}$ = 3.3 V | $V_{NC}$ = $V_{NO}$ = $V_{CC}$/2, $R_L$ = 50 Ω | $C_L$ = 35 pF, see Figure 20 | $T_A$ = 25°C | 4 | 11.1 | 22.7 | ns |
| | | $V_{CC}$ = 3 V to 3.6 V | | | $T_A$ = –40°C to +85°C | | | 28 | |
| $Q_C$ | Charge injection | $V_{CC}$ = 3.3 V | $V_{GEN}$ = 0, $R_{GEN}$ = 0 | $C_L$ = 0.1 nF, see Figure 24 | $T_A$ = 25°C | | 0.81 | | pC |
| $C_{NC(OFF)}$, $C_{NO(OFF)}$ | NC, NO OFF capacitance | $V_{CC}$ = 3.3 V | $V_{NC}$ or $V_{NO}$ = $V_{CC}$ or GND, Switch OFF | See Figure 18 | $T_A$ = 25°C | | 13 | | pF |
| $C_{COM(OFF)}$ | COM OFF capacitance | $V_{CC}$ = 3.3 V | $V_{NC}$ or $V_{NO}$ = $V_{CC}$ or GND, Switch OFF | See Figure 18 | $T_A$ = –40°C to +85°C | | 8.5 | | pF |
| $C_{NC(ON)}$, $C_{NO(ON)}$ | NC, NO ON capacitance | $V_{CC}$ = 3.3 V | $V_{NC}$ or $V_{NO}$ = $V_{CC}$ or GND, Switch OFF | See Figure 18 | | | 21.5 | | pF |
| $C_{COM(ON)}$ | COM ON capacitance | $V_{CC}$ = 3.3 V | $V_{COM}$ = $V_{CC}$ or GND, Switch ON | See Figure 18 | | | 21.5 | | pF |
| $C_I$ | Digital input capacitance | $V_{CC}$ = 3.3 V | $V_I$ = $V_{CC}$ or GND | See Figure 18 | | | 2 | | pF |
| BW | Bandwidth | $V_{CC}$ = 3.3 V | $R_L$ = 50 Ω, | Switch ON, see Figure 20 | | | 240 | | MHz |
| $O_{ISO}$ | OFF isolation | $V_{CC}$ = 3.3 V | $R_L$ = 50 Ω, f = 10 MHz | Switch OFF, see Figure 22 | | | –62 | | dB |
| $X_{TALK}$ | Crosstalk | $V_{CC}$ = 3.3 V | $R_L$ = 50 Ω, f = 10 MHz | Switch ON, see Figure 23 | | | –62 | | dB |
| $X_{TALK(ADJ)}$ | Crosstalk adjacent | $V_{CC}$ = 3.3 V | $R_L$ = 50 Ω, f = 10 MHz | Switch ON, see Figure 23 | | | –71 | | dB |
| THD | Total harmonic distortion | $V_{CC}$ = 3.3 V | $R_L$ = 600 Ω, $C_L$ = 50 pF | f = 20 Hz to 20 kHz, see Figure 25 | | | 0.05% | | |
| **SUPPLY** | | | | | | | | | |
| $I_{CC}$ | Positive supply current | $V_{CC}$ = 3.6 V | $V_I$ = $V_{CC}$ or GND | Switch ON or OFF | $T_A$ = 25°C | | 0.04 | 0.3 | µA |
| | | | | | $T_A$ = –40°C to +85°C | | | 3 | |

(2)   All unused digital inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

Product Folder Links: *TS3A27518E*

## 6.6 Electrical Characteristics for 2.5-V Supply[1]

$V_{CC}$ = 2.3 V to 2.7 V, $T_A$ = –40°C to +85°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | | |
| $V_{COM}$, $V_{NO}$, $V_{NC}$ | Analog signal voltage | | | | 0 | | $V_{CC}$ | V |
| $r_{on}$ | ON-state resistance | $V_{CC}$ = 2.3 V | 0 ≤ ($V_{NC}$ or $V_{NO}$) ≤ $V_{CC}$, $I_{COM}$ = –32 mA | Switch ON, see Figure 15 | $T_A$ = 25°C | | 5.5 | 9.6 | Ω |
| | | | | | $T_A$ = –40°C to +85°C | | | 11.5 | |
| $\Delta r_{on}$ | ON-state resistance match between channels | $V_{CC}$ = 2.3 V | $V_{NC}$ or $V_{NO}$ = 1.6 V, $I_{COM}$ = –32 mA | Switch ON, see Figure 15 | $T_A$ = 25°C | | 0.3 | 0.8 | Ω |
| | | | | | $T_A$ = –40°C to +85°C | | | 0.9 | |
| $r_{on(flat)}$ | ON-state resistance flatness | $V_{CC}$ = 2.3 V | 0 ≤ ($V_{NC}$ or $V_{NO}$) ≤ $V_{CC}$, $I_{COM}$ = –32 mA | Switch ON, see Figure 16 | $T_A$ = 25°C | | 0.91 | 2.2 | Ω |
| | | | | | $T_A$ = –40°C to +85°C | | | 2.3 | |
| $I_{NC(OFF)}$, $I_{NO(OFF)}$ | NC, NO OFF leakage current | $V_{CC}$ = 2.7 V | $V_{NC}$ or $V_{NO}$ = 0.5 V, $V_{COM}$ = 2.3 V, or $V_{NC}$ or $V_{NO}$ = 2.3 V, $V_{COM}$ = 0.5 V | Switch OFF, see Figure 16 | $T_A$ = 25°C | –0.3 | 0.04 | 0.3 | µA |
| | | | | | $T_A$ = –40°C to +85°C | –6 | | 6 | |
| $I_{NC(PWROFF)}$, $I_{NO(PWROFF)}$ | | $V_{CC}$ = 0 V | $V_{NC}$ or $V_{NO}$ = 0 to 2.7 V, $V_{COM}$ = 2.7 V to 0, or $V_{NC}$ or $V_{NO}$ = 2.7 V to 0, $V_{COM}$ = 0 to 2.7 V | | $T_A$ = 25°C | –0.6 | 0.02 | 0.6 | |
| | | | | | $T_A$ = –40°C to +85°C | –10 | | 10 | |
| $I_{COM(OFF)}$ | COM OFF leakage current | $V_{CC}$ = 2.7 V | $V_{NC}$ or $V_{NO}$ = 0.5 V, $V_{COM}$ = 2.3 V, or $V_{NC}$ or $V_{NO}$ = 2.3 V, $V_{COM}$ = 0.5 V | Switch OFF, see Figure 16 | $T_A$ = 25°C | –0.7 | 0.02 | 0.7 | µA |
| | | | | | $T_A$ = –40°C to +85°C | –1 | | 1 | |
| $I_{COM(PWROFF)}$ | | $V_{CC}$ = 0 V | $V_{NC}$ or $V_{NO}$ = 2.7 V to 0, $V_{COM}$ = 0 to 2.7 V, or $V_{NC}$ or $V_{NO}$ = 0 to 2.7 V, $V_{COM}$ = 2.7 V to 0 | | $T_A$ = 25°C | –0.7 | 0.02 | 0.7 | |
| | | | | | $T_A$ = –40°C to +85°C | –7.2 | | 7.2 | |
| $I_{NO(ON)}$ $I_{NC(ON)}$ | NC, NO ON leakage current | $V_{CC}$ = 2.7 V | $V_{NC}$ or $V_{NO}$ = 0.5 V or 2.3 V, $V_{COM}$ = open | Switch ON, see Figure 17 | $T_A$ = 25°C | –2.1 | 0.03 | 2.1 | µA |
| | | | | | $T_A$ = –40°C to +85°C | –6 | | 6 | |
| $I_{COM(ON)}$ | COM ON leakage current | $V_{CC}$ = 2.7 V | $V_{NC}$ or $V_{NO}$ = open, $V_{COM}$ = 0.5 V, or $V_{NC}$ or $V_{NO}$ = open, $V_{COM}$ = 2.3 V | Switch ON, see Figure 17 | $T_A$ = 25°C | –2 | 0.02 | 2 | µA |
| | | | | | $T_A$ = –40°C to +85°C | –5.7 | | 5.7 | |
| **DIGITAL CONTROL INPUTS (IN1, IN2, EN)** [2] | | | | | | | | |
| $V_{IH}$ | Input logic high | $V_{CC}$ = 2.7 V | $V_I$ = $V_{CC}$ or GND | | $T_A$ = –40°C to +85°C | 1.15 | | 3.6 | V |
| $V_{IL}$ | Input logic low | $V_{CC}$ = 2.7 V | | | | 0 | | 0.55 | V |
| $I_{IH}$, $I_{IL}$ | Input leakage current | $V_{CC}$ = 2.7 V | $V_I$ = $V_{CC}$ or 0 | | $T_A$ = 25°C | –0.1 | 0.01 | 0.1 | µA |
| | | | | | $T_A$ = –40°C to +85°C | –2.1 | | 2.1 | |
| **DYNAMIC** | | | | | | | | |
| $t_{ON}$ | Turnon time | $V_{CC}$ = 2.5 V | $V_{COM}$ = VCC, $R_L$ = 50 Ω | $C_L$ = 35 pF, see Figure 19 | $T_A$ = 25°C | | 17.2 | 36.8 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | | $T_A$ = –40°C to +85°C | | | 42.5 | |
| $t_{OFF}$ | Turnoff time | $V_{CC}$ = 2.5 V | $V_{COM}$ = VCC, $R_L$ = 50 Ω | $C_L$ = 35 pF, see Figure 19 | $T_A$ = 25°C | | 17.1 | 29.8 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | | $T_A$ = –40°C to +85°C | | | 34.4 | |
| $t_{BBM}$ | Break-before-make time | $V_{CC}$ = 2.5 V | $V_{NC}$ = $V_{NO}$ = $V_{CC}$/2, $R_L$ = 50 Ω | $C_L$ = 35 pF, see Figure 20 | $T_A$ = 25°C | 4.5 | 13 | 30 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | | $T_A$ = –40°C to +85°C | | | 33.3 | |

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(2) All unused digital inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

## Electrical Characteristics for 2.5-V Supply[1] (continued)

$V_{CC}$ = 2.3 V to 2.7 V, $T_A$ = −40°C to +85°C (unless otherwise noted)

| | PARAMETER | | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $Q_C$ | Charge injection | $V_{CC}$ = 2.5 V | $V_{GEN}$ = 0, $R_{GEN}$ = 0 | $C_L$ = 0.1 nF, see Figure 24 | | | 0.47 | | pC |
| $C_{NC(OFF)}$, $C_{NO(OFF)}$ | NC, NO OFF capacitance | $V_{CC}$ = 2.5 V | $V_{NC}$ or $V_{NO}$ = $V_{CC}$ or GND, switch OFF | See Figure 18 | | | 13.5 | | pF |
| $C_{COM(OFF)}$ | COM OFF capacitance | $V_{CC}$ = 2.5 V | $V_{NC}$ or $V_{NO}$ = $V_{CC}$ or GND, switch OFF | See Figure 18 | $T_A$ = −40°C to +85°C | | 9 | | pF |
| $C_{NC(ON)}$, $C_{NO(ON)}$ | NC, NO ON capacitance | $V_{CC}$ = 2.5 V | $V_{NC}$ or $V_{NO}$ = $V_{CC}$ or GND, switch OFF | See Figure 18 | | | 22 | | pF |
| $C_{COM(ON)}$ | COM ON capacitance | $V_{CC}$ = 2.5 V | $V_{COM}$ = $V_{CC}$ or GND, switch ON | See Figure 18 | | | 22 | | pF |
| $C_I$ | Digital input capacitance | $V_{CC}$ = 2.5 V | $V_I$ = $V_{CC}$ or GND | See Figure 18 | | | 2 | | pF |
| BW | Bandwidth | $V_{CC}$ = 2.5 V | $R_L$ = 50 Ω | Switch ON, see Figure 20 | | | 240 | | MHz |
| $O_{ISO}$ | OFF isolation | $V_{CC}$ = 2.5 V | $R_L$ = 50 Ω, f = 10 MHz | Switch OFF, see Figure 22 | | | −62 | | dB |
| $X_{TALK}$ | Crosstalk | $V_{CC}$ = 2.5 V | $R_L$ = 50 Ω, f = 10 MHz | Switch ON, see Figure 23 | | | −62 | | dB |
| $X_{TALK(ADJ)}$ | Crosstalk adjacent | $V_{CC}$ = 2.5 V | $R_L$ = 50 Ω, f = 10 MHz | Switch ON, see Figure 23 | | | −71 | | dB |
| THD | Total harmonic distortion | $V_{CC}$ = 2.5 V | $R_L$ = 600 Ω, $C_L$ = 50 pF | f = 20 Hz to 20 kHz, see Figure 25 | | | 0.06% | | |
| **SUPPLY** | | | | | | | | | |
| $I_{CC}$ | Positive supply current | $V_{CC}$ = 2.7 V | $V_I$ = $V_{CC}$ or GND | Switch ON or OFF | $T_A$ = 25°C | | 0.01 | 0.1 | μA |
| | | | | | $T_A$ = −40°C to +85°C | | | 2 | |

## 6.7 Electrical Characteristics for 1.8-V Supply[1]

$V_{CC}$ = 1.65 V to 1.95 V, $T_A$ = −40°C to 85°C (unless otherwise noted)

| | PARAMETER | | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | | | |
| $V_{COM}$, $V_{NO}$, $V_{NC}$ | Analog signal voltage | | | | | 0 | | $V_{CC}$ | V |
| $r_{on}$ | ON-state resistance | $V_{CC}$ = 1.65 V | 0 ≤ ($V_{NC}$ or $V_{NO}$) ≤ $V_{CC}$, $I_{COM}$ = −32 mA | Switch ON, see Figure 15 | $T_A$ = 25°C | | 7.1 | 14.4 | Ω |
| | | | | | $T_A$ = −40°C to +85°C | | | 16.3 | |
| $\Delta r_{on}$ | ON-state resistance match between channels | $V_{CC}$ = 1.65 V | $V_{NC}$ or $V_{NO}$ = 1.5 V, $I_{COM}$ = −32 mA | Switch ON, see Figure 15 | $T_A$ = 25°C | | 0.3 | 1 | Ω |
| | | | | | $T_A$ = −40°C to +85°C | | | 1.2 | |
| $r_{on(flat)}$ | ON-state resistance flatness | $V_{CC}$ = 1.65 V | 0 ≤ ($V_{NC}$ or $V_{NO}$) ≤ $V_{CC}$, $I_{COM}$ = −32 mA | Switch ON, see Figure 16 | $T_A$ = 25°C | | 2.7 | 5.5 | Ω |
| | | | | | $T_A$ = −40°C to +85°C | | | 7.3 | |
| $I_{NC(OFF)}$, $I_{NO(OFF)}$ | NC, NO OFF leakage current | $V_{CC}$ = 1.95 V | $V_{NC}$ or $V_{NO}$ = 0.3 V, $V_{COM}$ = 1.65 V, or $V_{NC}$ or $V_{NO}$ = 1.65 V, $V_{COM}$ = 0.3 V | Switch OFF, see Figure 16 | $T_A$ = 25°C | −0.25 | 0.03 | 0.25 | μA |
| | | | | | $T_A$ = −40°C to +85°C | −5 | | 5 | |
| $I_{NC(PWROFF)}$, $I_{NO(PWROFF)}$ | | $V_{CC}$ = 0 V | $V_{NC}$ or $V_{NO}$ = 1.95 V to 0, $V_{COM}$ = 0 to 1.95 V, or $V_{NC}$ or $V_{NO}$ = 0 to 1.95 V, $V_{COM}$ = 1.95 V to 0 | | $T_A$ = 25°C | −0.4 | 0.01 | 0.4 | μA |
| | | | | | $T_A$ = −40°C to +85°C | −7.2 | | 7.2 | |

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

Product Folder Links: TS3A27518E

## Electrical Characteristics for 1.8-V Supply[1]  (continued)

$V_{CC}$ = 1.65 V to 1.95 V, $T_A$ = –40°C to 85°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $I_{COM(OFF)}$ | COM OFF leakage current | $V_{CC}$ = 1.95 V | $V_{NC}$ or $V_{NO}$ = 0.3 V, $V_{COM}$ = 1.65 V, or $V_{NC}$ or $V_{NO}$ = 1.65 V, $V_{COM}$ = 0.3 V | Switch OFF, see Figure 16 | $T_A$ = 25°C | –0.4 | 0.02 | 0.4 | µA |
| | | | | | $T_A$ = –40°C to +85°C | –0.9 | | 0.9 | |
| $I_{COM(PWROFF)}$ | | $V_{CC}$ = 0 V | $V_{NC}$ or $V_{NO}$ = 1.95 V to 0, $V_{COM}$ = 0 to 1.95 V, or $V_{NC}$ or $V_{NO}$ = 0 to 1.95 V, $V_{COM}$ = 1.95 V to 0 | | $T_A$ = 25°C | –0.4 | 0.02 | 0.4 | µA |
| | | | | | $T_A$ = –40°C to +85°C | –5 | | 5 | |
| $I_{NO(ON)}$, $I_{NC(ON)}$ | NC, NO ON leakage current | $V_{CC}$ = 1.95 V | $V_{NC}$ or $V_{NO}$ = 0.3 V, $V_{COM}$ = open, or $V_{NC}$ or $V_{NO}$ = 1.65 V, $V_{COM}$ = open | Switch ON, see Figure 17 | $T_A$ = 25°C | –2 | 0.02 | 2 | µA |
| | | | | | $T_A$ = –40°C to +85°C | –5.2 | | 5.2 | |
| $I_{COM(ON)}$ | COM ON leakage current | $V_{CC}$ = 1.95 V | $V_{NC}$ or $V_{NO}$ = open, $V_{COM}$ = 0.3 V, or $V_{NC}$ or $V_{NO}$ = open, $V_{COM}$ = 1.65 V | Switch ON, see Figure 17 | $T_A$ = 25°C | –2 | 0.02 | 2 | µA |
| | | | | | $T_A$ = –40°C to +85°C | –5.2 | | 5.2 | |
| **DIGITAL CONTROL INPUTS (IN1, IN2, $\overline{EN}$)** [2] | | | | | | | | | |
| $V_{IH}$ | Input logic high | $V_{CC}$ = 1.95 V | $V_I$ = $V_{CC}$ or GND | | $T_A$ = –40°C to +85°C | 1 | | 3.6 | V |
| $V_{IL}$ | Input logic low | $V_{CC}$ = 1.95 V | | | $T_A$ = –40°C to +85°C | 0 | | 0.4 | V |
| $I_{IH}$, $I_{IL}$ | Input leakage current | $V_{CC}$ = 1.95 V | $V_I$ = $V_{CC}$ or 0 | | $T_A$ = 25°C | –0.1 | 0.01 | 0.1 | µA |
| | | | | | $T_A$ = –40°C to +85°C | –2.1 | | 2.1 | |
| **DYNAMIC** | | | | | | | | | |
| $t_{ON}$ | Turnon time | $V_{CC}$ = 1.8 V | $V_{COM}$ = $V_{CC}$, $R_L$ = 50 Ω | $C_L$ = 35 pF, see Figure 19 | $T_A$ = 25°C | | 14.1 | 49.3 | ns |
| | | $V_{CC}$ = 1.65 V to 1.95 V | | | $T_A$ = –40°C to +85°C | | | 56.7 | |
| $t_{OFF}$ | Turnoff time | $V_{CC}$ = 1.8 V | $V_{COM}$ = $V_{CC}$, $R_L$ = 50 Ω | $C_L$ = 35 pF, see Figure 19 | $T_A$ = 25°C | | 16.1 | 26.5 | ns |
| | | $V_{CC}$ = 1.65 V to 1.95 V | | | $T_A$ = –40°C to +85°C | | | 31.2 | |
| $t_{BBM}$ | Break-before-make time | $V_{CC}$ = 1.8 V | $V_{NC}$ = $V_{NO}$ = $V_{CC}$/2, $R_L$ = 50 Ω | $C_L$ = 35 pF, see Figure 20 | $T_A$ = 25°C | 5.3 | 18.4 | 58 | ns |
| | | $V_{CC}$ = 1.65 V to 1.95 V | | | $T_A$ = –40°C to +85°C | | | 58 | |
| $Q_C$ | Charge injection | $V_{CC}$ = 1.8 V | $V_{GEN}$ = 0, $R_{GEN}$ = 0 | $C_L$ = 1 nF, see Figure 24 | | | 0.21 | | pC |
| $C_{NC(OFF)}$, $C_{NO(OFF)}$ | NC, NO OFF capacitance | $V_{CC}$ = 1.8 V | $V_{NC}$ or $V_{NO}$ = $V_{CC}$ or GND, switch OFF | See Figure 18 | | | 9 | | pF |
| $C_{NC(ON)}$, $C_{NO(ON)}$ | NC, NO ON capacitance | $V_{CC}$ = 1.8 V | $V_{NC}$ or $V_{NO}$ = $V_{CC}$ or GND, switch OFF | See Figure 18 | | | 22 | | pF |
| $C_{COM(ON)}$ | COM ON capacitance | $V_{CC}$ = 1.8 V | $V_{COM}$ = $V_{CC}$ or GND, switch ON | See Figure 18 | | | 22 | | pF |
| $C_I$ | Digital input capacitance | $V_{CC}$ = 1.8 V | $V_I$ = $V_{CC}$ or GND | See Figure 18 | | | 2 | | pF |
| BW | Bandwidth | $V_{CC}$ = 1.8 V | $R_L$ = 50 Ω | Switch ON, see Figure 20 | | | 240 | | MHz |
| $O_{ISO}$ | OFF isolation | $V_{CC}$ = 1.8 V | $R_L$ = 50 Ω, f = 10 MHz | Switch OFF, see Figure 22 | | | –60 | | dB |

(2)   All unused digital inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

Product Folder Links: *TS3A27518E*

## Electrical Characteristics for 1.8-V Supply[1]  (continued)

$V_{CC}$ = 1.65 V to 1.95 V, $T_A$ = –40°C to 85°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $X_{TALK}$ | Crosstalk | $V_{CC}$ = 1.8 V | $R_L$ = 50 Ω, f = 10 MHz | Switch ON, see Figure 23 | | | –60 | | dB |
| $X_{TALK(ADJ)}$ | Crosstalk adjacent | $V_{CC}$ = 1.8 V | $R_L$ = 50 Ω, f = 10 MHz | Switch ON, see Figure 23 | | | –71 | | dB |
| THD | Total harmonic distortion | $V_{CC}$ = 1.8 V | $R_L$ = 600 Ω, $C_L$ = 50 pF | f = 20 Hz to 20 kHz, see Figure 25 | | | 0.1% | | |
| **SUPPLY** | | | | | | | | | |
| $I_{CC}$ | Positive supply current | $V_{CC}$ = 1.95 V | $V_I$ = $V_{CC}$ or GND | Switch ON or OFF | $T_A$ = 25°C | | 0.01 | 0.1 | µA |
| | | | | | $T_A$ = –40°C to +85°C | | | 1.5 | |

Product Folder Links: *TS3A27518E*

## 6.8 Typical Characteristics
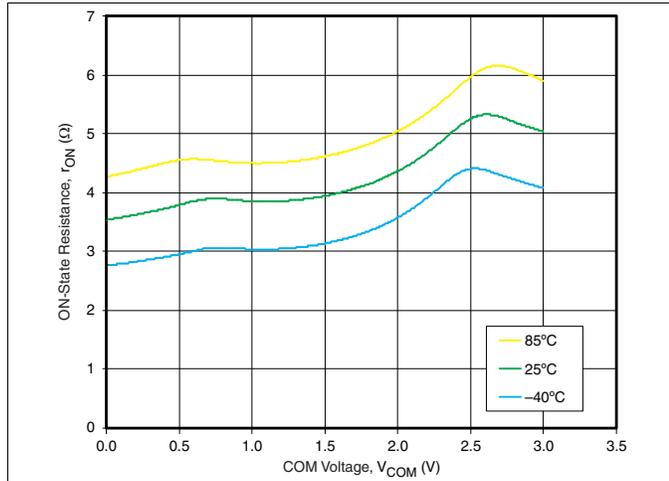


**Figure 1. ON-State Resistance vs COM Voltage (V_CC = 3 V)**
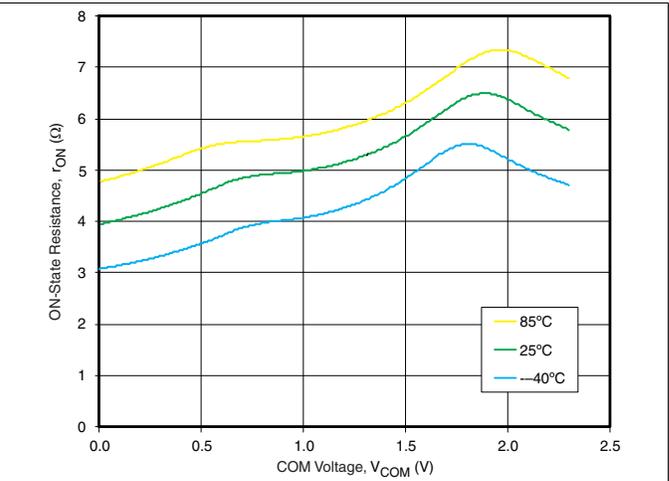


**Figure 2. ON-State Resistance vs COM Voltage (V_CC = 2.3 V)**
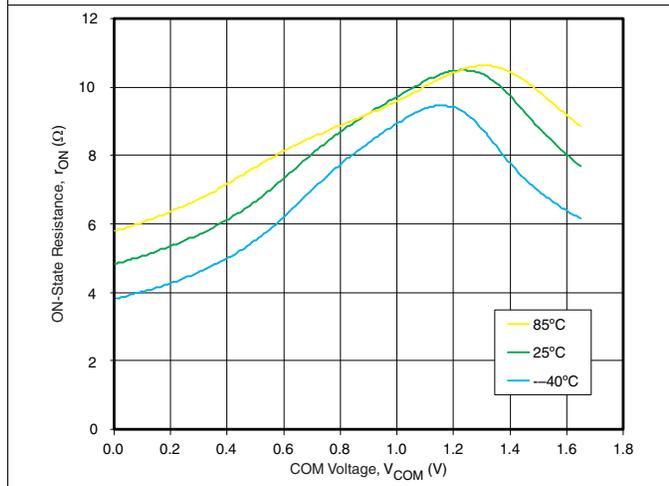


**Figure 3. ON-State Resistance vs COM Voltage**
**(V_CC = 1.65 V)**
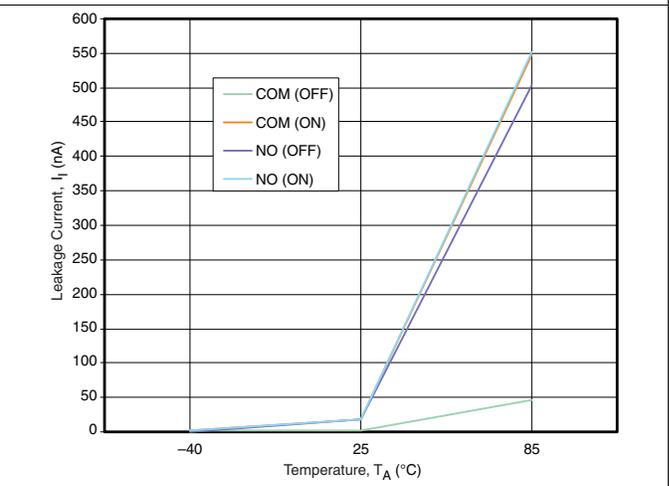


**Figure 4. Leakage Current vs Temperature (V_CC = 3.3 V)**
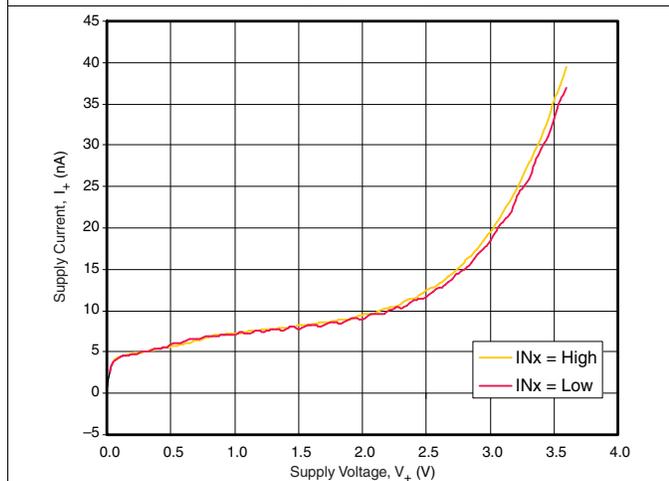


**Figure 5. Supply Current vs Supply Voltage**
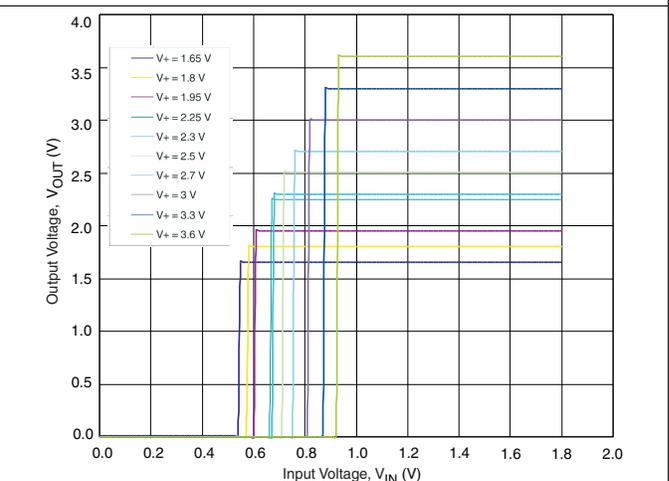


**Figure 6. Control Input Thresholds (IN1, T_A = 25°C)**

Product Folder Links: *TS3A27518E*

## Typical Characteristics (continued)
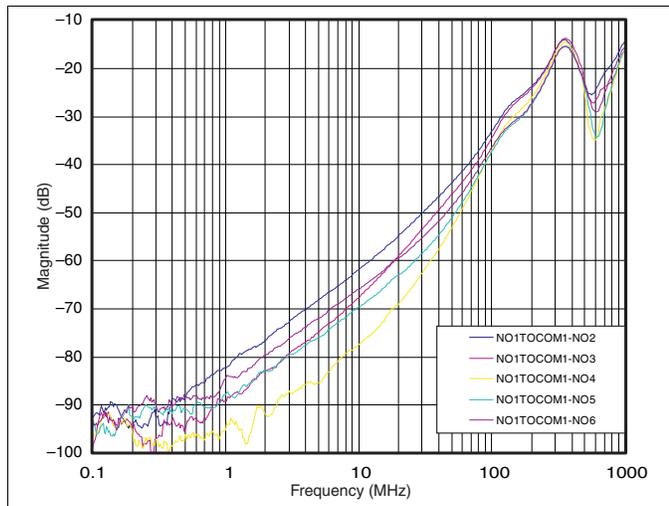


**Figure 7. Crosstalk Adjacent**
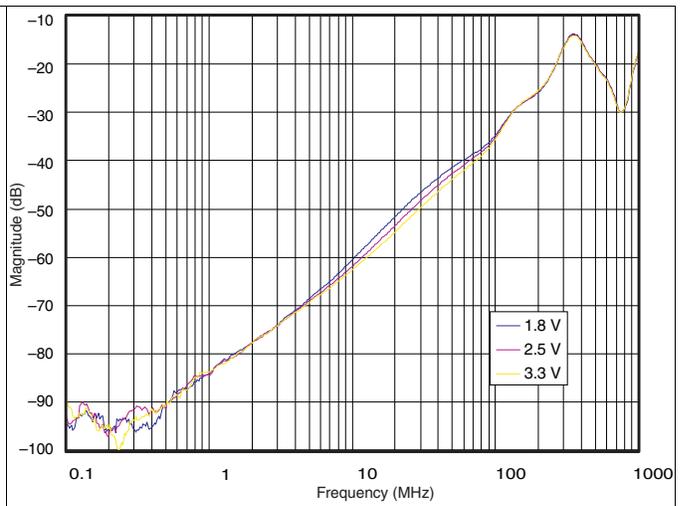


**Figure 8. Crosstalk**
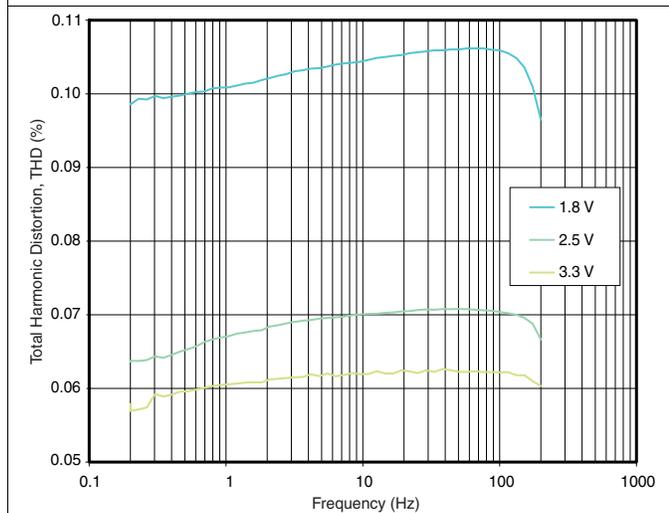


**Figure 9. Total Harmonic Distortion vs Frequency**
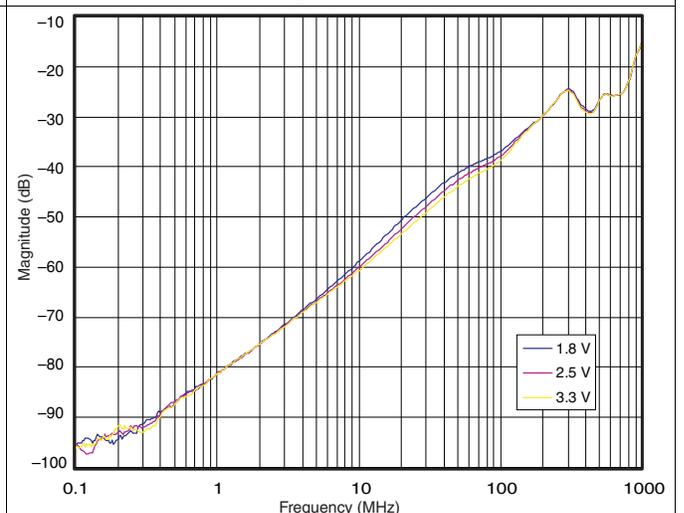


**Figure 10. OFF Isolation**
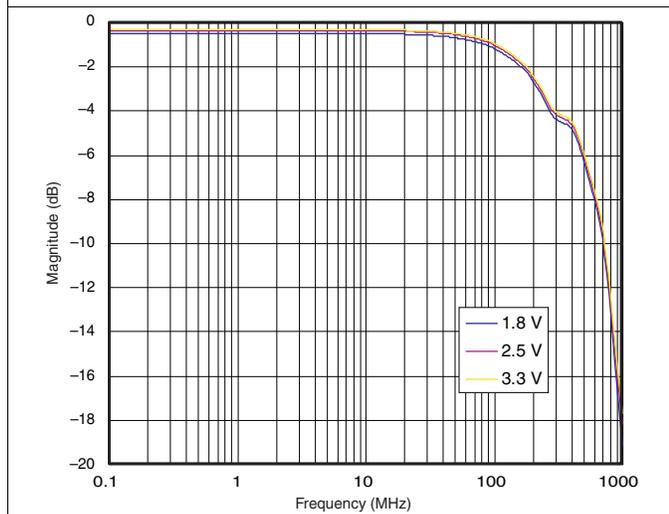


**Figure 11. Insertion Loss**
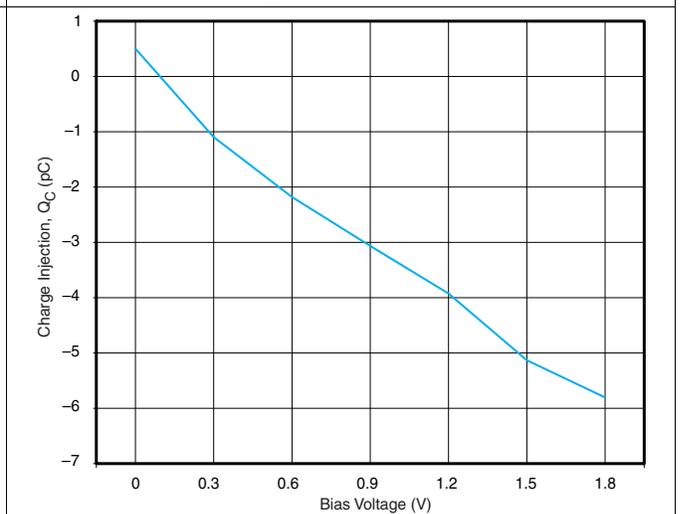


**Figure 12. Charge Injection vs Bias Voltage (1.8 V)**

Product Folder Links: *TS3A27518E*

## Typical Characteristics (continued)



**Figure 13. Charge Injection vs Bias Voltage (2.5 V)**



**Figure 14. Charge Injection vs Bias Voltage (3.3 V)**

Product Folder Links: *TS3A27518E*
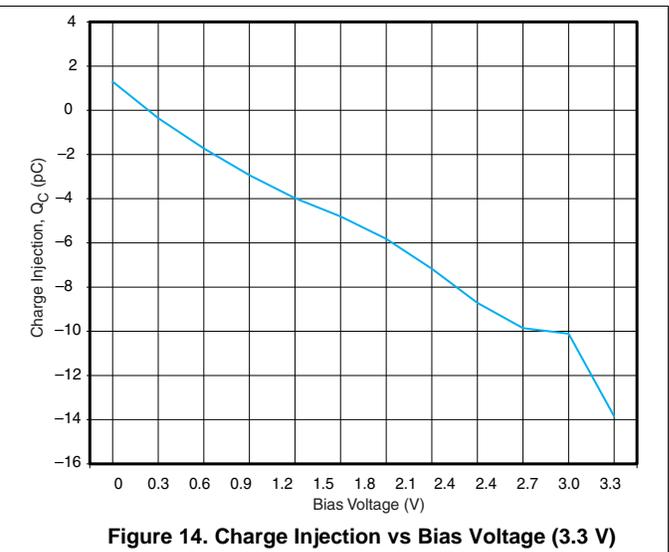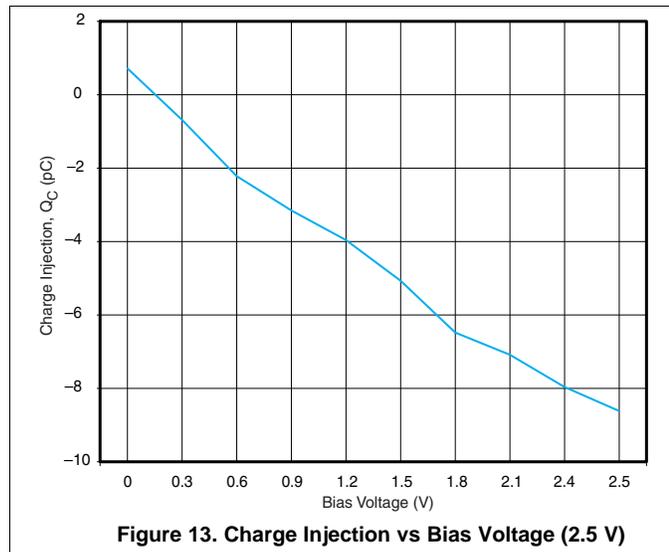
# 7 Parameter Measurement Information

**Table 1. Parameter Description**

| | DESCRIPTION |
|---|---|
| $V_{COM}$ | Voltage at COM. |
| $V_{NC}$ | Voltage at NC. |
| $V_{NO}$ | Voltage at NO. |
| $r_{on}$ | Resistance between COM and NC or NO ports when the channel is ON. |
| $\Delta r_{on}$ | Difference of $r_{on}$ between channels in a specific device. |
| $r_{on(flat)}$ | Difference between the maximum and minimum value of $r_{on}$ in a channel over the specified range of conditions. |
| $I_{NC(OFF)}$ | Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state. |
| $I_{NC(ON)}$ | Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) open. |
| $I_{NO(OFF)}$ | Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state. |
| $I_{NO(ON)}$ | Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open. |
| $I_{COM(OFF)}$ | Leakage current measured at the COM port, with the corresponding channel (COM to NC or NO) in the OFF state. |
| $I_{COM(ON)}$ | Leakage current measured at the COM port, with the corresponding channel (COM to NC or NO) in the ON state and the output (NC or NO) open. |
| $V_{IH}$ | Minimum input voltage for logic high for the control input (IN, $\overline{EN}$). |
| $V_{IL}$ | Maximum input voltage for logic low for the control input (IN, $\overline{EN}$). |
| $V_I$ | Voltage at the control input (IN, $\overline{EN}$). |
| $I_{IH}$, $I_{IL}$ | Leakage current measured at the control input (IN, $\overline{EN}$). |
| $t_{ON}$ | Turnon time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (NC or NO) signal when the switch is turning ON. |
| $t_{OFF}$ | Turnoff time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (NC or NO) signal when the switch is turning OFF. |
| $Q_C$ | Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC or NO) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_{COM}$, $C_L$ is the load capacitance, and $\Delta V_{COM}$ is the change in analog output voltage. |
| $C_{NC(OFF)}$ | Capacitance at the NC port when the corresponding channel (NC to COM) is OFF. |
| $C_{NC(ON)}$ | Capacitance at the NC port when the corresponding channel (NC to COM) is ON. |
| $C_{NO(OFF)}$ | Capacitance at the NC port when the corresponding channel (NO to COM) is OFF. |
| $C_{NO(ON)}$ | Capacitance at the NC port when the corresponding channel (NO to COM) is ON. |
| $C_{COM(OFF)}$ | Capacitance at the COM port when the corresponding channel (COM to NC) is OFF. |
| $C_{COM(ON)}$ | Capacitance at the COM port when the corresponding channel (COM to NC) is ON. |
| $C_I$ | Capacitance of control input (IN, $\overline{EN}$). |
| $O_{ISO}$ | OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM) in the OFF state. |
| $X_{TALK}$ | Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC1 to NO1). Adjacent crosstalk is a measure of unwanted signal coupling from an ON channel to an adjacent ON channel (NC1 to NC2). This is measured in a specific frequency and in dB. |
| BW | Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain. |
| THD | Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of the fundamental harmonic. |
| $I_{CC}$ | Static power-supply current with the control (IN) pin at $V_{CC}$ or GND. |
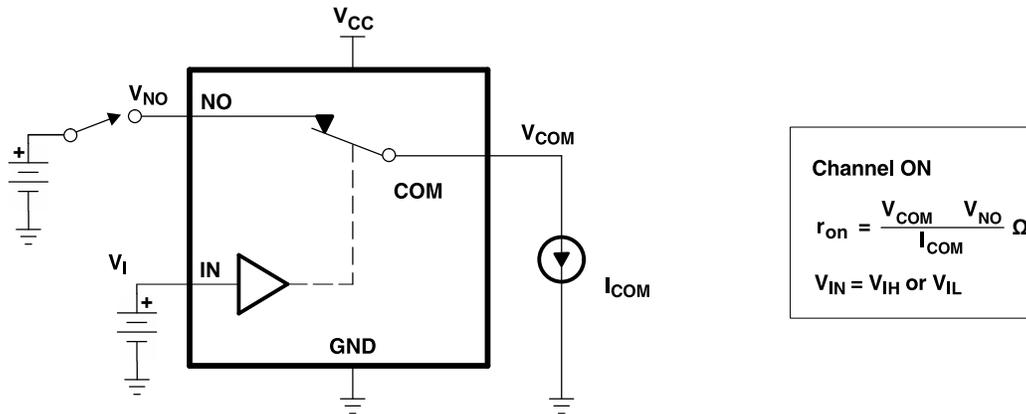
**Figure 15. ON-State Resistance ($r_{ON}$)**

$$r_{on} = \frac{V_{COM} \quad V_{NO}}{I_{COM}} \ \Omega$$

Channel ON

$V_{IN} = V_{IH}$ or $V_{IL}$
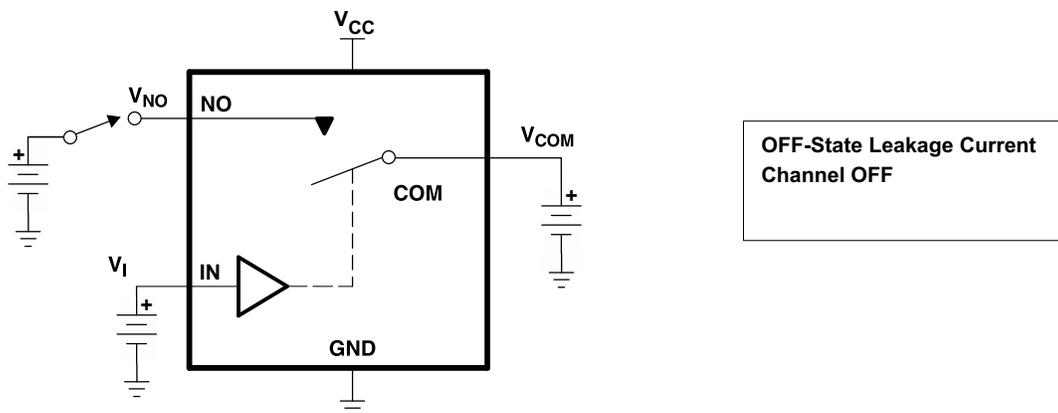


**Figure 16. OFF-State Leakage Current**
**($I_{COM(OFF)}$, $I_{NC(OFF)}$, $I_{COM(PWROFF)}$, $I_{NC(PWROFF)}$)**

OFF-State Leakage Current
Channel OFF
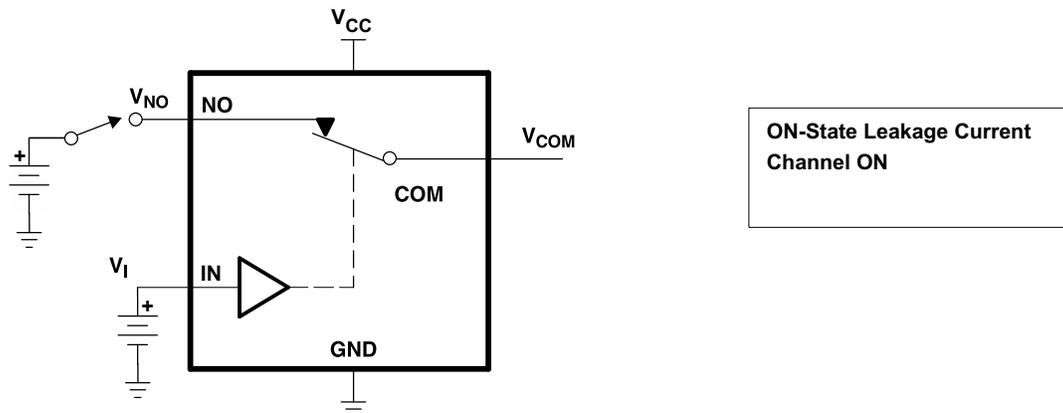


**Figure 17. ON-State Leakage Current**
**($I_{COM(ON)}$, $I_{NC(ON)}$)**

ON-State Leakage Current
Channel ON

Product Folder Links: *TS3A27518E*
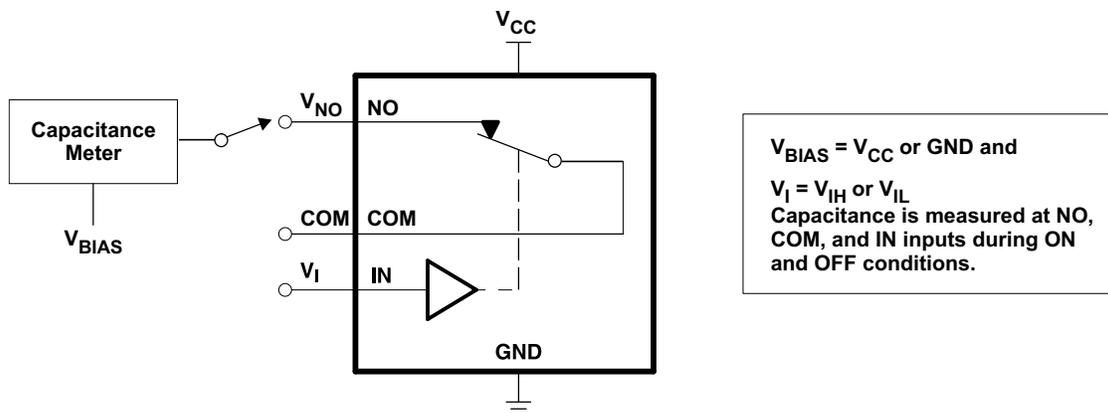
**Figure 18. Capacitance**
**($C_I$, $C_{COM(OFF)}$, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NC(ON)}$)**

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ < 5 ns, $t_f$ < 5 ns.

$C_L$ includes probe and jig capacitance.



| TEST | | | |
|---|---|---|---|
| | 50 Ω | 35 pF | |
| | 50 Ω | 35 pF | |
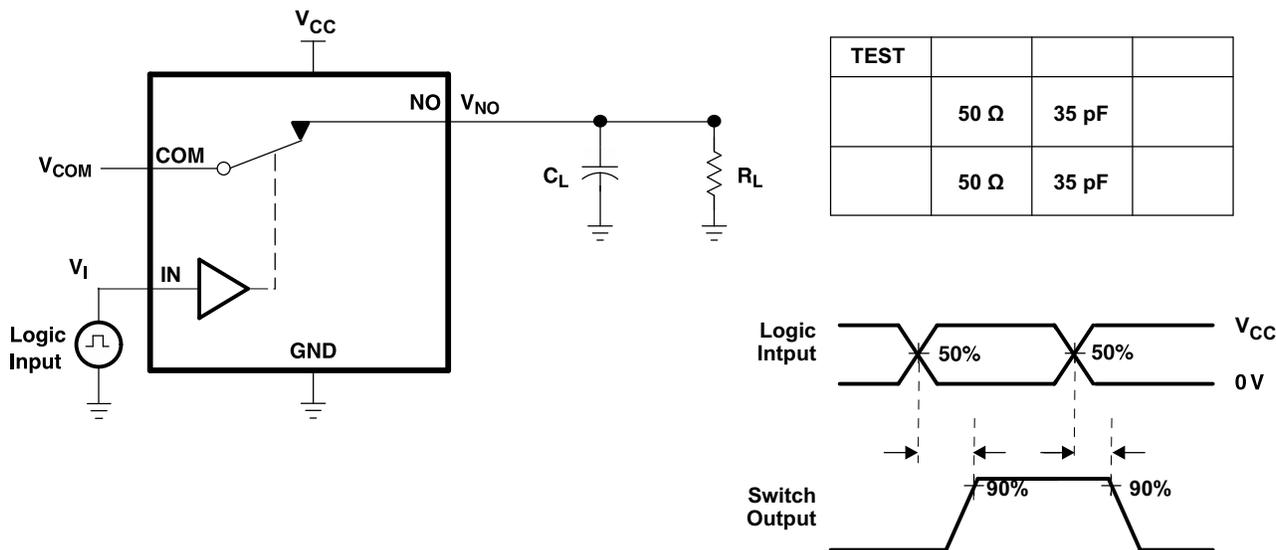
**Figure 19. Turnon ($t_{ON}$) and Turnoff Time ($t_{OFF}$)**

$C_L$ includes probe and jig capacitance.

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ < 5 ns, $t_f$ < 5 ns.

Product Folder Links: *TS3A27518E*
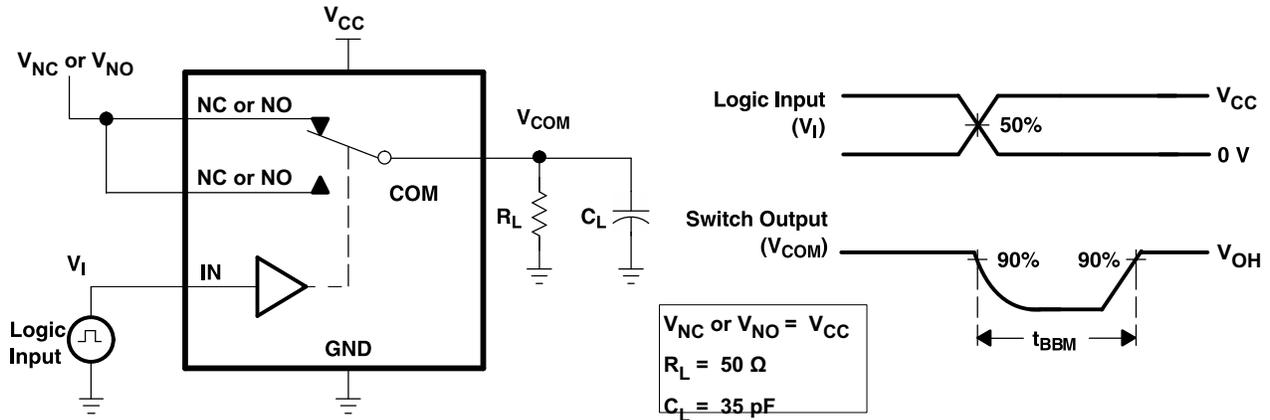
**Figure 20. Break-Before-Make Time (t$_{BBM}$)**
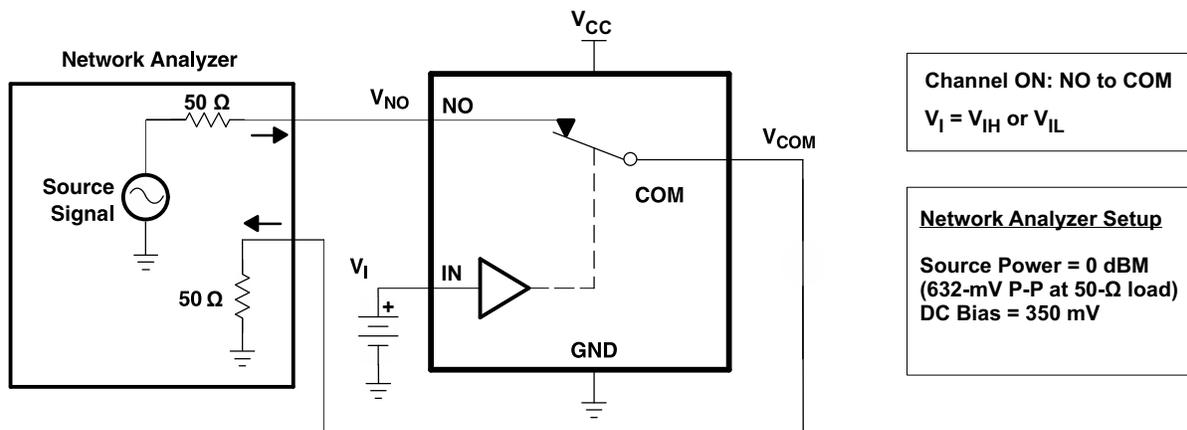


**Figure 21. Bandwidth (BW)**
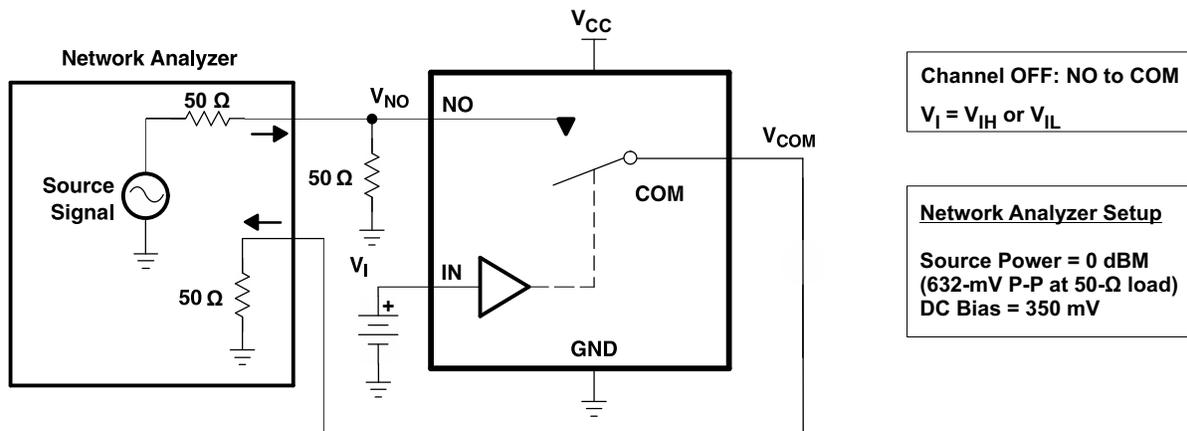


**Figure 22. OFF Isolation (O$_{ISO}$)**
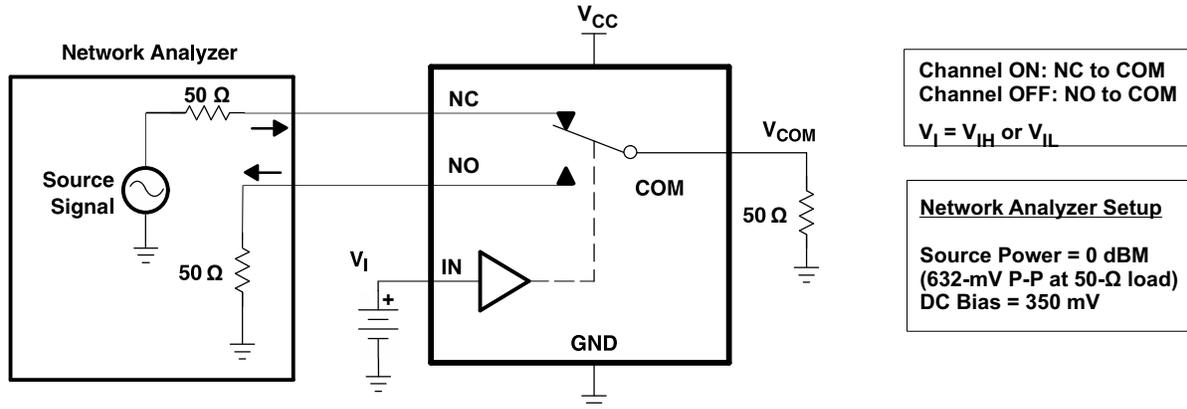
**Figure 23. Crosstalk (X$_{TALK}$)**

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ < 5 ns, $t_f$ < 5 ns.

$C_L$ includes probe and jig capacitance.
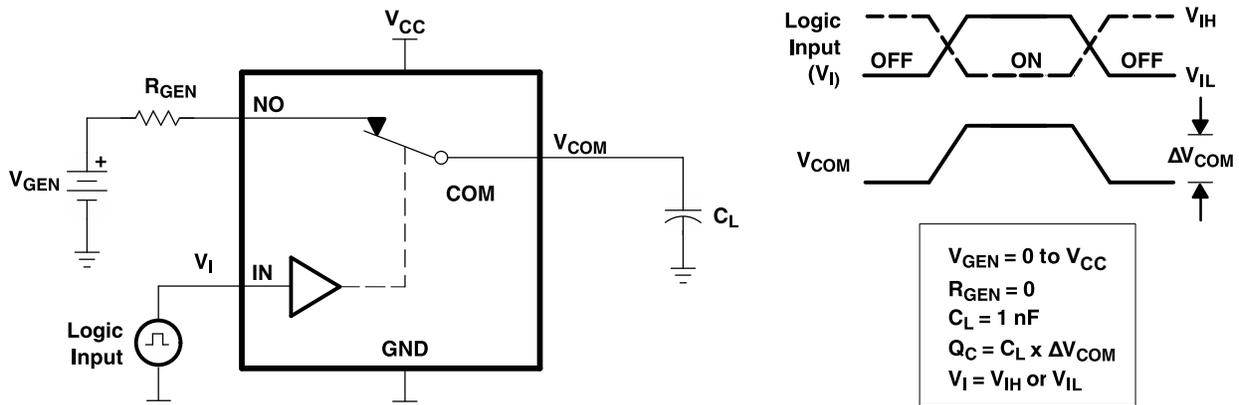


**Figure 24. Charge Injection (Q$_C$)**

$C_L$ includes probe and jig capacitance.

| | | | |
|---|---|---|---|
| **Channel ON: COM to NO** | $V_I$ = $V_{IH}$ or $V_{IL}$ | $R_L$ = 600 Ω | |
| **V$_{SOURCE}$ = V$_{CC}$ P-P** | f$_{SOURCE}$ = 20 Hz to 20 kHz | $C_L$ = 50 pF | |
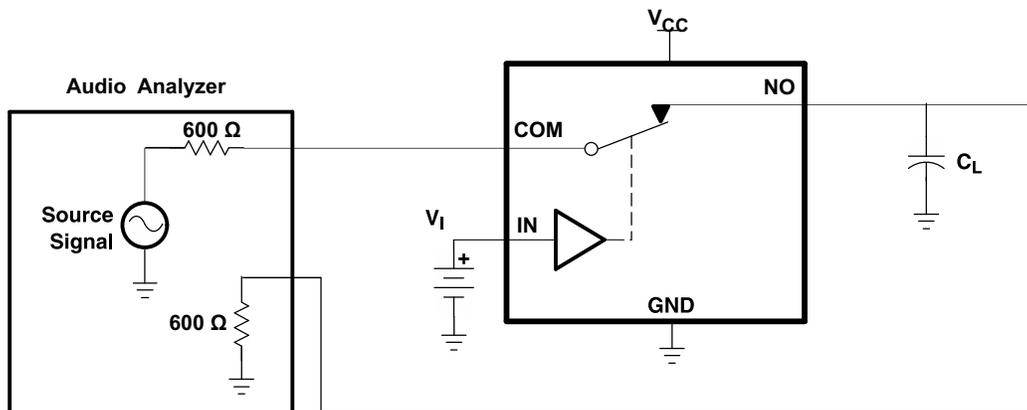


**Figure 25. Total Harmonic Distortion (THD)**

Product Folder Links: TS3A27518E

# 8 Detailed Description

## 8.1 Overview

The TS3A27518E is a bidirectional, 6-channel, 1:2 multiplexer-demultiplexer designed to operate from 1.65 V to 3.6 V. This device can handle both digital and analog signals, and can transmit signals up to $V_{CC}$ in either direction. The TS3A27518E has two control pins, each controlling three 1:2 muxes at the same time, and an enable pin that puts all outputs in high-impedance mode. The control pins are compatible with 1.8-V logic thresholds and are backward compatible with 2.5-V and 3.3-V logic thresholds.

## 8.2 Functional Block Diagram
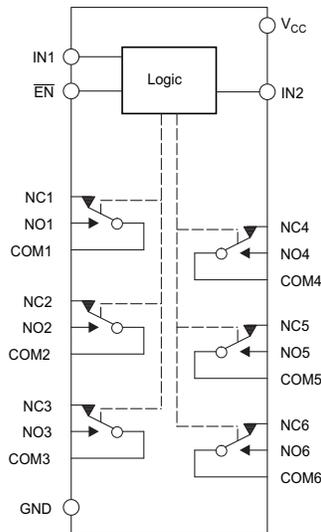


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## 8.3 Feature Description

The isolation in power-down mode, $V_{CC}$ = 0 feature places all switch paths in high-impedance state (High-Z) when the supply voltage equals 0 V.

## 8.4 Device Functional Modes

The TS3A27518E is a bidirectional device that has two sets of three single-pole double-throw switches.
Two digital signals control the 6 channels of the switch; one digital control for each set of three single-pole, double-throw switches. Digital input pin IN1 controls switches 1, 2, and 3, while pin IN2 controls switches 4, 5, and 6.

The TS3A27518 has an $\overline{EN}$ pin that when set to logic high, it places all channels into a high-impedance or HIGH-Z state. Table 2 lists the functions of TS3A27518E

### Table 2. Function Table

| $\overline{EN}$ | IN1 | IN2 | NC1/2/3 TO COM1/2/3, COM1/2/3 TO NC1/2/3 | NC4/5/6 TO COM4/5/6, COM4/5/6 TO NC4/5/6 | NO1/2/3 TO COM1/2/3, COM1/2/3 TO NO1/2/3 | NO4/5/6 TO COM4/5/6, COM4/5/6 TO NO4/5/6 |
|---|---|---|---|---|---|---|
| H | X | X | OFF | OFF | OFF | OFF |
| L | L | L | ON | ON | OFF | OFF |
| L | H | L | OFF | ON | ON | OFF |
| L | L | H | ON | OFF | OFF | ON |
| L | H | H | OFF | OFF | ON | ON |

# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The switches are bidirectional, so the NO, NC, and COM pins can be used as either inputs or outputs.

## 9.2 Typical Application
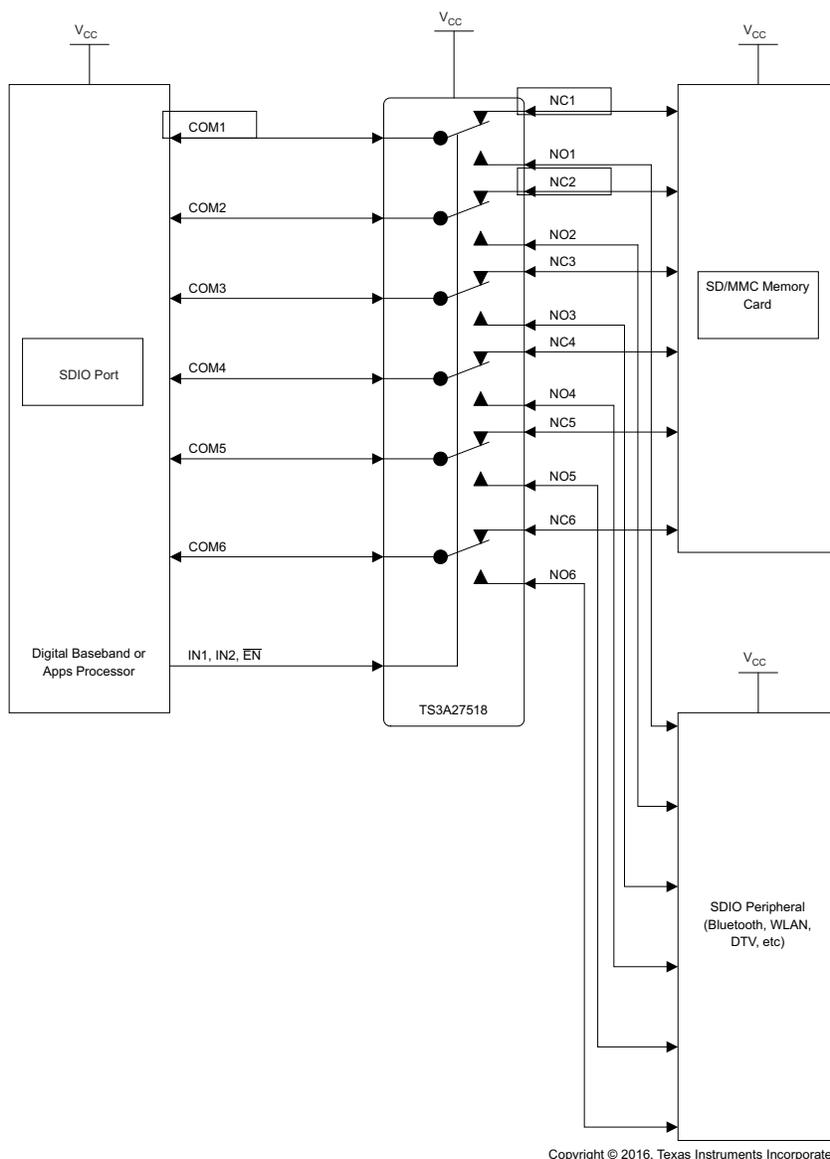


**Figure 26. SDIO Expander Application Block Diagram**

Product Folder Links: *TS3A27518E*

## Typical Application (continued)

### 9.2.1 Design Requirement

Ensure that all of the signals passing through the switch are within the recommended operating ranges to ensure proper performance, see *Recommended Operating Conditions*.

### 9.2.2 Detailed Design Procedure

The TS3A27518E can be properly operated without any external components. However, TI recommends connecting unused pins to the ground through a 50-Ω resistor to prevent signal reflections back into the device. TI also recommends that the digital control pins (INX) be pulled up to $V_{CC}$ or down to GND to avoid undesired switch positions that could result from the floating pin.

For the RTW package connect the thermal pad to ground.

### 9.2.3 Application Curve
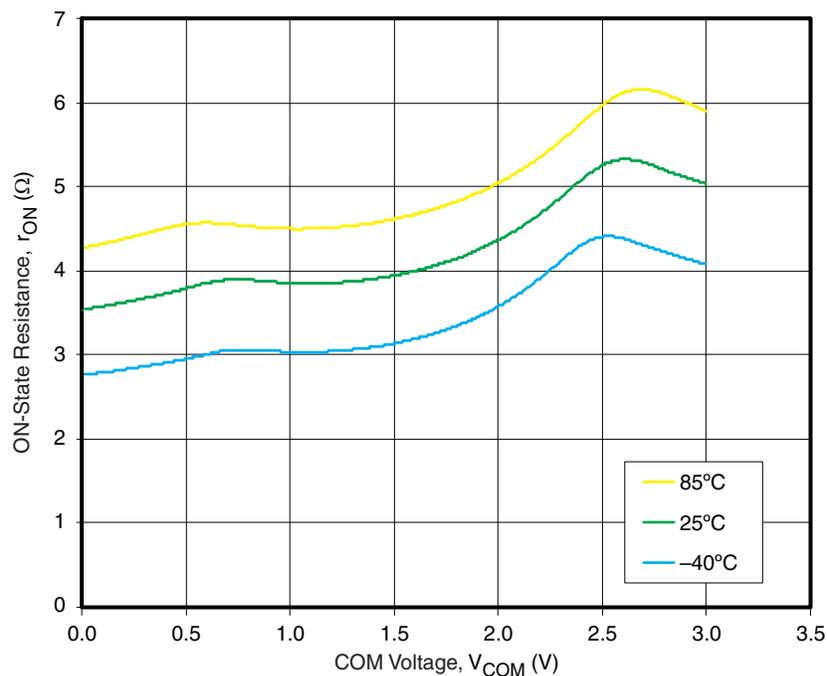


**Figure 27. ON-State Resistance vs COM Voltage ($V_{CC}$ = 3 V)**

Product Folder Links: *TS3A27518E*

# 10 Power Supply Recommendations

TI recommends proper power-supply sequencing for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the device. Always sequence $V_{CC}$ on first, followed by NO, NC, or COM. Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the $V_{CC}$ supply to other components. A 0.1-μF capacitor is adequate for most applications, if connected from $V_{CC}$ to GND.

# 11 Layout

## 11.1 Layout Guidelines

To ensure reliability of the device, TI recommends following these common printed-circuit board layout guidelines:
- Bypass capacitors should be used on power supplies, and should be placed as close as possible to the $V_{CC}$ pin
- Short trace-lengths should be used to avoid excessive loading
- For the RTW package, connect the thermal pad to ground

## 11.2 Layout Example
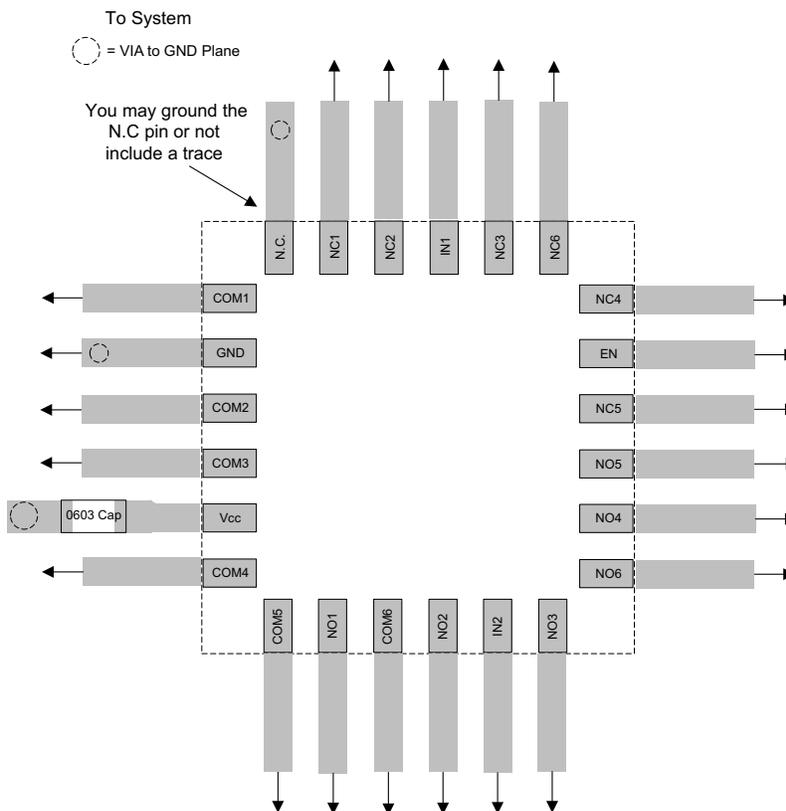


**Figure 28. WQFN Layout Recommendation**

Product Folder Links: *TS3A27518E*

## 12 Device and Documentation Support

### 12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

### 12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TS3A27518EPWR | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | YL518E | Samples |
| TS3A27518ERTWR | ACTIVE | WQFN | RTW | 24 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | YL518E | Samples |
| TS3A27518EZQSR | ACTIVE | BGA MICROSTAR JUNIOR | ZQS | 24 | 2500 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | YL518E | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TS3A27518E :**

- Automotive: TS3A27518E-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

# PACKAGE MATERIALS INFORMATION

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |
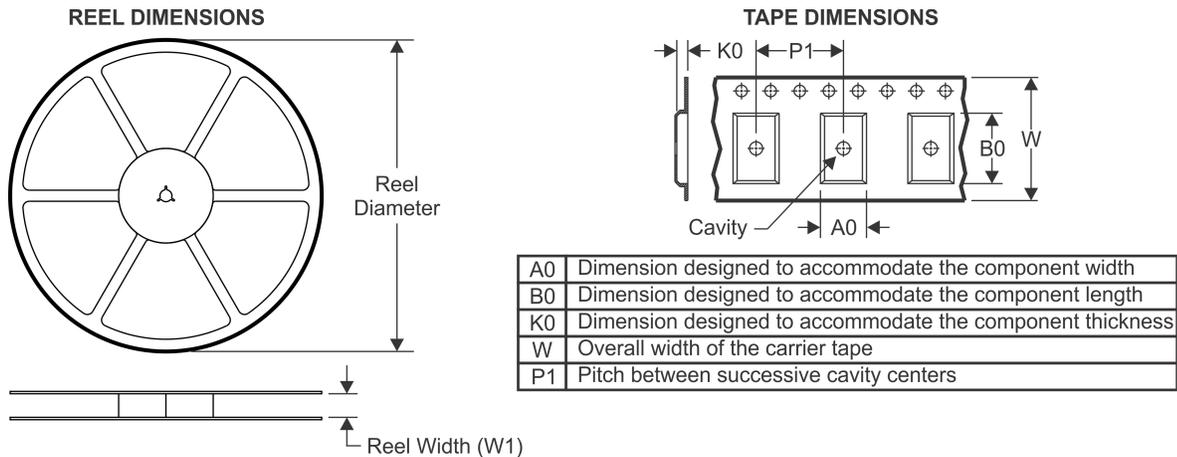
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**
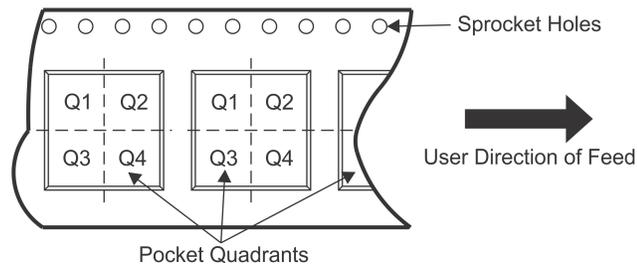
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TS3A27518EPWR | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |
| TS3A27518ERTWR | WQFN | RTW | 24 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| TS3A27518EZQSR | BGA MICROSTAR JUNIOR | ZQS | 24 | 2500 | 330.0 | 12.4 | 3.3 | 3.3 | 1.6 | 8.0 | 12.0 | Q1 |

**TAPE AND REEL BOX  DIMENSIONS**
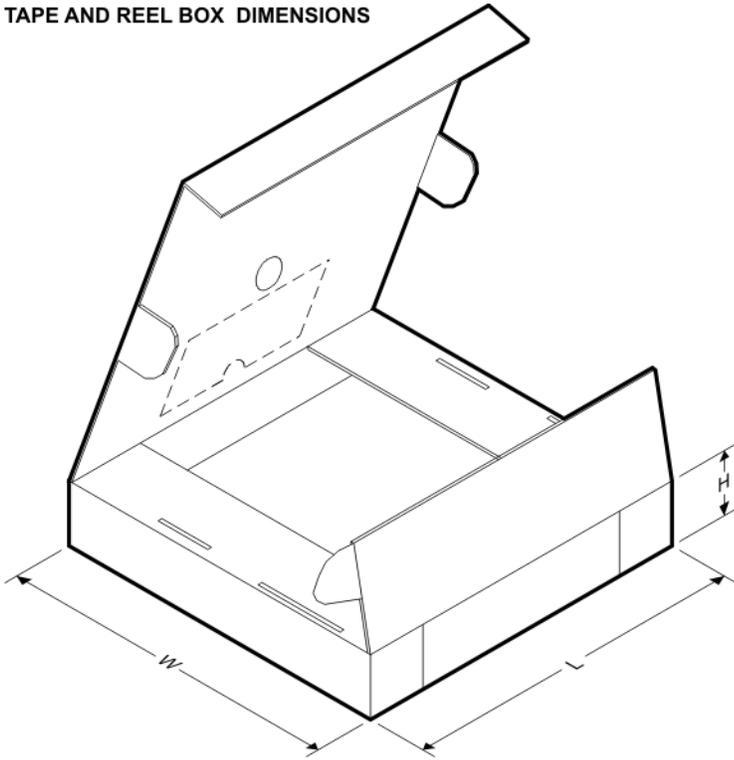


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TS3A27518EPWR | TSSOP | PW | 24 | 2000 | 367.0 | 367.0 | 38.0 |
| TS3A27518ERTWR | WQFN | RTW | 24 | 3000 | 367.0 | 367.0 | 35.0 |
| TS3A27518EZQSR | BGA MICROSTAR JUNIOR | ZQS | 24 | 2500 | 336.6 | 336.6 | 28.6 |

RTW (S−PWQFN−N24)                    PLASTIC QUAD FLATPACK NO−LEAD

$\frac{4,15}{3,85}$ A

B

$\frac{4,15}{3,85}$

PIN 1 INDEX AREA
TOP AND BOTTOM

$\frac{0,80}{0,70}$

0,20 REF.

SEATING PLANE

⌓ 0,08

$\frac{0,05}{0,00}$ C

24X $\frac{0,50}{0,30}$

0,50

1   6

24   7

THERMAL PAD

SIZE AND SHAPE
SHOWN ON SEPARATE SHEET

19   12

18   13   24X $\frac{0,30}{0,18}$

⊕ | 0,10 Ⓜ | C A B
  | 0,05 Ⓜ | C
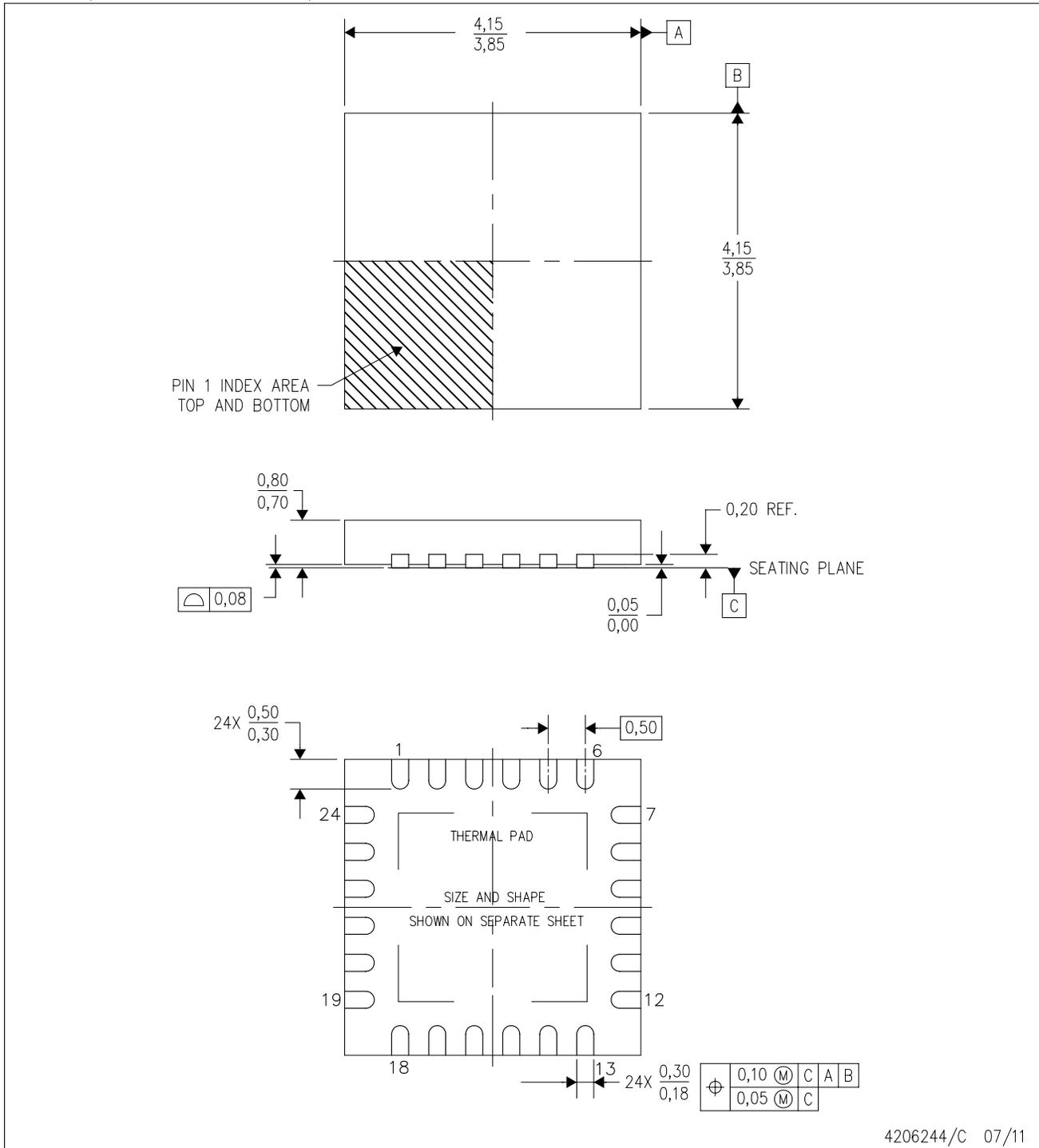
4206244/C  07/11

NOTES:   A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   Quad Flatpack, No−Leads (QFN) package configuration.
         D.   The package thermal pad must be soldered to the board for thermal and mechanical performance.
         E.   See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
         F.   Falls within JEDEC MO−220.

TEXAS
INSTRUMENTS
www.ti.com

4219135/A   11/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

LAND PATTERN EXAMPLE
SCALE: 20X

(□ 2.45)

SYMM

24

19

24X (0.6)

1

24X (0.24)

SYMM

18

(0.97)

(3.8)

25

20X (0.5)

(R0.05) TYP

6

13

(Ø0.2) TYP VIA

7

12

(0.97)

(3.8)

SOLDER MASK DETAILS

0.07 MAX ALL AROUND

METAL

SOLDER MASK OPENING

NON SOLDER MASK DEFINED (PREFERRED)

0.07 MIN ALL AROUND

SOLDER MASK OPENING

METAL UNDER SOLDER MASK
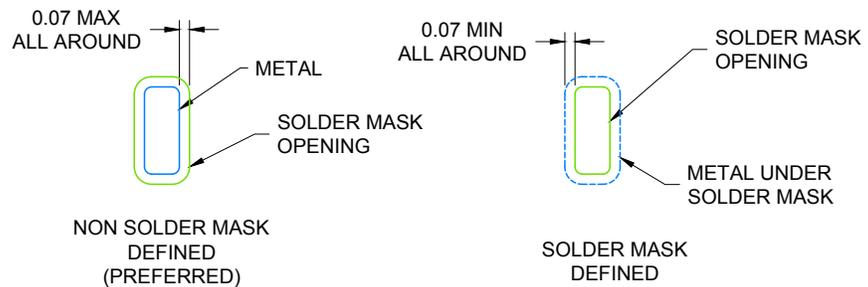
SOLDER MASK DEFINED

4219135/A   11/2016

NOTES: (continued)

3.    For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .

4X(□ 1.08)

(0.64) TYP

(R0.05) TYP

24

19

24X (0.6)

1

25

18

24X (0.24)

(0.64)
TYP

20X (0.5)

SYMM
₵

(3.8)

6

13

METAL
TYP

7

12

SYMM
₵

(3.8)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25:
78% PRINTED COVERAGE BY AREA UNDER PACKAGE
SCALE: 20X

4219135/A   11/2016

NOTES: (continued)

4.   Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
     design recommendations.

PW (R−PDSO−G24)                                    PLASTIC SMALL OUTLINE
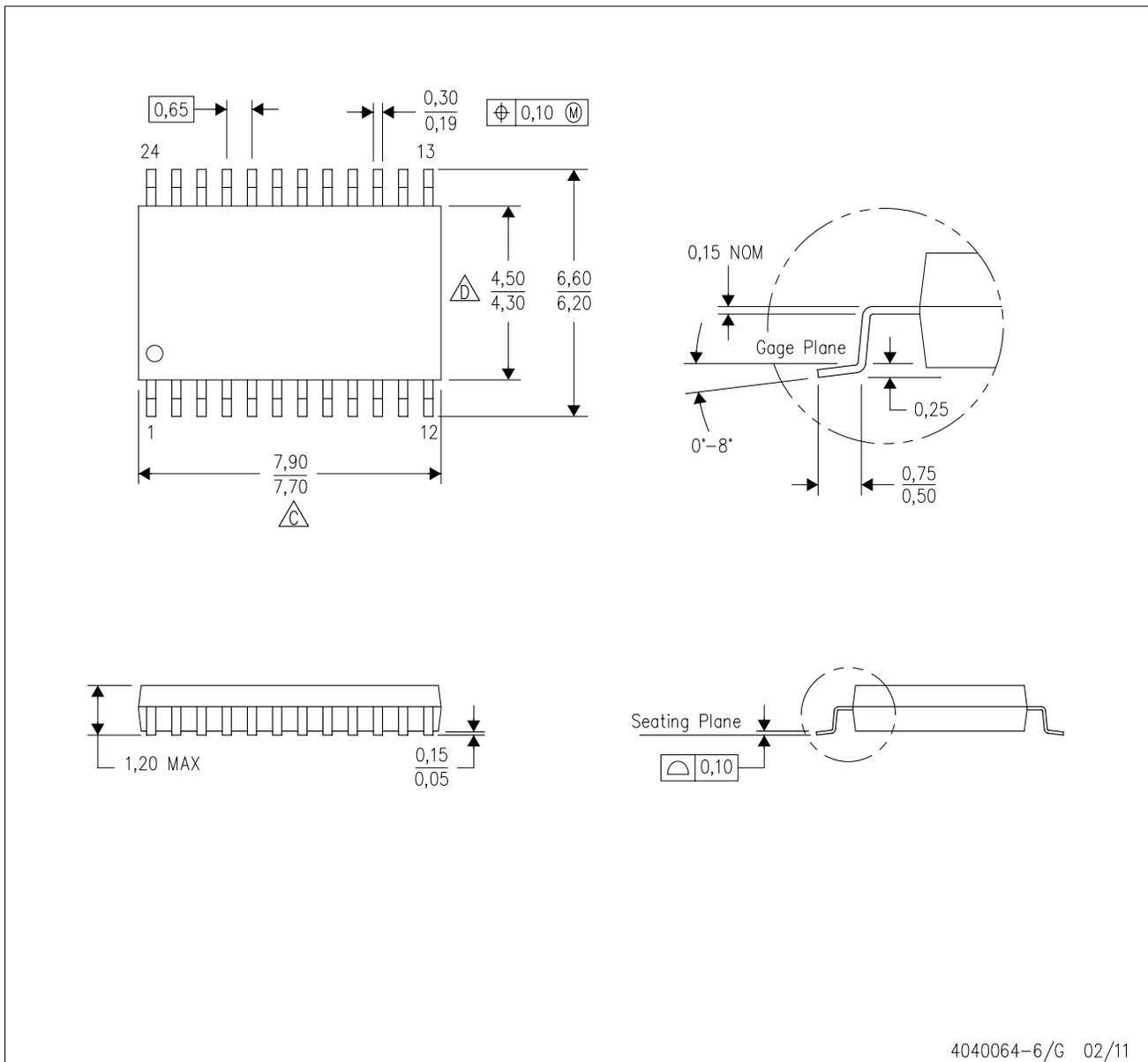


4040064−6/G  02/11

NOTES:   A.   All linear dimensions are in millimeters.  Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   Body length does not include mold flash, protrusions, or gate burrs.  Mold flash, protrusions, or gate burrs shall
              not exceed 0,15 each side.
         D.   Body width does not include interlead flash.  Interlead flash shall not exceed 0,25 each side.
         E.   Falls within JEDEC MO−153

PW (R−PDSO−G24)                              PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

22x0,65

24x0,25

1,55

5,6

5,6

22x0,65

Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
(See Note E)

0,3

1,6

0,07
All Around

Pad Geometry
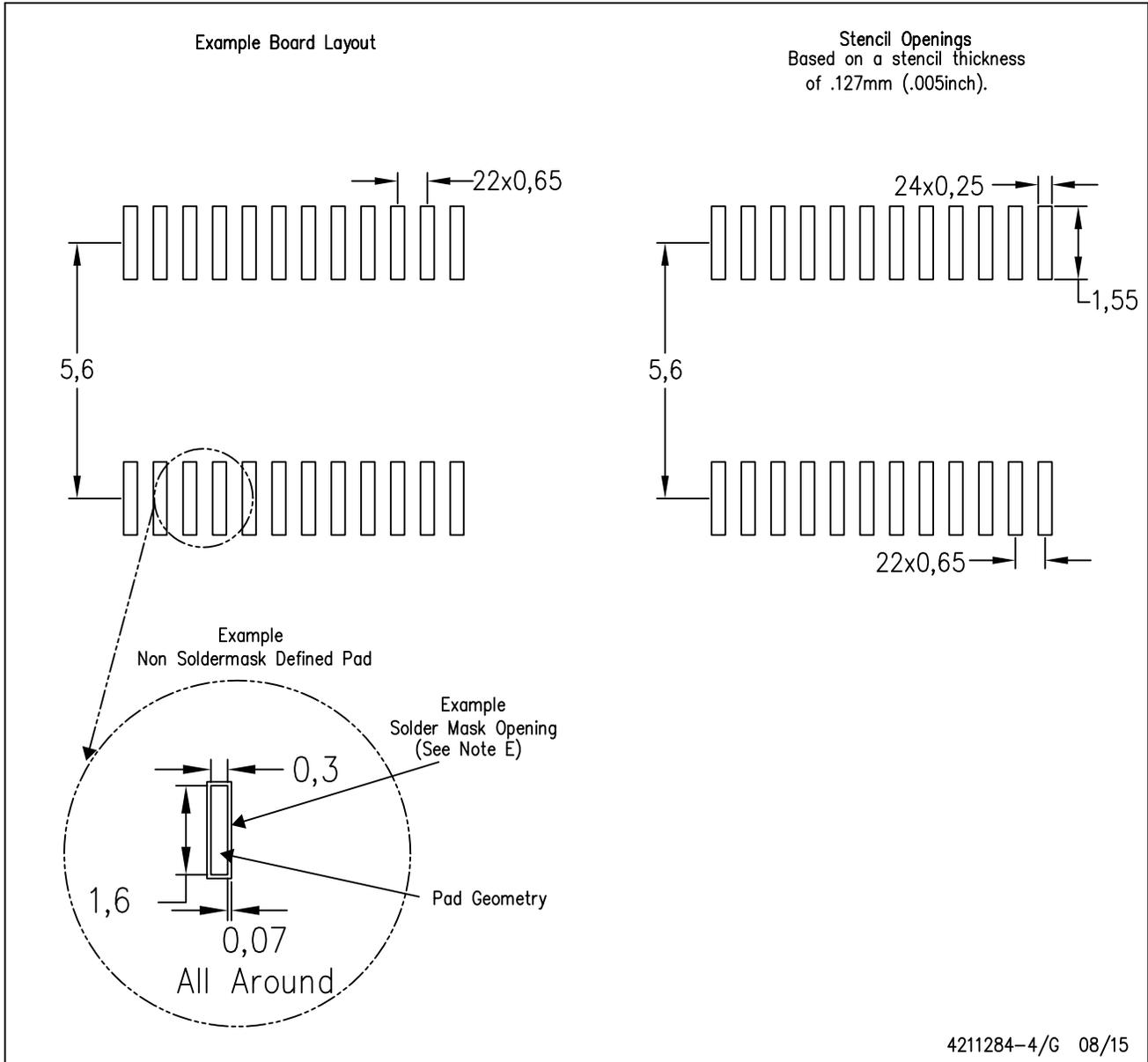
4211284−4/G   08/15

NOTES:   A.  All linear dimensions are in millimeters.
         B.  This drawing is subject to change without notice.
         C.  Publication IPC−7351 is recommended for alternate design.
         D.  Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.  Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
         E.  Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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ZQS (S−PBGA−N24)                    PLASTIC BALL GRID ARRAY
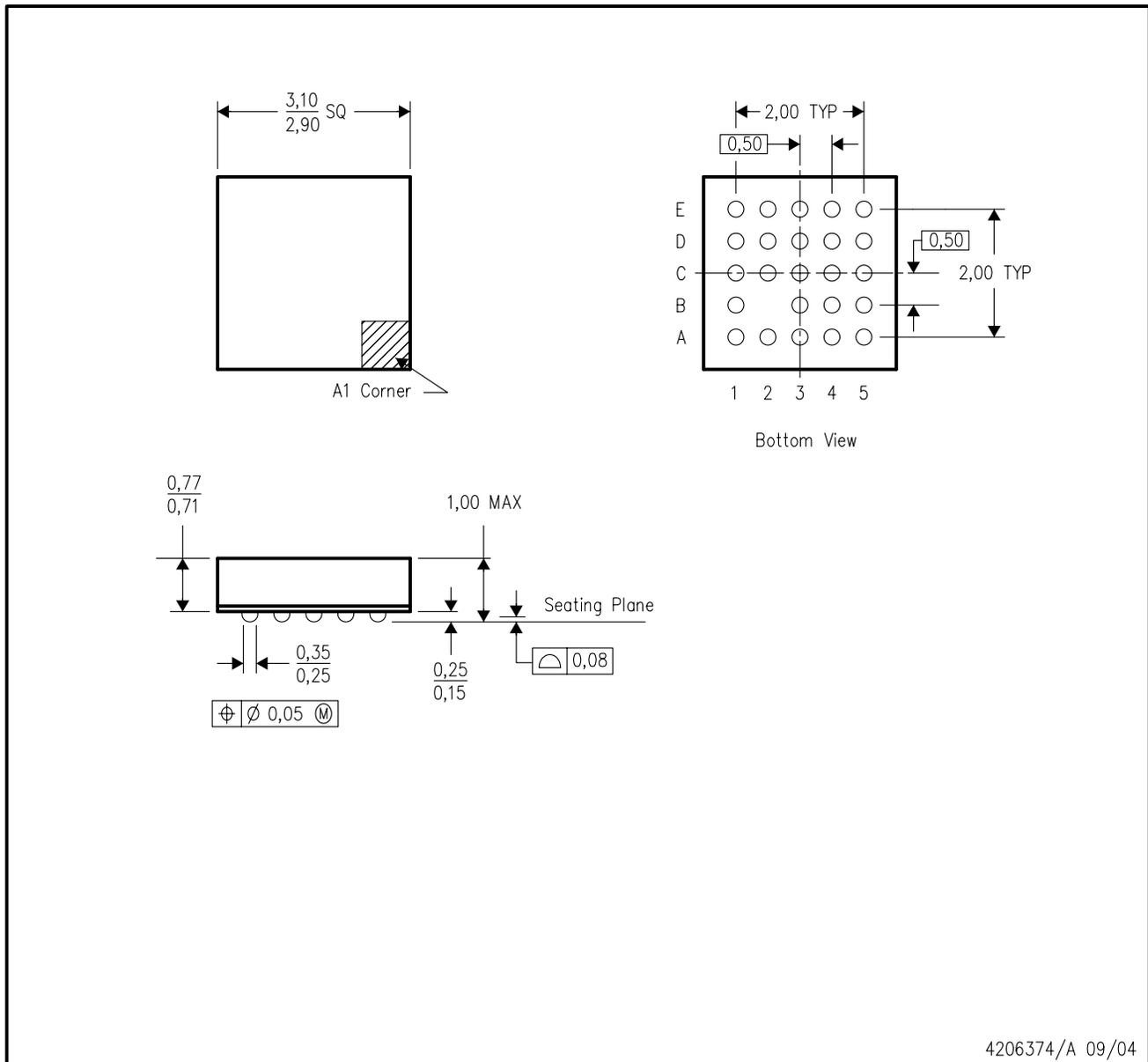


NOTES:   A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Falls within JEDEC MO−225
         D.   This package is lead−free.

# IMPORTANT NOTICE