

12-Channel 1:2 MUX/DEMUX Switch with Integrated 4-Channel Sideband Signal Switching for DVI/HDMI and DisplayPort (DP) Applications

Check for Samples: [TS3DV621](#)

FEATURES

- **Switch Type:** 2:1 or 1:2
- **Data Rate Compatibility**
 - HDMI v1.4
 - DVI 1.0
 - DisplayPort 1.1a
- **Bandwidth (-3dB) – 2.2 GHz**
- **R_{ON} – 8 Ω**
- **C_{ON} – 5.6 pF**
- **V_{CC} Range – 3.0V–3.6 V**
- **I/O Voltage Range – 0–5 V**
- **Bit-to-Bit Skew – 6 ps Typical**
- **Propagation Delay – 40 ps Typical**
- **Special Features**
 - **Dedicated Enable Logic Supports Hi-Z Mode**
 - **I_{OFF} Protection Prevents Current Leakage in Powered Down State (V_{CC} = 0 V)**
- **ESD Performance**
 - **2kV Human Body Model (A114B, Class II)**
 - **1kV Charged Device Model (C101)**
- **42-pin QFN Package (9 x 3.5 mm, 0.5 mm Pitch)**

APPLICATIONS

- **DVI/HDMI/DisplayPort Signal Switching**
- **General Purpose TMDS/LVDS Signal Switching**

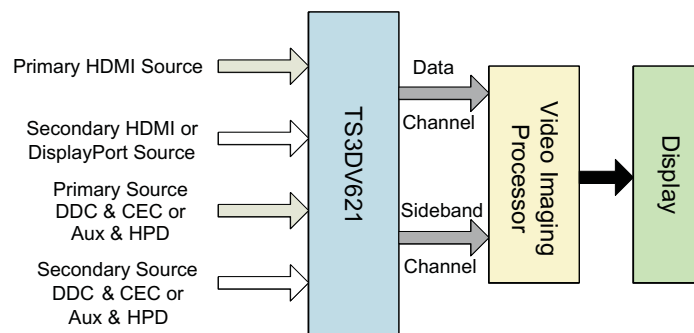
DESCRIPTION

The TS3DV621 is a 1:2 or 2:1 bi-directional multiplexer/demultiplexer with an integrated 4 side-band control channel (DDC, AUX, CEC, or HPD) signal switcher. Operating from a 3 to 3.6V supply, the TS3DV621 offers low and flat ON-state resistance as well as low I/O capacitance, which allows the TS3DV621 to achieve a typical bandwidth of 2.2 GHz. The device provides the high bandwidth necessary for HDMI, DVI, and DisplayPort applications. The TS3DV621 expands the high-speed physical link interface from a single HDMI port to two HDMI ports (A or B port) or vice-versa. It can also be used for DisplayPort (DP) source/sink applications. The integrated side-band control channels allow 5V signals to pass through, making the TS3DV621 suitable for HDMI applications.

The most common application for the TS3DV621 is the sink application. In this case, there are two possible sources (DVD, set-top box, or game console) that are routed to one receiver. The unselected port is in the high-impedance mode, such that the receiver receives information from only one source. HDCP encryption is passed through the switch for the receiver to decode.

ORDERING INFORMATION

For package and ordering information, see the Package Option Addendum at the end of this document.


Figure 1. Multiplexing Dual Video Input Source (HDMI/DisplayPort)


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN FUNCTIONS

	PIN		I/O TYPE	DESCRIPTION
	NAME	NO.		
VCC	1, 17, 30	Power	Supply Voltage	
GND	PowerPad	Ground	Ground	
EN	8	I	Enable Input	
SEL1	9	I	Select Input 1	
SEL2	10	I	Select Input 2	
D0+	41	I/O	Port A, Lane 0, +ve signal	
D0-	39	I/O	Port A, Lane 0, -ve signal	
D1+	38	I/O	Port A, Lane 1, +ve signal	
D1-	36	I/O	Port A, Lane 1, -ve signal	
D2+	34	I/O	Port A, Lane 2, +ve signal	
D2-	32	I/O	Port A, Lane 2, -ve signal	
D3+	29	I/O	Port A, Lane 3, +ve signal	
D3-	27	I/O	Port A, Lane 3, -ve signal	
D0+B	42	I/O	Port B, Lane 0, +ve signal	
D0-B	40	I/O	Port B, Lane 0, -ve signal	
D1+B	37	I/O	Port B, Lane 1, +ve signal	
D1-B	35	I/O	Port B, Lane 1, -ve signal	
D2+B	33	I/O	Port B, Lane 2, +ve signal	
D2-B	31	I/O	Port B, Lane 2, -ve signal	
D3+B	28	I/O	Port B, Lane 3, +ve signal	
D3-B	26	I/O	Port B, Lane 3, -ve signal	
D0+	2	I/O	Common Port, Lane 0, +ve signal	
D0-	3	I/O	Common Port, Lane 0, -ve signal	
D1+	4	I/O	Common Port, Lane 1, +ve signal	
D1-	5	I/O	Common Port, Lane 1, -ve signal	
D2+	6	I/O	Common Port, Lane 2, +ve signal	
D2-	7	I/O	Common Port, Lane 2, -ve signal	
D3+	11	I/O	Common Port, Lane 3, +ve signal	
D3-	12	I/O	Common Port, Lane 3, -ve signal	
AUX+A	25	I/O	+ve AUX Channel for Port A	
AUX-A	23	I/O	-ve AUX Channel for Port A	
HPDA	21	I/O	Port A HPD	
CECA	19	I/O	Port A CEC	
AUX+B	24	I/O	+ve AUX Channel for Port B	
AUX-B	22	I/O	-ve AUX Channel for Port B	
HPDB	20	I/O	Port B HPD	
CECB	18	I/O	Port B CEC	
AUX+	13	I/O	+ve AUX Channel for Common Port	
AUX-	14	I/O	-ve AUX Channel for Common Port	
HPD	15	I/O	HPD for Common Port	
CEC	16	I/O	CEC for Common Port	

LOGIC DIAGRAM

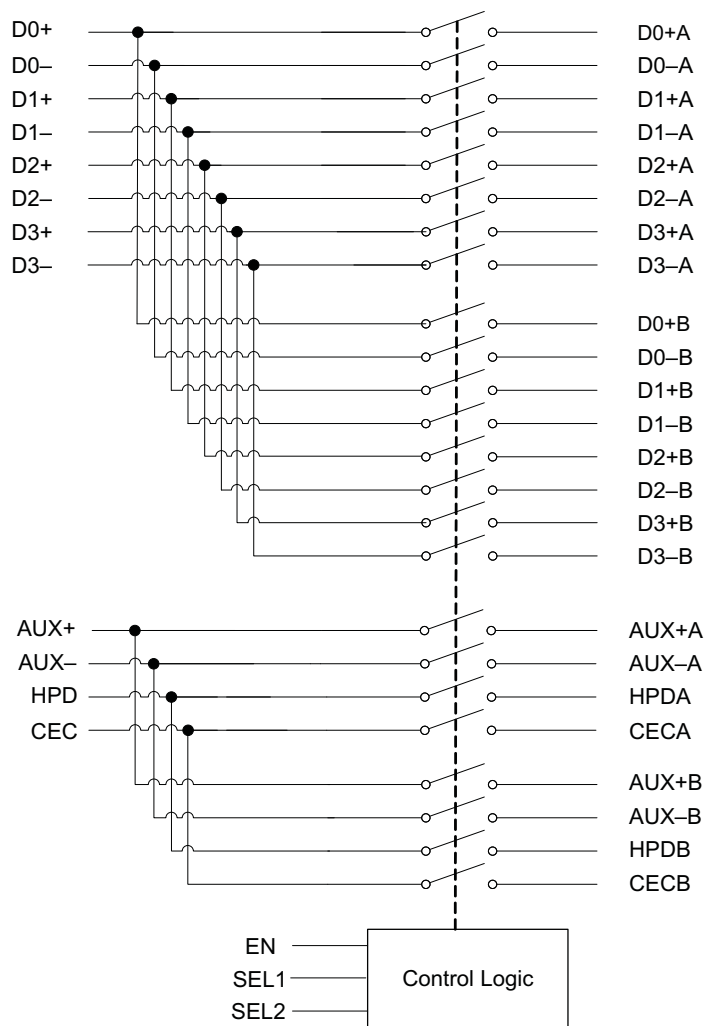


Table 1. FUNCTION TABLE

EN	SEL1	SEL2	FUNCTION
L	X	X	All I/O = High Impedance
H	L ⁽¹⁾	L ⁽¹⁾	Output port A = Input Output Port B = High Impedance
H	H ⁽¹⁾	H ⁽¹⁾	Output Port A = High Impedance Output Port B = Input

(1) Tie SEL1 and SEL2 together for easy output control

TS3DV621

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APPLICATION EXAMPLES

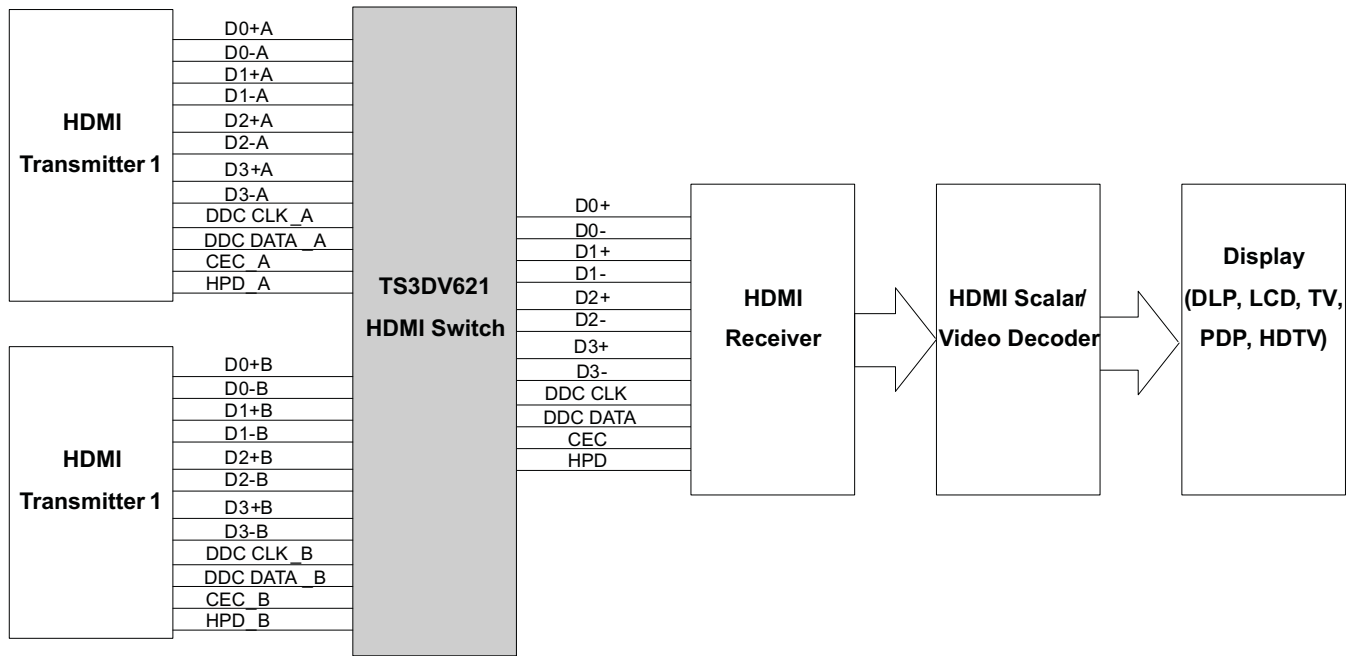


Figure 2. Dual HDMI Source Application

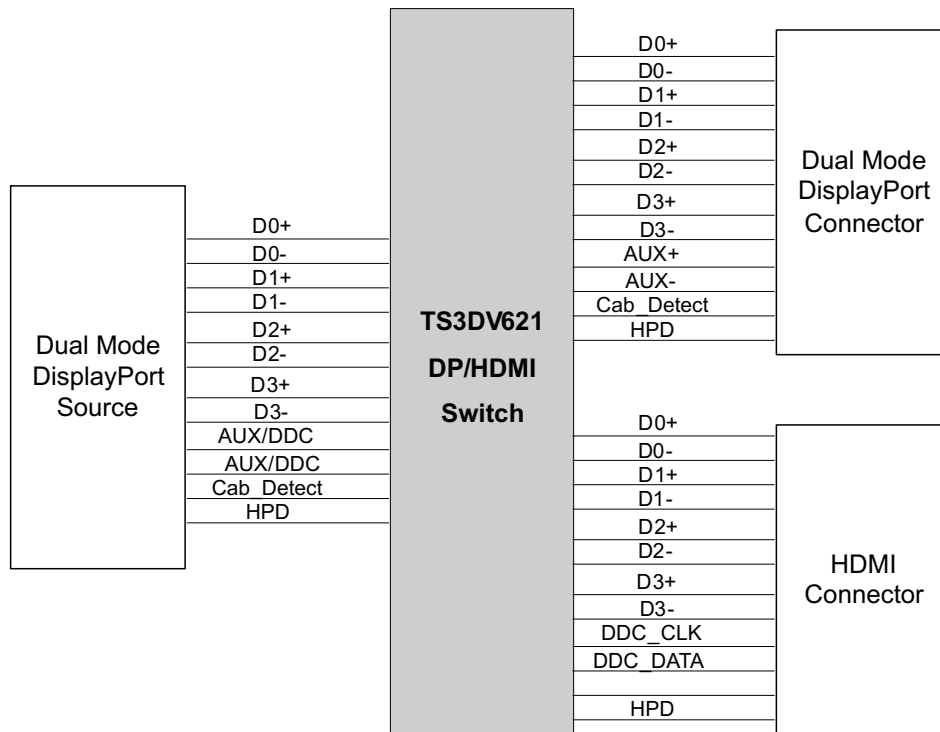


Figure 3. Dual-Mode DisplayPort Application

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	4.6	V
V _{I/O}	Analog voltage range ⁽²⁾⁽³⁾⁽⁴⁾	All I/O	-0.5	7	V
V _{IN}	Digital input voltage range ⁽²⁾⁽³⁾	SEL1, SEL2	-0.5	7	V
I _{I/OK}	Analog port diode current	V _{I/O} < 0		-50	mA
I _{IK}	Digital input clamp current	V _{IN} < 0		-50	mA
I _{I/O}	On-state switch current ⁽⁵⁾	All I/O	-128	128	mA
I _{DD} I _{GND}	Continuous current through V _{DD} or GND		-100	100	mA
θ _{JA}	Package thermal impedance ⁽⁶⁾	RUA package		31.8	°C/W
T _{stg}	Storage temperature range		-65	150	°C

- (1) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4) V_I and V_O are used to denote specific conditions for V_{I/O}.
- (5) I_I and I_O are used to denote specific conditions for I_{I/O}.
- (6) The package thermal impedance is calculated in accordance with JESD 51-7

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		3	3.6	V
V _{IH}	High-level control input voltage	SEL1, SEL2	2	5.5	V
V _{IL}	Low-level control input voltage	SEL1, SEL2	0	0.8	V
V _{IN}	Input voltage	SEL1, SEL2	0	5.5	V
V _{I/O}	Input/Output voltage		0	5.5	V
T _A	Operating free-air temperature		-40	85	°C

- (1) All unused control inputs of the device must be held at VDD or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

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ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS ⁽¹⁾		MIN	TYP ⁽²⁾	MAX	UNIT
V _{IK}	Digital input clamp voltage	SEL1,SEL2	V _{CC} = 3.6 V, I _{IN} = -18 mA	-1.2	-0.8		V
R _{ON}	On-state resistance	All I/O	V _{CC} = 3 V, 1.5 V ≤ V _{I/O} ≤ V _{CC} , I _{I/O} = -40 mA		8	12	Ω
R _{ON(flat)} ⁽³⁾	On-state resistance flatness	All I/O	V _{CC} = 3 V, V _{I/O} = 1.5 V and V _{CC} , I _{I/O} = -40mA		1.5		Ω
ΔR _{ON} ⁽⁴⁾	On-state resistance match between channels	All I/O	V _{CC} = 3 V, 1.5 V ≤ V _{I/O} ≤ V _{CC} , I _{I/O} = -40mA		0.4	1	Ω
I _{IH}	Digital input high leakage current	SEL1,SEL2	V _{CC} = 3.6 V, V _{IN} = V _{DD}			±1	μA
I _{IL}	Digital input low leakage current	SEL1,SEL2	V _{CC} = 3.6 V, V _{IN} = GND			±1	μA
I _{OFF}	Leakage under power off conditions	All outputs	V _{CC} = 0 V, V _{I/O} = 0 to 3.6 V, V _{IN} = 0 to 5.5V			±1	μA
C _{IN}	Digital input capacitance	SEL1,SEL2	f = 1 MHz, V _{IN} = 0 V		2.6	3.2	pF
C _{OFF}	Switch OFF capacitance	All I/O	f = 1 MHz, V _{I/O} = 0 V, Output is open, Switch is OFF		2		pF
C _{ON}	Switch ON capacitance	All I/O	f = 1 MHz, V _{I/O} = 0 V, Output is open, Switch is ON		5.6		pF
I _{CC}	VCC supply current		V _{CC} = 3.6 V, I _{I/O} = 0, V _{IN} = V _{DD} or GND		300	400	μA

- (1) V_I, V_O, I_I, and I_O refer to I/O pins, V_{IN} refers to the control inputs
(2) All typical values are at V_{CC} = 3.3V (unless otherwise noted), T_A = 25°C
(3) R_{ON(FLAT)} is the difference of R_{ON} in a given channel at specified voltages.
(4) ΔR_{ON} is the difference of R_{ON} from center port to any other ports.

SWITCHING CHARACTERISTICS

Over recommended operation free-air temperature range, V_{CC} = 3.3 V ± 0.3 V, R_L = 200 Ω, C_L = 4 pF (unless otherwise noted) (see and)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP ⁽¹⁾	MAX	UNIT
t _{pd} ⁽²⁾	All I/O input side	All I/O output side		40		ps
t _{PZH} , t _{PZL}	SEL1, SEL2	All I/O		2	7	ns
t _{PHZ} , t _{PLZ}	SEL1, SEL2	All I/O		2	5	ns
t _{sk(o)} ⁽³⁾	All I/O input side	All I/O output side		6	30	ps
t _{sk(p)} ⁽⁴⁾				6	30	ps

- (1) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
(2) The propagation delay is the calculated RC time constant of the typical ON-State resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).
(3) Output skew between center port and any other channel.
(4) Skew between opposite transitions of the same output |t_{PHL} - t_{PLH}|

DYNAMIC CHARACTERISTICS

Over recommended operation free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP ⁽¹⁾	UNIT
XTALK	R _L = 50 Ω, f = 250 MHz (Figure 11)	-43	dB
OIRR	R _L = 50 Ω, f = 250 MHz (Figure 12)	-42	dB
BW	R _L = 50 Ω, Switch ON (Figure 10)	2.2	GHz

- (1) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

OPERATING CHARACTERISTICS

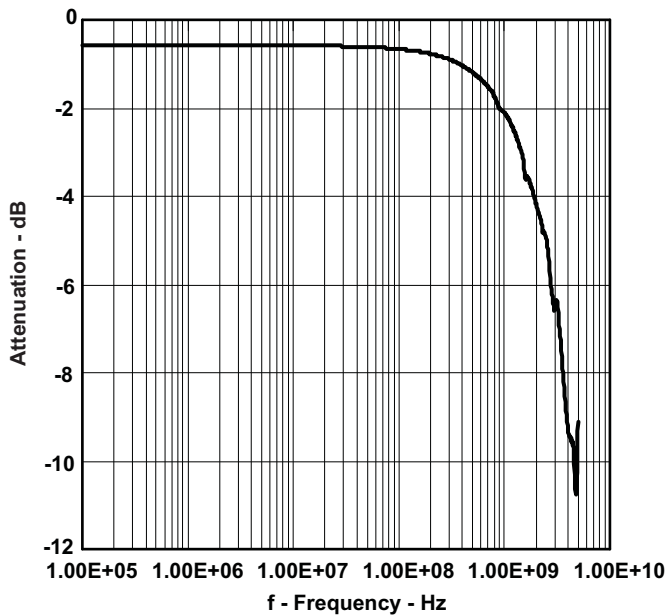


Figure 4. Gain vs Frequency

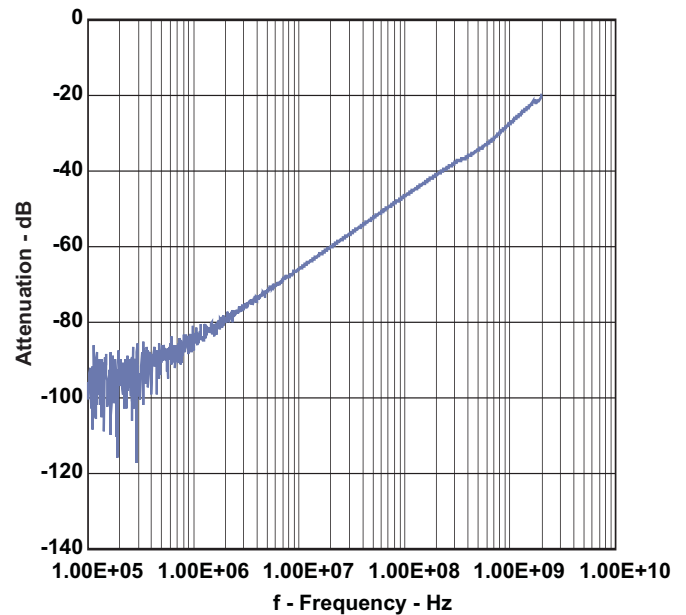


Figure 5. Off Isolation vs Frequency

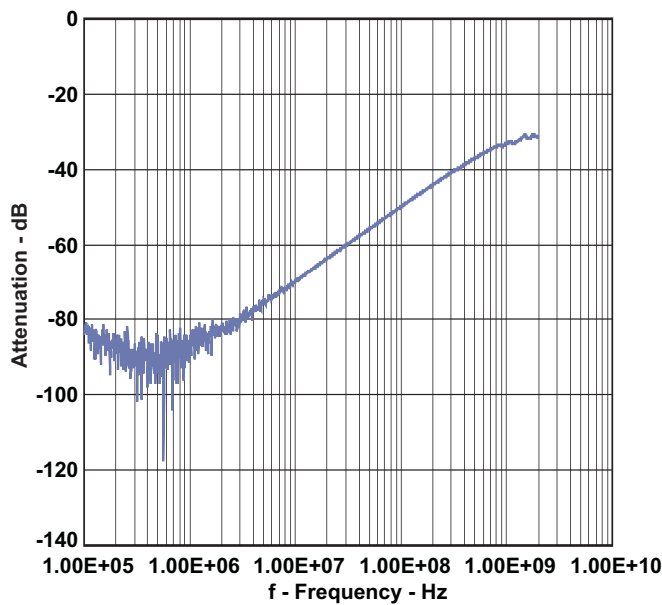


Figure 6. Crosstalk vs Frequency

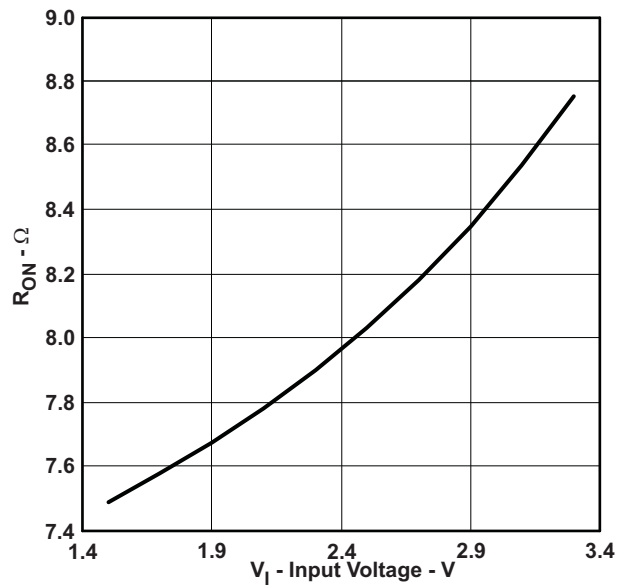
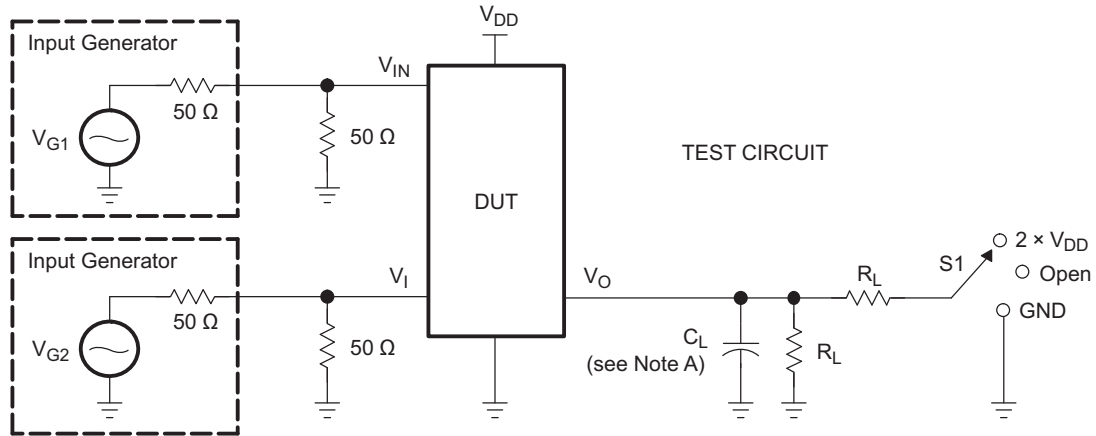


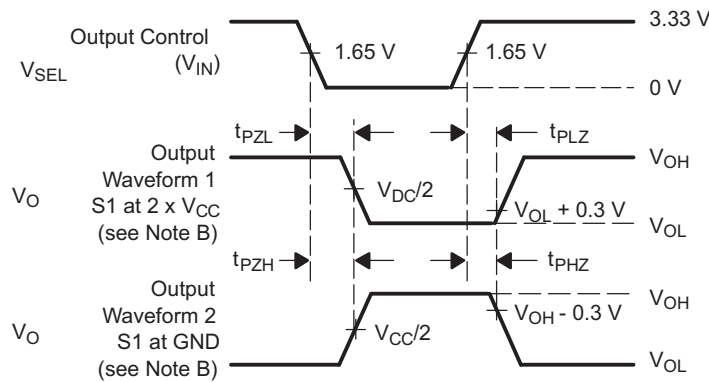
Figure 7. R_{ON} vs V_{IN}

PARAMETER MEASUREMENT INFORMATION

Enable and Disable Times



TEST	V _{DD}	S1	R _L	V _{in}	C _L	V _Δ
t _{PLZ} /t _{PZL}	3.3 V ± 0.3 V	2 × V _{DD}	200 Ω	GND	4 pF	0.3 V
t _{PHZ} /t _{PZH}	3.3 V ± 0.3 V	GND	200 Ω	V _{DD}	4 pF	0.3 V

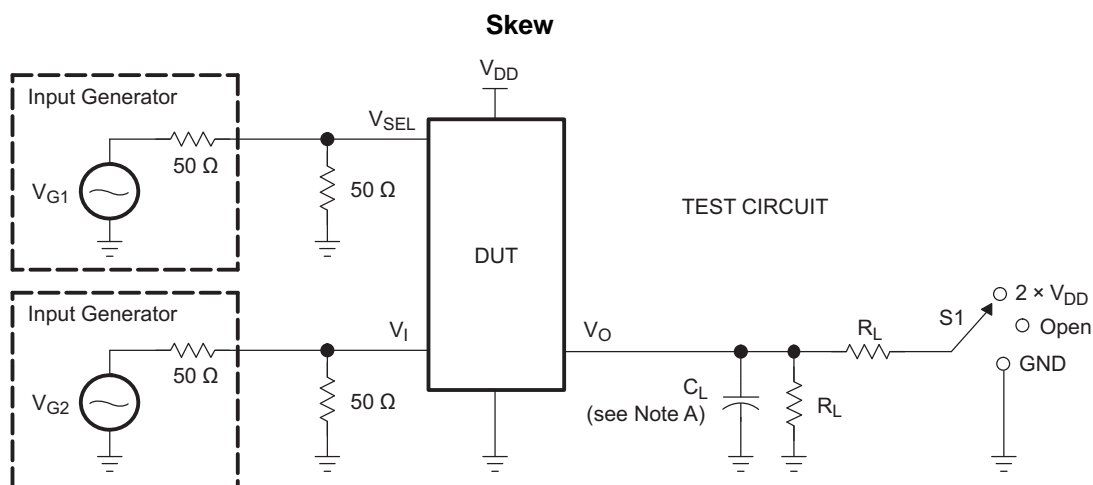


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

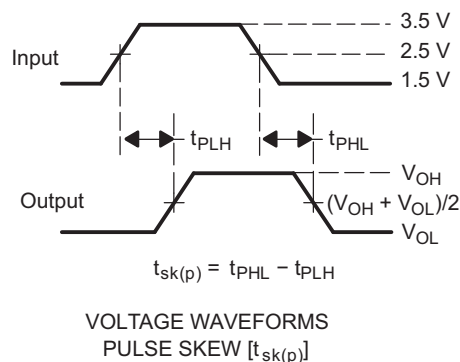
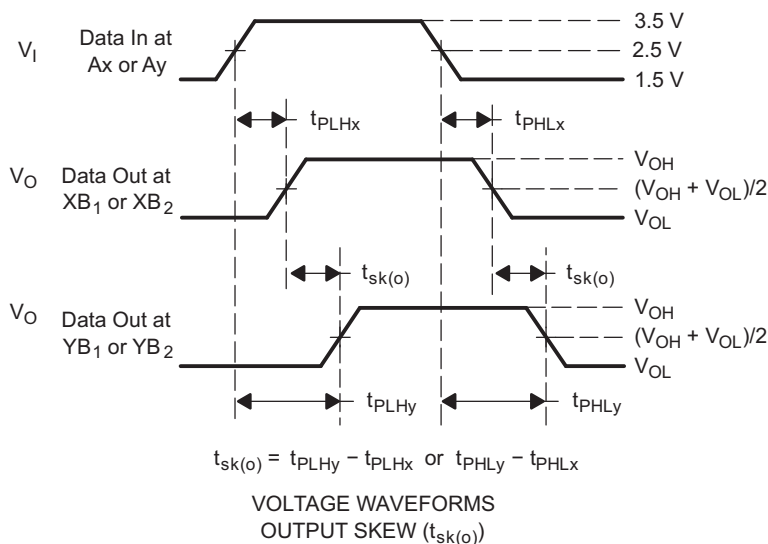
- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
 - F. t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 8. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

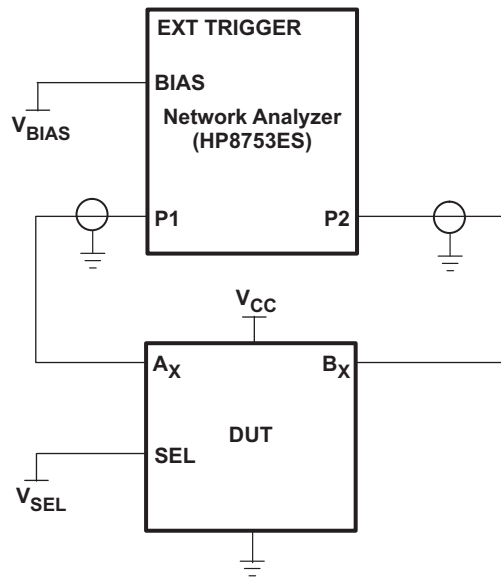


TEST	V _{CC}	S1	R _L	V _{in}	C _L
t _{sk(o)}	3.3 V ± 0.3 V	Open	200 Ω	V _{CC} or GND	4 pF
t _{sk(p)}	3.3 V ± 0.3 V	Open	200 Ω	V _{CC} or GND	4 pF



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 D. The outputs are measured one at a time, with one transition per measurement.

Figure 9. Test Circuit and Voltage Waveforms

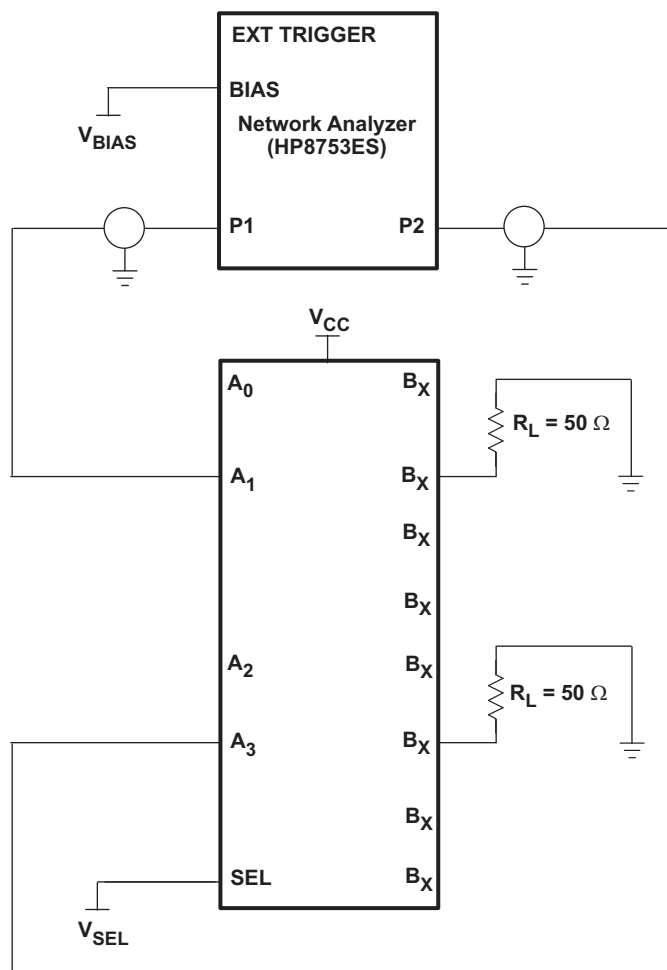
PARAMETER MEASUREMENT INFORMATION (continued)

Figure 10. Test Circuit for Frequency Response (BW)

Frequency response is measured at the output of the ON channel. For example, when $V_{SEL} = 0$ and A_0 is the input, the output is measured at B_0 . All unused analog I/O ports are left open.

HP8753ES Setup

Average = 4
 RBW = 3 kHz
 $V_{BIAS} = 0.35$ V
 ST = 2 s
 P1 = 0 dBm

PARAMETER MEASUREMENT INFORMATION (continued)



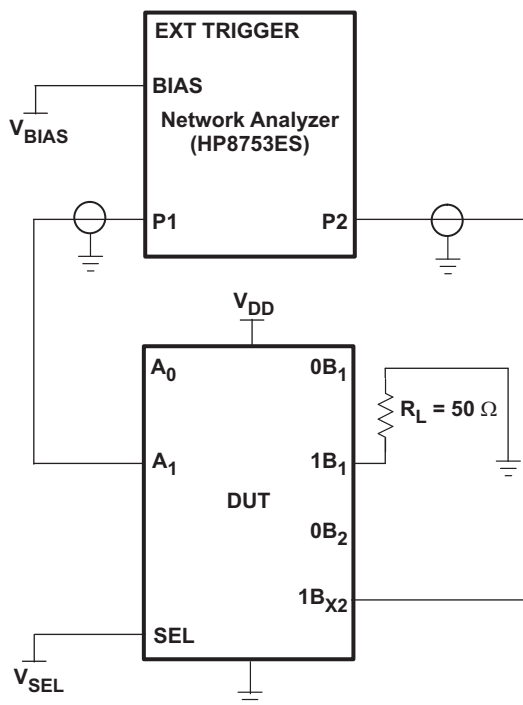
- A. C_L includes probe and jig capacitance.
- B. A 50 W termination resistor is needed to match the loading of the network analyzer.

Figure 11. Test Circuit for Crosstalk (X_{TALK})

Crosstalk is measured at the output of the nonadjacent ON channel. For example, when $V_{SEL} = 0$ and A_1 is the input, the output is measured at A_3 . All unused analog input (A) ports are connected to GND, and output (B) ports are left open.

HP8753ES Setup

- Average = 4
- RBW = 3 kHz
- $V_{BIAS} = 0.35 V$
- ST = 2 s
- P1 = 0 dBm

PARAMETER MEASUREMENT INFORMATION (continued)


A. C_L includes probe and jig capacitance.

B. A 50 W termination resistor is needed to match the loading of the network analyzer.

Figure 12. Test Circuit for OFF Isolation (O_{IRR})

OFF isolation is measured at the output of the OFF channel. For example, when $V_{SEL} = GND$ and A_1 is the input, the output is measured at $1B_2$. All unused analog input (A) ports are connected to ground, and output (B) ports are left open.

HP8753ES Setup

Average = 4

RBW = 3 kHz

$V_{BIAS} = 0.35$ V

ST = 2 s

P1 = 0 dBm

REVISION HISTORY

Changes from Original (January 2012) to Revision A	Page
• Changed C _{ON} value in FEATURES from 5.6 pF to 4 pF.	1
• Deleted LEVEL-SHIFTING REQUIREMENT FOR DUAL-MODE DP/HDMI APPLICATION section from document.	4
• Added C _{ON} TYP value to the ELECTRICAL CHARACTERISTICS table.	6
Changes from Revision A (February 2012) to Revision B	Page
• Changed C _{ON} value from 4 pF to 5.6 pF.	1
• Changed C _{ON} TYP value to the ELECTRICAL CHARACTERISTICS table.	6
Changes from Revision B (May 2012) to Revision C	Page
• Updated APPLICATIONS.	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3DV621RUAR	ACTIVE	WQFN	RUA	42	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SD621	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3DV621RUAR	WQFN	RUA	42	3000	330.0	16.4	3.8	9.3	1.0	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

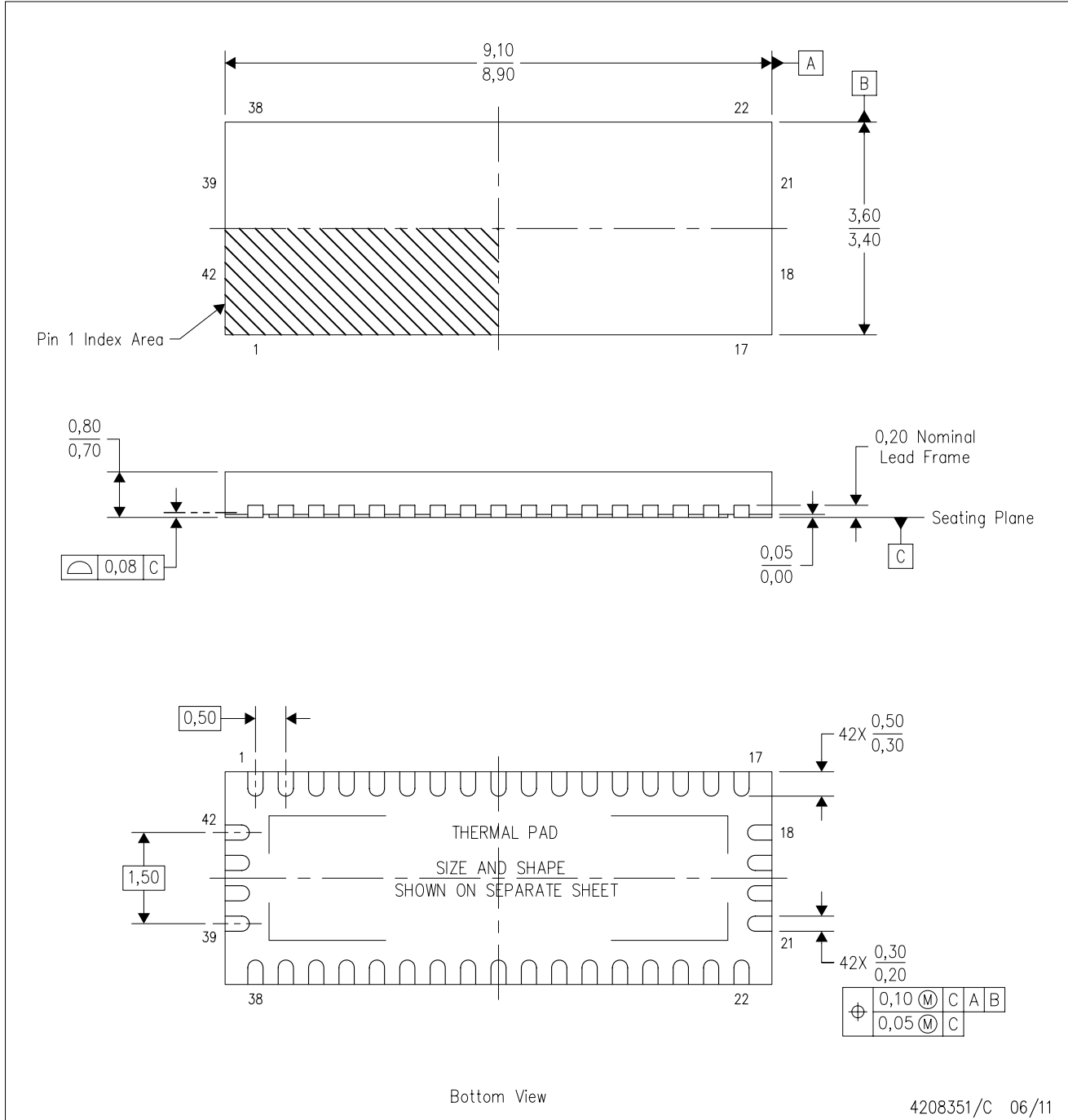


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3DV621RUAR	WQFN	RUA	42	3000	358.0	335.0	35.0

RUA (R-PWQFN-N42)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

THERMAL PAD MECHANICAL DATA

RUA (R-PWQFN-N42)

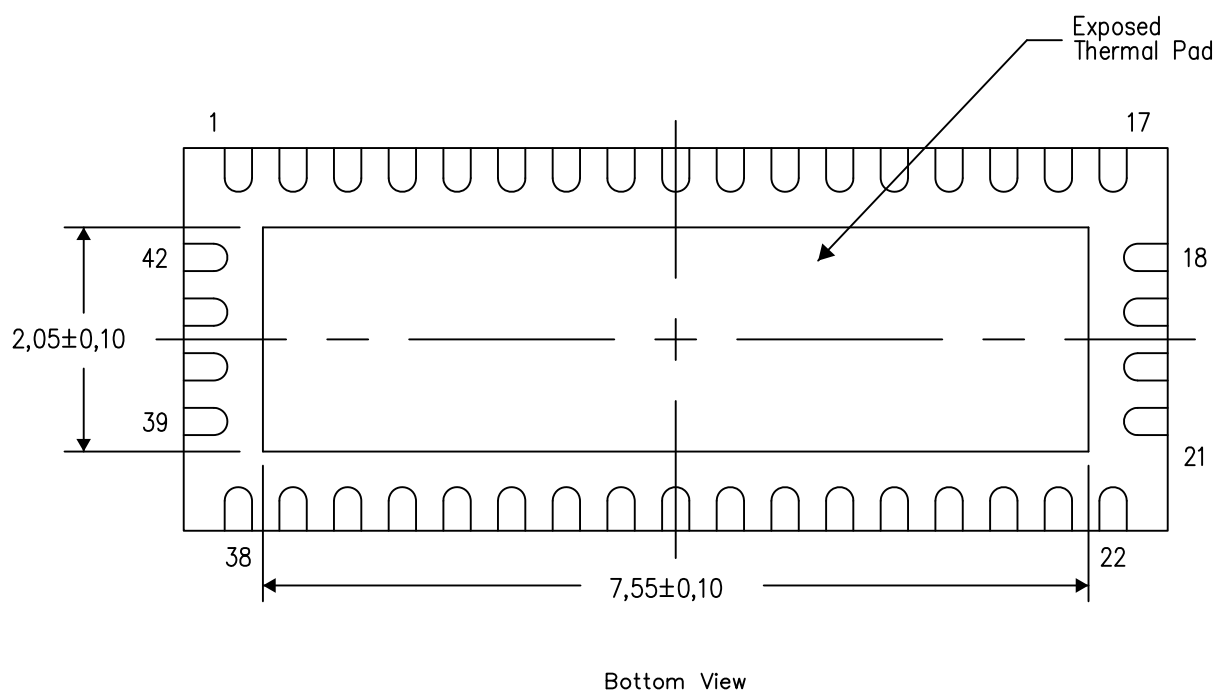
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



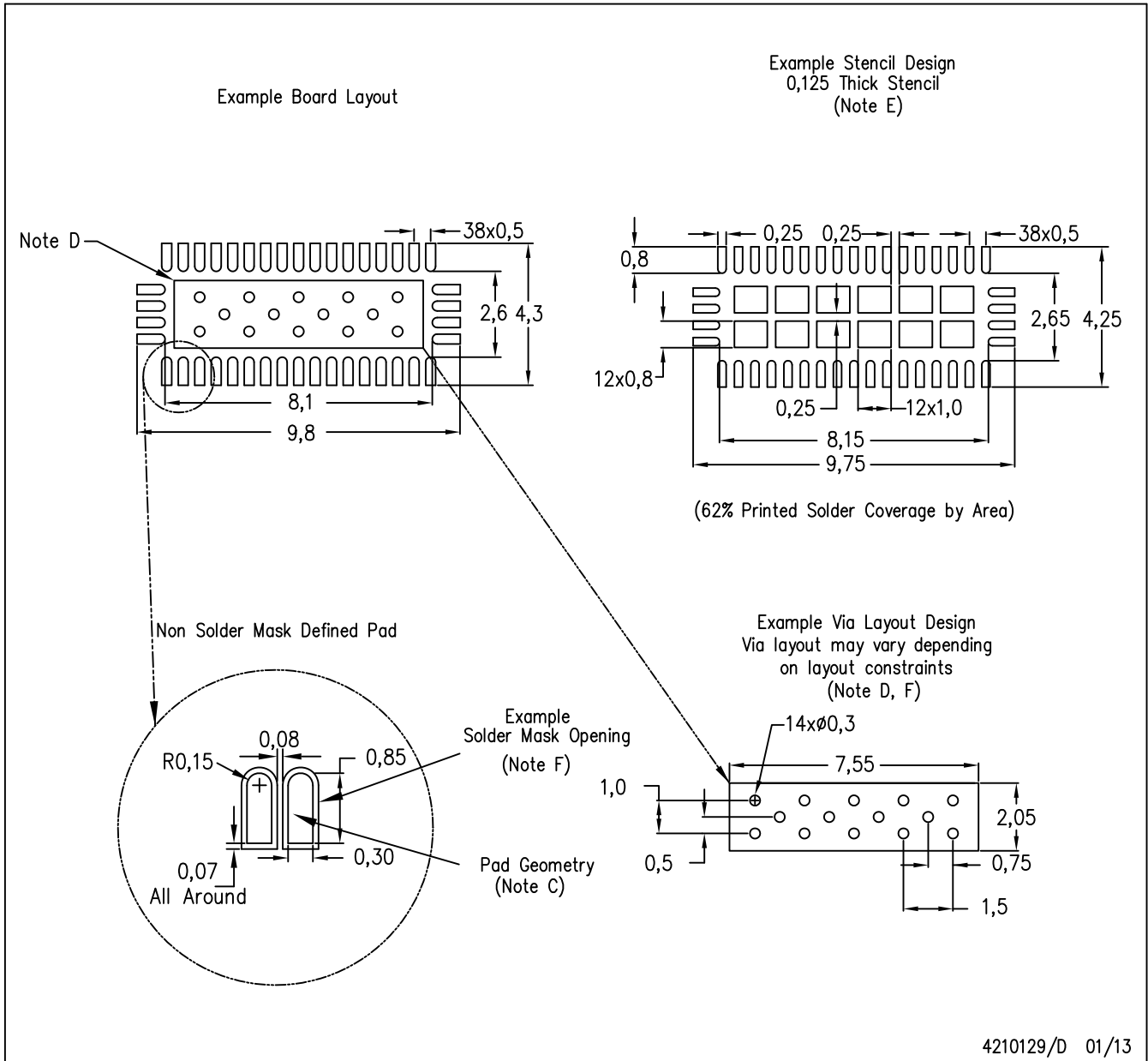
Exposed Thermal Pad Dimensions

4208352/E 01/13

NOTE: All linear dimensions are in millimeters

RUA (R-PWQFN-N42)

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- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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