SCDS256A – OCTOBER 2009 – REVISED SEPTEMBER 2016

TS3USB31E High-Speed USB 2.0 (480-Mbps) 1-Port Switch with Single Enable and ESD Protection

1 Features

- V_{CC} Operation 2.25 V to 4.3 V
- 1.8-V Compatible Control-Pin Inputs
- I_{OFF} Supports Partial Power-Down Mode Operation
- r_{on} = 10 Ω Maximum
- Δr_{on} <0.35 Ω Typical
- $C_{io(ON)}$ = 6 pF Typical
- Low Power Consumption (1 μA Maximum)
- ESD Performance Tested Per JESD 22
  - 8000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
  - 250-V Machine Model (A115-A)
- ESD Performance COM Port to GND
  - 15000-V Human-Body Model (A114-B, Class II)
- Wide –3-dB Bandwidth = 1100 MHz Typical
- Packaged in 8-Pin TQFN (1.5 mm × 1.5 mm)

2 Applications

- Routes Signals for USB 1.0, 1.1, and 2.0

3 Description

The TS3USB31E is a high-bandwidth switch specially designed for the switching of high-speed USB 2.0 signals in handset and consumer applications, such as cell phones, digital cameras, and notebooks with hubs or controllers with limited USB I/Os. The wide bandwidth (1100 MHz) of this switch allows signals to pass with minimum edge and phase distortion. The switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs. It is designed for low bit-to-bit skew and high channel-to-channel noise isolation, and is compatible with various standards, such as high-speed USB 2.0 (480 Mbps).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS3USB31E	UQFN (8)	1.50 mm × 1.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagram

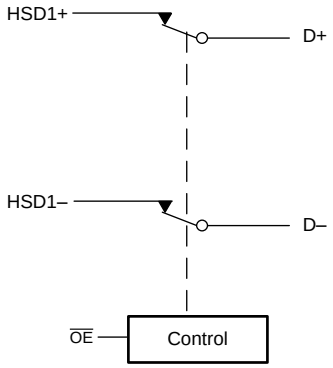


Table of Contents

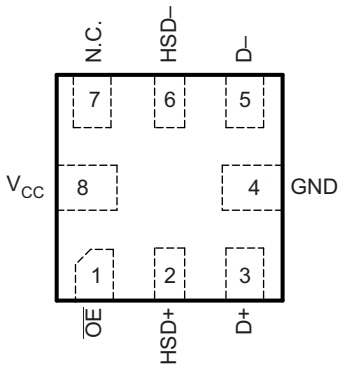
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

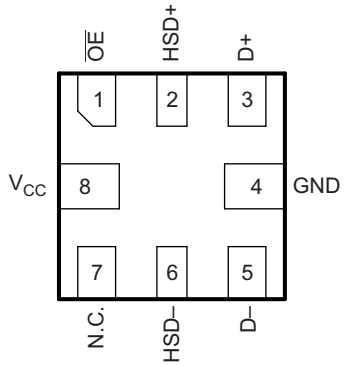
Changes from Original (Oct 2009) to Revision A	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Pin Configuration and Functions

RSE Package
8-Pin UQFN
Top View



RSE Package
8-Pin UQFN
Bottom View



N.C. – No internal connection

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{OE}$	1	I	Bus-switch enable, To isolate the D± pins from the HSD± pins set $\overline{OE}$ pin to valid high logic level, To connect D± pins to HSD± pins set $\overline{OE}$ pin to valid low logic level
D+	3	I/O	Data ports
D–	5	I/O	Data ports
HSD+	2	I/O	Data ports
HSD–	6	I/O	Data ports
N.C.	7	—	No connect, This pin must be left floating or connect to ground
GND	4	—	Ground
V_{CC}	8	I/O	Supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
V_{IN}	Control input voltage(2)(3)		–0.5	7	V
$V_{I/O}$	Switch I/O voltage (2)(3)(4)	HSD+, HSD–	–0.5	V_{CC} + 0.3	V
		D+, D– when V_{CC} > 0	–0.5	V_{CC} + 0.3	
		D+, D– when V_{CC} = 0		5.25	
I_{IK}	Control input clamp current	V_{IN} < 0		–50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O}$ < 0		–50	mA
$I_{I/O}$	ON-state switch current(5)			±64	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±8000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.25	4.3	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	0.9		V
		V_{CC} = 3 V to 3.6 V	1.3		
		V_{CC} = 4.3 V	1.7		
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V		0.4	V
		V_{CC} = 3 V to 3.6 V		0.5	
		V_{CC} = 4.3 V		0.7	
$V_{I/O}$	Data input-output voltage		0	V_{CC}	V
T_A	Operating free-air temperature		–40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*.

6.4 Thermal Information

THERMAL METRIC[1]		TS3USB31 RSE (UQFN) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	127.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	35	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	34.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	MIN	TYP[2]	MAX	UNIT
V_{IK}	Input Clamp Voltage	V_{CC} = 3 V, I_I = –18 mA			–1.2	V
I_{IN}	Control inputs	V_{CC} = 4.3 V or 0 V, V_{IN} = 0 to 4.3 V			±1	µA
I_{OZ}[3]		V_{CC} = 4.3 V, V_O = 0 to 3.6 V, V_I = 0, switch OFF			±1	µA
I_{OFF}	D+ and D–	V_{CC} = 0 V, V_O = 0 V to 4.3 V, V_I = 0, V_{IN} = V_{CC} or GND			±2	µA
I_{CC}		V_{CC} = 4.3 V, $I_{I/O}$ = 0, switch ON or OFF			1	µA
ΔI_{CC}[4]	Control inputs	V_{CC} = 4.3 V, V_{IN} = 2.6 V			10	µA
C_{in}	Control inputs	V_{CC} = 0 V, V_{IN} = V_{CC} or GND		1		pF
$C_{io(OFF)}$	Off-state input-output capacitance	V_{CC} = 2.5 V, $V_{I/O}$ = 2.5 V or 0, switch OFF		2		pF
		V_{CC} = 3.3 V, $V_{I/O}$ = 3.3 V or 0, switch OFF		2		
$C_{io(ON)}$	On-state input-output capacitance	V_{CC} = 2.5 V, $V_{I/O}$ = 2.5 V or 0, switch ON		6		pF
		V_{CC} = 3.3 V, $V_{I/O}$ = 3.3 V or 0, switch ON		6		
r_{on}[5]	On-state resistance	V_{CC} = 2.5 V, V_I = 0.4 V, I_O = –8 mA		7.5	9	Ω
		V_{CC} = 3 V, V_I = 0.4 V, I_O = –8 mA		6.5	10	
Δr_{on}	Channel match	V_{CC} = 2.5 V, V_I = 0.4 V, I_O = –8 mA		0.4		Ω
		V_{CC} = 3 V, V_I = 0.4 V, I_O = –8 mA		0.35		
$r_{on(flat)}$	On-state resistance flatness	V_{CC} = 2.5 V, V_I = 0 V or 1 V, I_O = –8 mA		0.07		Ω
		V_{CC} = 3 V, V_I = 0 V or 1 V, I_O = –8 mA		2		

(1) V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.
(2) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
(5) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

6.6 Dynamic Electrical Characteristics

over operating range, T_A = –40°C to +85°C, GND = 0 V

PARAMETER		TEST CONDITIONS	TYP[1]	UNIT
V_{CC} = 2.5 V ± 10%				
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 240 MHz, See Figure 6	–53	dB
O_{IRR}	OFF isolation	R_L = 50 Ω, f = 240 MHz, See Figure 5	–30	dB
BW	Bandwidth (–3 dB)	R_L = 50 Ω, C_L = 5 pF, See Figure 7	1100	MHz
V_{CC} = 3.3 V ± 10%				
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 240 MHz, See Figure 6	–53	dB

(1) For Max or Min conditions, use the appropriate value specified under *Electrical Characteristics* for the applicable device type.

Dynamic Electrical Characteristics (continued)

over operating range, T_A = –40°C to +85°C, GND = 0 V

PARAMETER		TEST CONDITIONS	TYP(1)	UNIT
O_{IRR}	OFF isolation	R_L = 50 Ω, f = 240 MHz, See Figure 5	–30	dB
BW	Bandwidth (–3 dB)	R_L = 50 Ω, C_L = 5 pF, See Figure 7	1100	MHz

6.7 Switching Characteristics

over operating range, T_A = –40°C to 85°C, GND = 0 V

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{CC} = 2.5 V ± 10%						
t_{pd}	Propagation delay(2)(3)	R_L = 50 Ω, C_L = 5 pF, See Figure 8		0.25		ns
t_{ON}	Line enable time, $\overline{OE}$ to D, nD	R_L = 50 Ω, C_L = 5 pF, See Figure 4			30	ns
t_{OFF}	Line disable time, $\overline{OE}$ to D, nD	R_L = 50 Ω, C_L = 5 pF, See Figure 4			25	ns
$t_{SK(O)}$	Output skew between centre port to any other port(2)	R_L = 50 Ω, C_L = 5 pF, See Figure 9		50		ps
$t_{SK(P)}$	Skew between opposite transitions of the same output (t_{PHL} – t_{PLH})(2)	R_L = 50 Ω, C_L = 5 pF, See Figure 9		20		ps
t_J	Total jitter(2)	R_L = 50 Ω, C_L = 5 pF, t_R = t_F = 500 ps at 480 Mbps (PRBS = 2^{15} – 1)		200		ps
V_{CC} = 3.3 V ± 10%						
t_{pd}	Propagation delay(2)(3)	R_L = 50 Ω, C_L = 5 pF, See Figure 8		0.25		ns
t_{ON}	Line enable time, $\overline{OE}$ to D, nD	R_L = 50 Ω, C_L = 5 pF, See Figure 4			30	ns
t_{OFF}	Line disable time, $\overline{OE}$ to D, nD	R_L = 50 Ω, C_L = 5 pF, See Figure 4			25	ns
$t_{SK(O)}$	Output skew between centre port to any other port(2)	R_L = 50 Ω, C_L = 5 pF, See Figure 9		50		ps
$t_{SK(P)}$	Skew between opposite transitions of the same output (t_{PHL} – t_{PLH})(2)	R_L = 50 Ω, C_L = 5 pF, See Figure 9		20		ps
t_J	Total jitter(2)	R_L = 50 Ω, C_L = 5 pF, t_R = t_F = 500 ps at 480 Mbps (PRBS = 2^{15} – 1)		200		ps

(1) For Max or Min conditions, use the appropriate value specified under *Electrical Characteristics* for the applicable device type.
(2) Specified by design
(3) The bus switch contributes no propagational delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 10-pF load. Since this time constant is much smaller than the rise and fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interactions with the load on the driven side.

7 Application Information

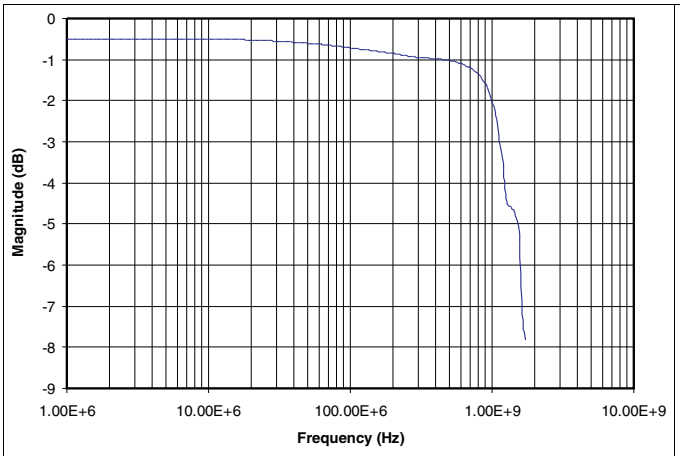


Figure 1. Insertion Loss

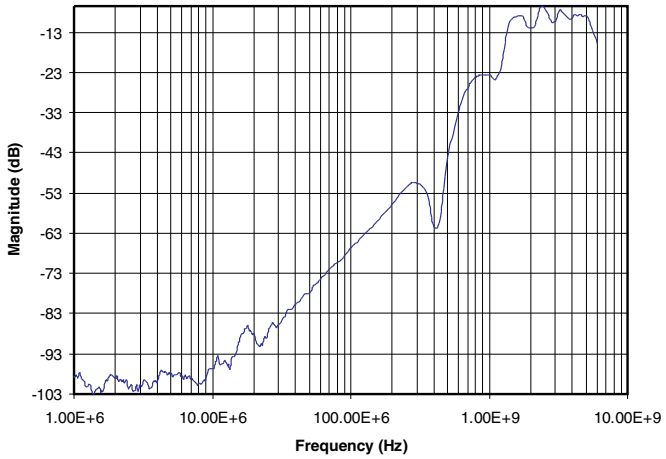


Figure 2. OFF Isolation

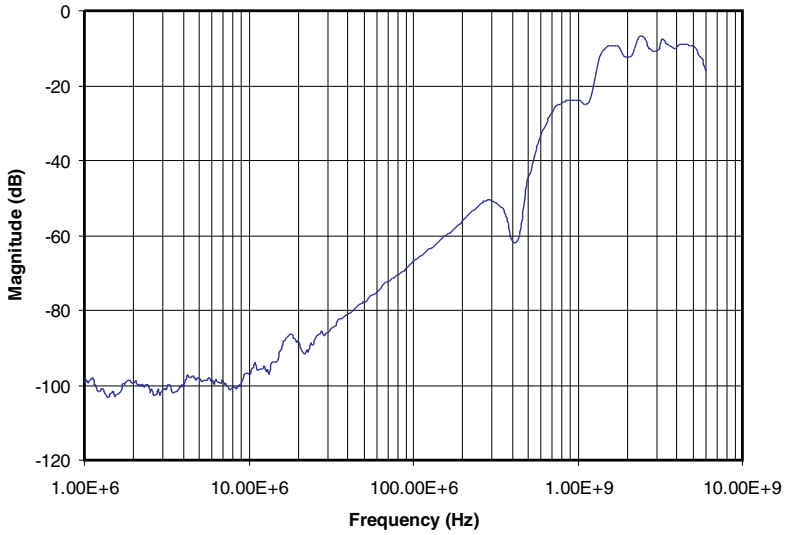
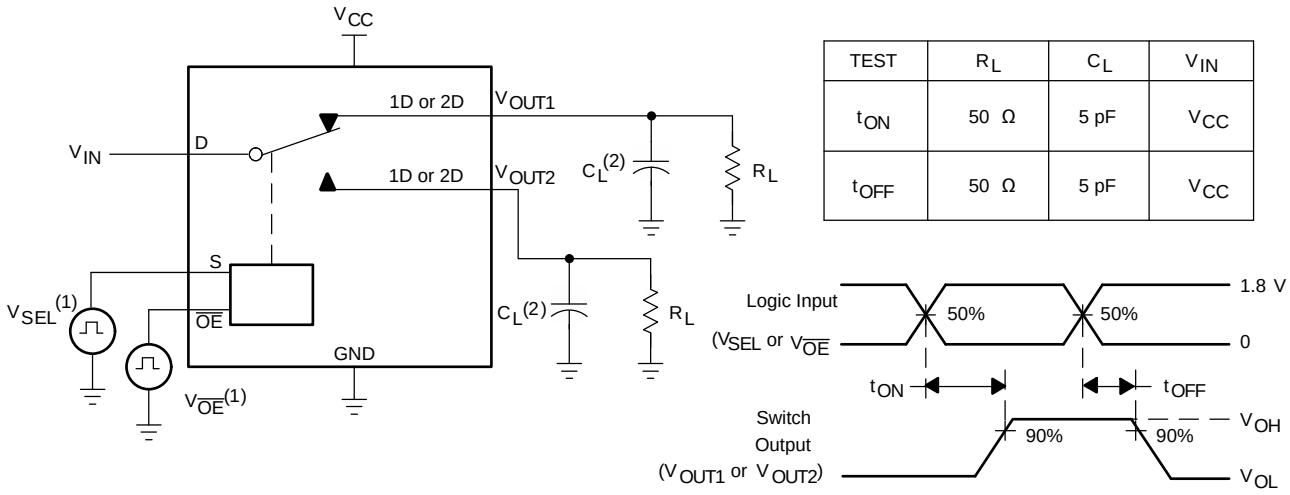


Figure 3. Crosstalk

8 Parameter Measurement Information

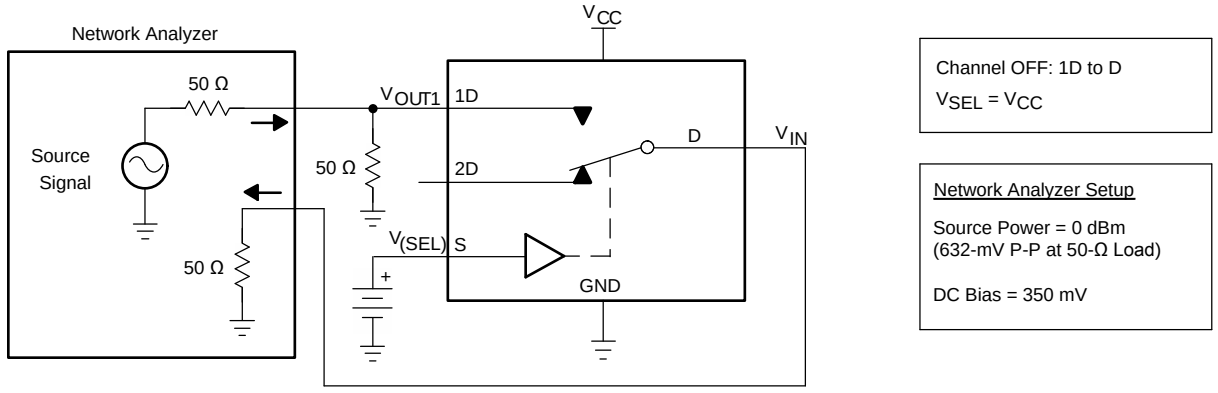


TEST	R_L	C_L	V_{IN}
t_{ON}	50 Ω	5 pF	V_{CC}
t_{OFF}	50 Ω	5 pF	V_{CC}

(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

(2) C_L includes probe and jig capacitance.

Figure 4. Turnon (t_{ON}) and Turnoff Time (t_{OFF})



Channel OFF: 1D to D

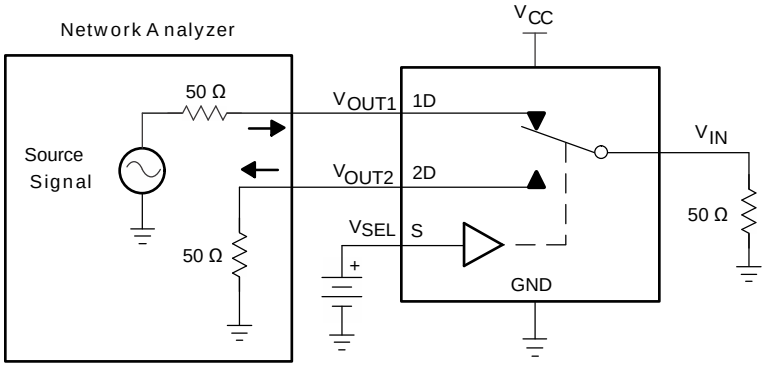
V_{SEL} = V_{CC}

Network Analyzer Setup

Source Power = 0 dBm
(632-mV P-P at 50-Ω Load)

DC Bias = 350 mV

Figure 5. OFF Isolation (O_{IRR})



Channel ON: 1D to D
Channel OFF: 2D to D

V_{SEL}= V_{CC}

Network Analyzer Setup

Source Power= 0 dBm
(632-mV P-P at 50-Ω load)

DC Bias = 350 mV

Figure 6. Crosstalk (X_{TALK})

Parameter Measurement Information (continued)

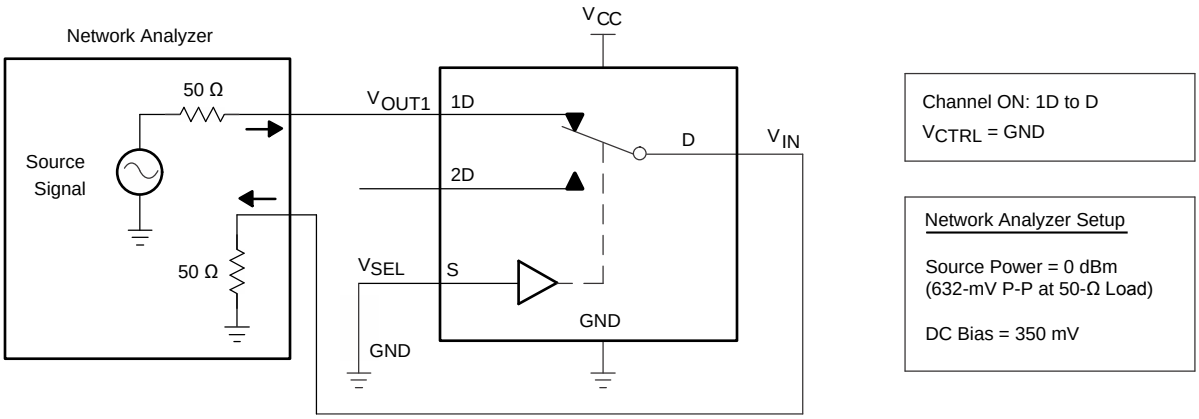


Figure 7. Bandwidth (BW)

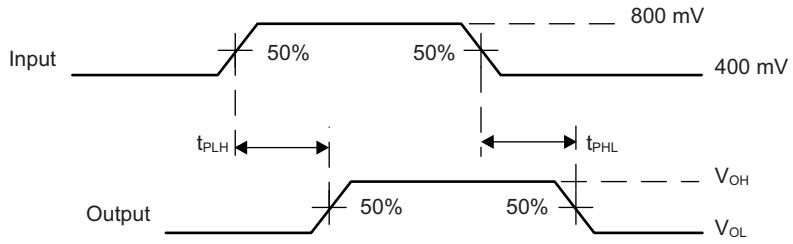


Figure 8. Propagation Delay

Parameter Measurement Information (continued)

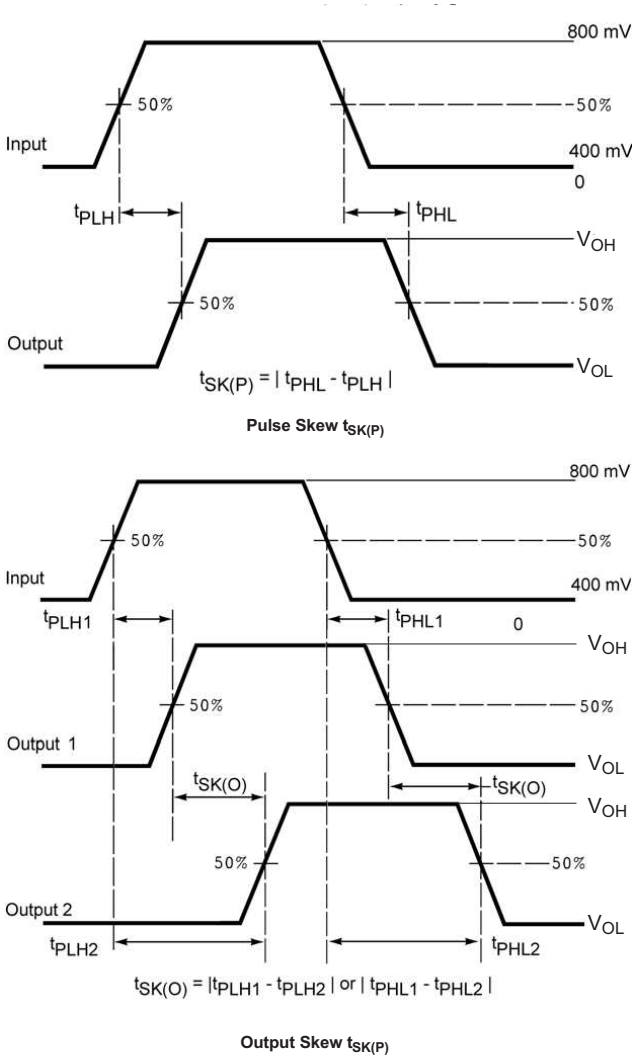


Figure 9. Skew Test

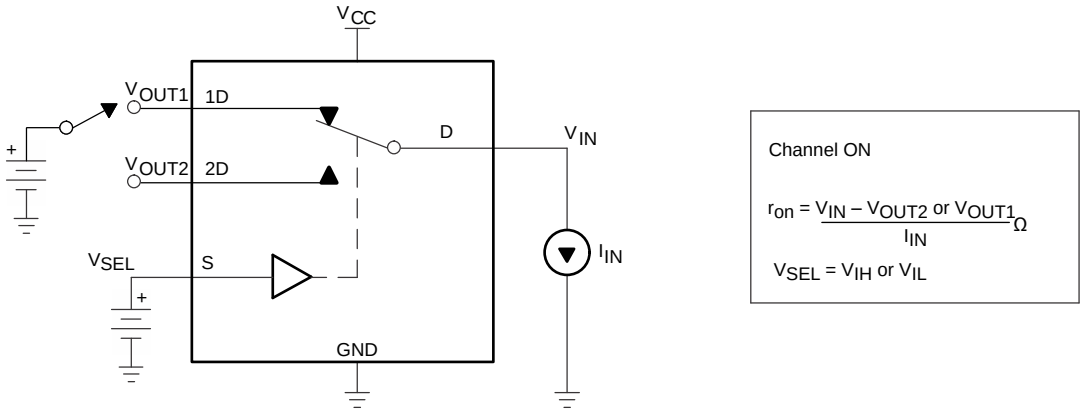


Figure 10. ON-State Resistance (r_{on})

Parameter Measurement Information (continued)

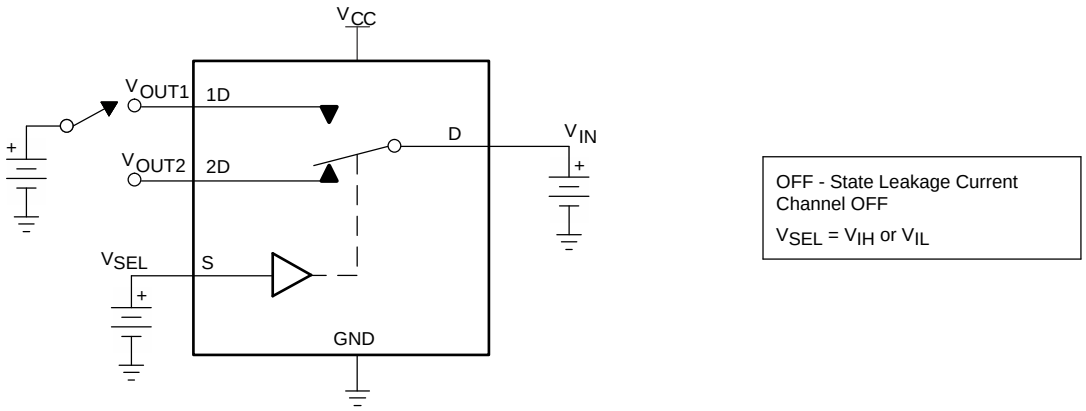


Figure 11. OFF-State Leakage Current

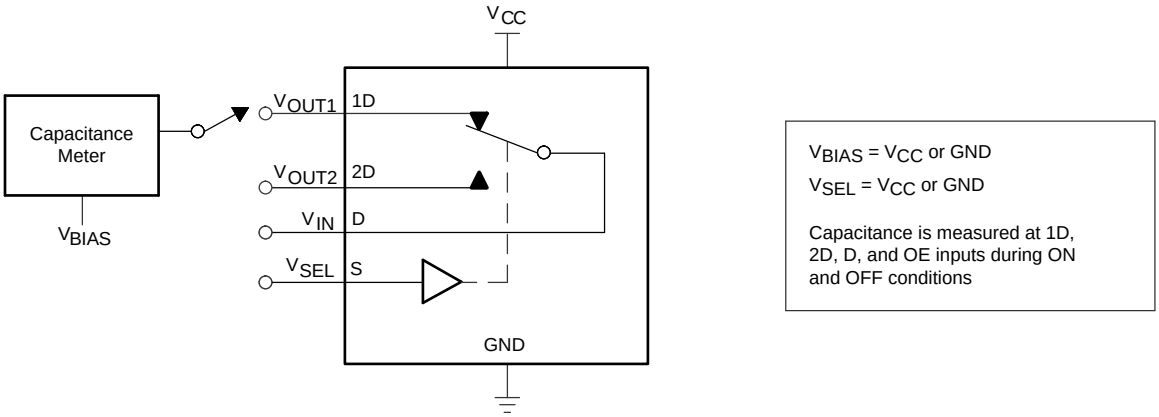


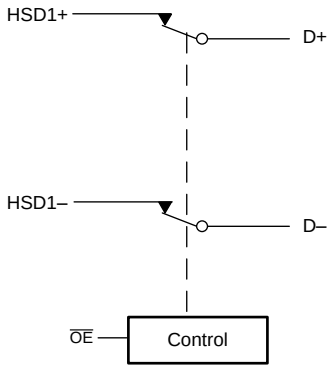
Figure 12. Capacitance

9 Detailed Description

9.1 Overview

The TS3USB31E is a 1:1 SPST high-bandwidth switch specially designed for the switching of high-speed USB 2.0 signals. The switch is bidirectional and offers little or no attenuation of the high-speed signals. It is designed for low bit-to-bit skew and high channel-to-channel noise isolation, and is compatible with various standards, such as high-speed USB 2.0 (480 Mbps).

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 I_{OFF} Supports Partial Power-Down Mode Operation

When V_{CC} = 0 V, the signal path is placed in a high impedance state which isolates the bus. This allows signals to be present on the D± and HSD± pins before the device is powered up without damaging the device.

9.4 Device Functional Modes

The TS3USB31E device has two modes that are digitally controlled by the OE pin. Setting the OE pin *High* isolates the signal path by a high impedance state. See Table 1.

Table 1. Truth Table

$\overline{OE}$	FUNCTION
H	Disconnect
L	D+, D– = HSD+, HSD–

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TS3USB31E device is used to isolate a USB bus when it is not in use to prevent two different USB devices from interfering with each other.

10.2 Typical Application

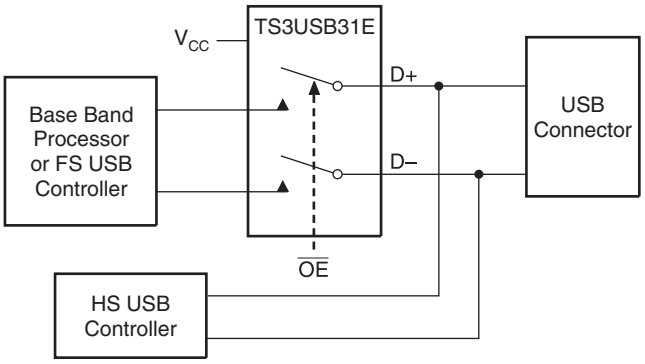


Figure 13. Application Diagram

10.2.1 Design Requirements

Design requirements of the USB 1.0, 1.1, and 2.0 standards must be followed. TI recommends that the digital control pin $\overline{OE}$ be pulled up to V_{CC} or down to ground to avoid undesired switch positions that could result from the floating pin.

10.2.2 Detailed Design Procedure

The TS3USB31E can be properly operated without any external components. However, it is recommended that unused pins be connected to ground through a 50-Ω resistor to prevent signal reflections back into the device.

The N.C pin must be left floating.

Typical Application (continued)

10.2.3 Application Curves

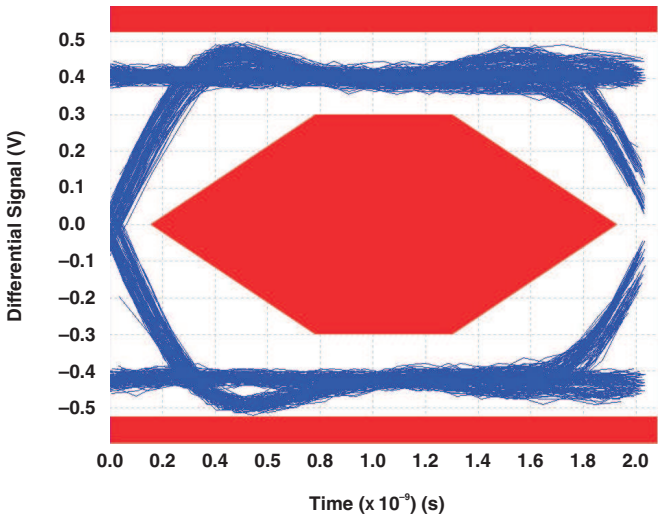


Figure 14. Eye Pattern: 480-Mbps USB Signal with No Switch (Through Path)

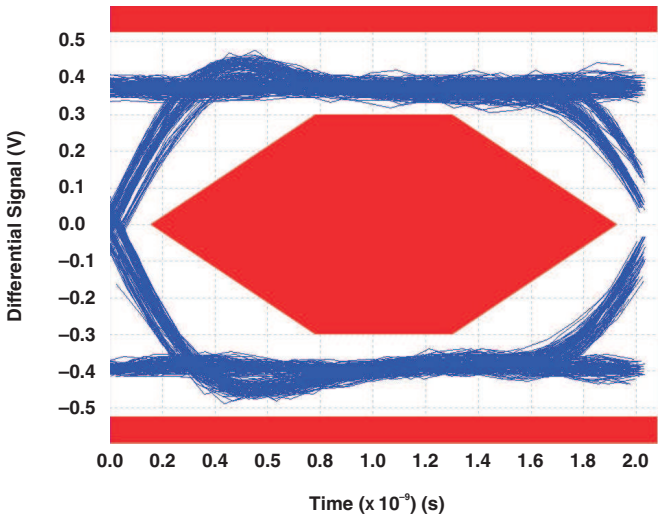


Figure 15. Eye Pattern: 480-Mbps USB Signal with Switch NO Path

11 Power Supply Recommendations

Power to the device is supplied through the V_{CC} pin. TI recommends placing a bypass capacitor as close as possible to the supply pin V_{CC} to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

This device doesn't require any power sequencing with respect to other devices in the system due to its power off isolation feature which allows signals to be present on the D± and HSD± pins before the device is powered up without damaging the device.

12 Layout

12.1 Layout Guidelines

Place supply bypass capacitors as close to V_{CC} pin as possible and avoid placing the bypass caps near the D+ and D– traces.

The high-speed D+ and D– traces must always be of equal length and must be no more than 4 inches; otherwise, the eye diagram performance may be degraded. A high-speed USB connection is made through a shielded, twisted pair cable with a differential characteristic impedance. In layout, the impedance of D+ and D– traces must match the cable characteristic differential impedance for optimal performance.

Route the high-speed USB signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the transmission line of the signal and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.

When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.

Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices, or IC's that use or duplicate clock signals.

Avoid stubs on the high-speed USB signals because they cause signal reflections. If a stub is unavoidable, then the stub must be less than 200 mm.

Route all high-speed USB signal traces over continuous planes (VCC or GND), with no interruptions.

Avoid crossing over anti-etch, commonly found with plane splits.

Due to high frequencies associated with the USB, a printed circuit board with at least four layers is recommended: two signal layers separated by a ground layer and a power layer. The majority of signal traces must run on a single layer, preferably top layer. Immediately next to this layer must be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies. For more information on layout guidelines, see *High Speed Layout Guidelines* (SCAA082) and *USB 2.0 Board Design and Layout Guidelines* (SPRAAR7).

12.2 Layout Example

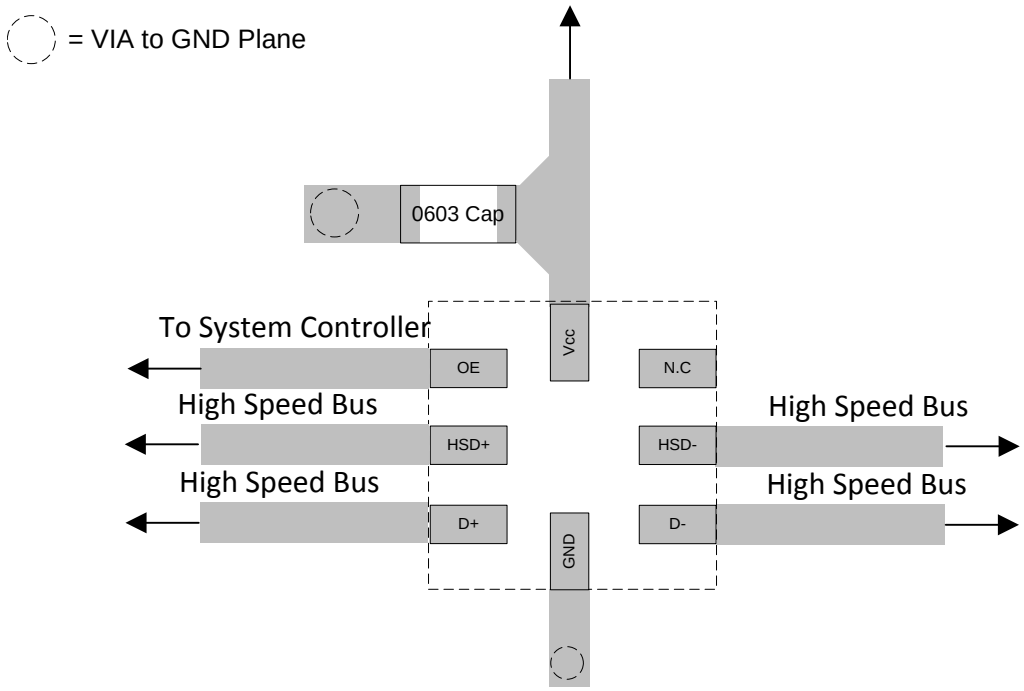


Figure 16. Layout Recommendation

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following

- *High Speed Layout Guidelines*
- *USB 2.0 Board Design and Layout Guidelines*

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3USB31ERSER	ACTIVE	UQFN	RSE	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	LJ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

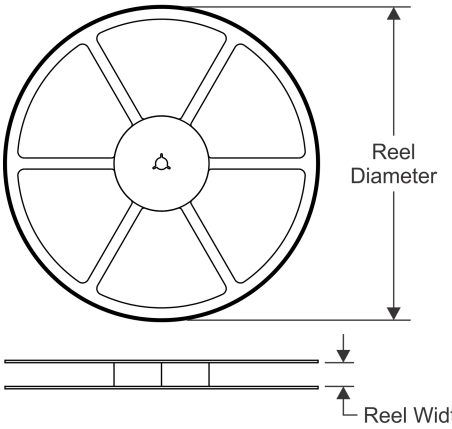
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

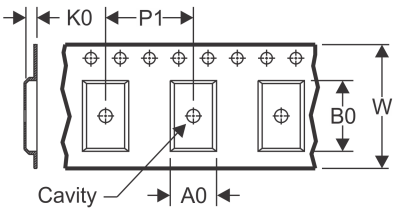
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

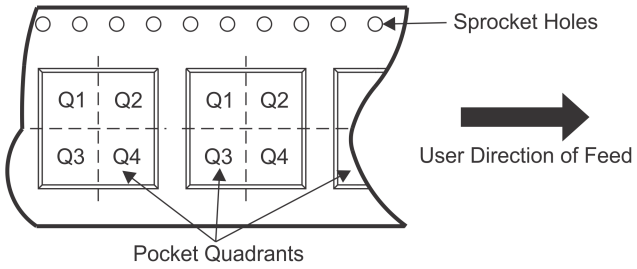


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

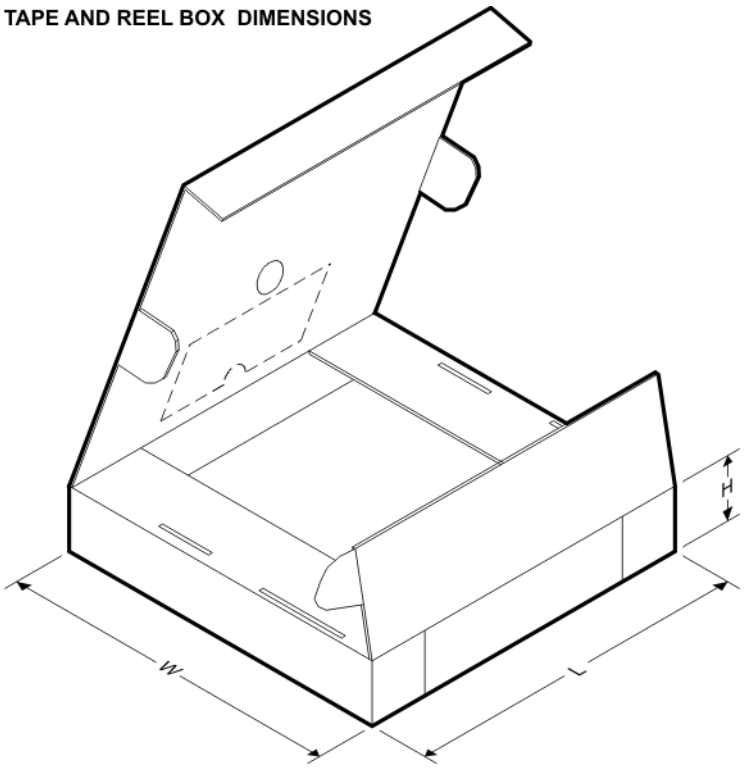
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3USB31ERSER	UQFN	RSE	8	3000	180.0	8.4	1.7	1.7	0.7	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

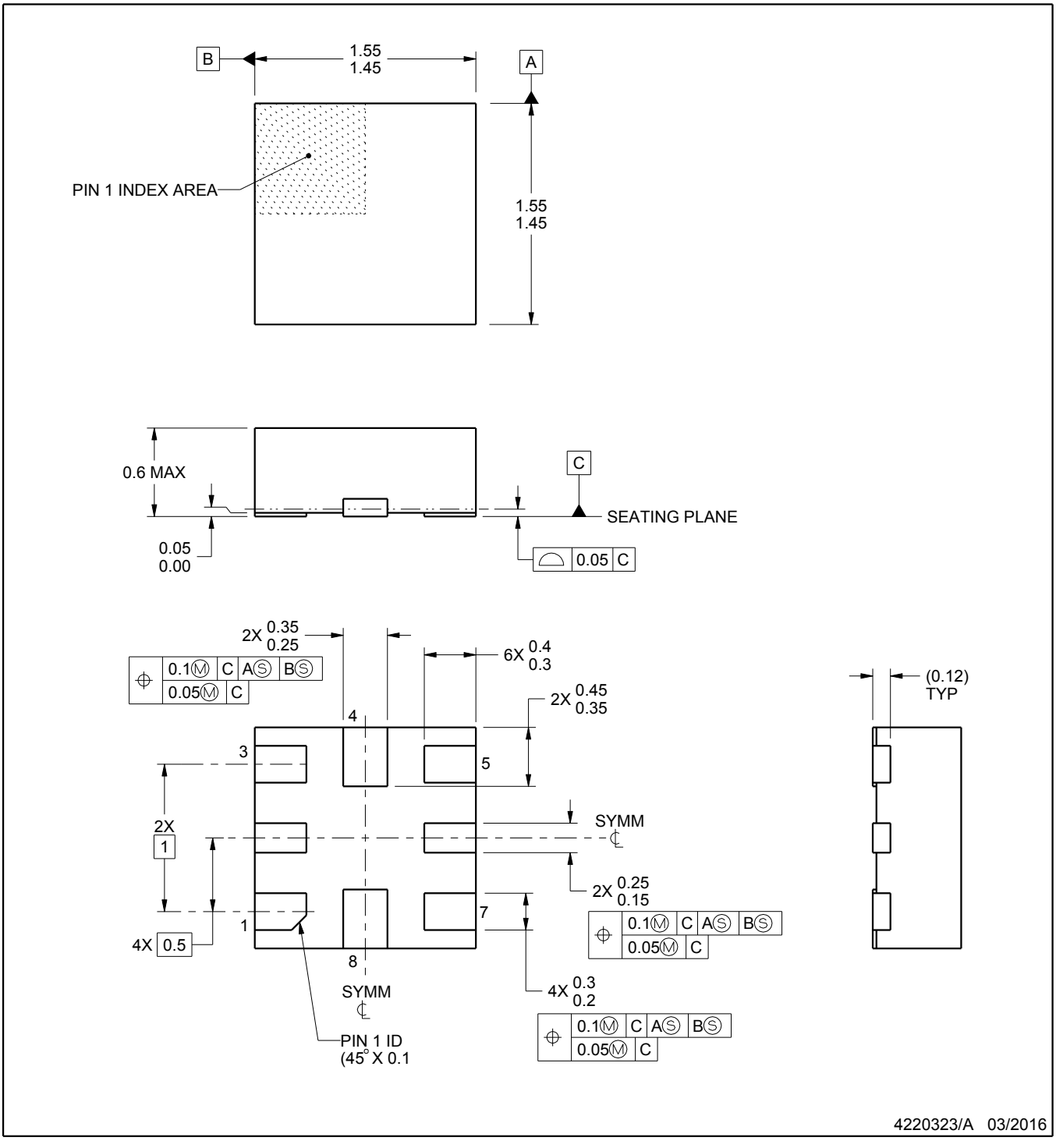
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3USB31ERSER	UQFN	RSE	8	3000	202.0	201.0	28.0

PACKAGE OUTLINE

RSE0008A

UQFN - 0.6 mm max height

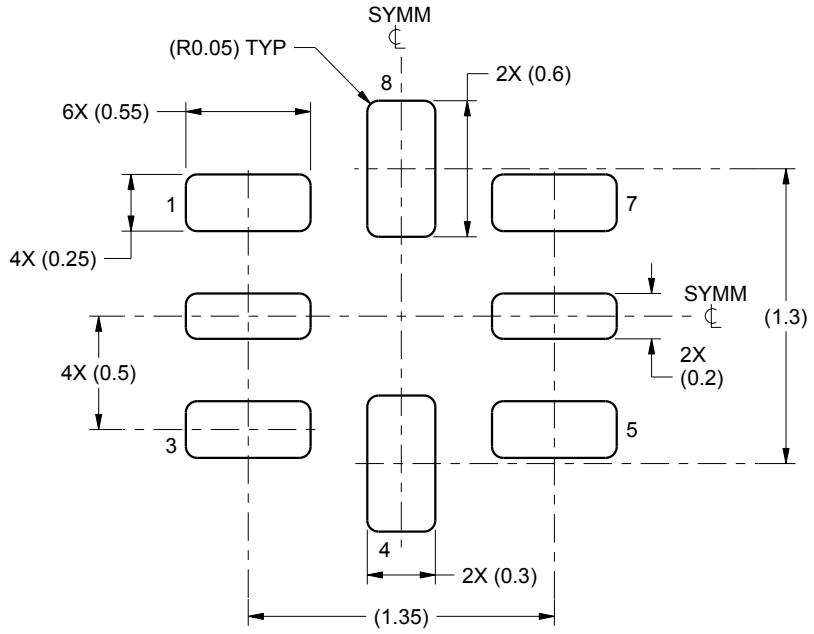
PLASTIC QUAD FLATPACK - NO LEAD



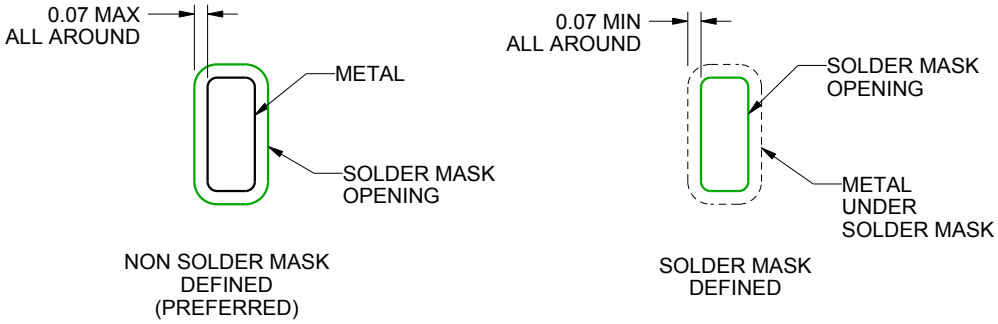
4220323/A 03/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X

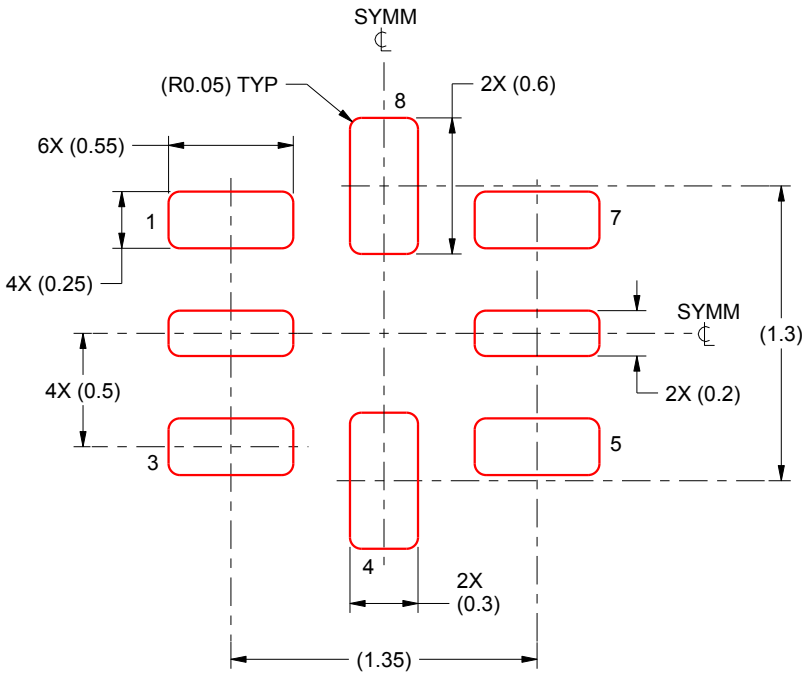


SOLDER MASK DETAILS
NOT TO SCALE

4220323/A 03/2016

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICKNESS
SCALE: 30X

4220323/A 03/2016

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265