

## TS5A22362 0.65-Ω 2-channel SPDT Analog Switches With Negative Signaling Capability

### 1 Features

- Specified Break-Before-Make Switching
- Negative Signaling Capability: Maximum Swing from  $-2.75\text{ V}$  to  $2.75\text{ V}$  ( $V_{CC} = 2.75\text{ V}$ )
- Low ON-State Resistance ( $0.65\ \Omega$  Typical)
- Low Charge Injection
- Excellent ON-State Resistance Matching
- 2.3-V to 5.5-V Power Supply ( $V_{CC}$ )
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2500-V Human-Body Model (A114-B, Class II)
  - 1500-V Charged-Device Model (C101)
  - 200-V Machine Model (A115-A)

### 2 Applications

- Cell Phones
- PDAs
- Portable Instrumentation
- Audio Routing
- Medical Imaging

### 3 Description

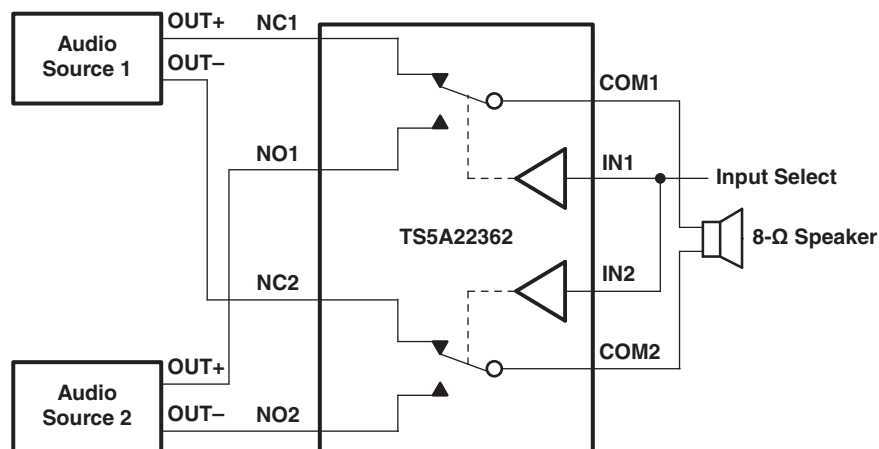
The TS5A22362 is a bidirectional, 2-channel single-pole double-throw (SPDT) analog switch designed to operate from 2.3 V to 5.5 V. The device features negative signal swing capability that allows signals below ground to pass through the switch without distortion. The break-before-make feature prevents signal distortion during the transferring of a signal from one path to another. Low ON-state resistance, excellent channel-to-channel ON-state resistance matching, and minimal total harmonic distortion (THD) performance are ideal for audio applications. The 3.00 mm × 3.00 mm DRC package is also available as a nonmagnetic package for medical imaging application.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS5A22362	VSON (10)	3.00 mm × 3.00 mm
	DSBGA (10)	1.86 mm × 1.36 mm
	VSSOP (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Typical Application Schematic



## Table of Contents

<b>1 Features</b> .....	1	8.2 Functional Block Diagram .....	15
<b>2 Applications</b> .....	1	8.3 Feature Description .....	15
<b>3 Description</b> .....	1	8.4 Device Functional Modes .....	15
<b>4 Revision History</b> .....	2	<b>9 Application and Implementation</b> .....	16
<b>5 Pin Configuration and Functions</b> .....	3	9.1 Application Information .....	16
<b>6 Specifications</b> .....	4	9.2 Typical Application .....	16
6.1 Absolute Maximum Ratings .....	4	<b>10 Power Supply Recommendations</b> .....	18
6.2 ESD Ratings .....	4	<b>11 Layout</b> .....	18
6.3 Recommended Operating Conditions .....	4	11.1 Layout Guidelines .....	18
6.4 Thermal Information .....	5	11.2 Layout Example .....	18
6.5 Electrical Characteristics for 2.5-V Supply .....	5	<b>12 Device and Documentation Support</b> .....	19
6.6 Electrical Characteristics for 3.3-V Supply .....	6	12.1 Receiving Notification of Documentation Updates .....	19
6.7 Electrical Characteristics for 5-V Supply .....	7	12.2 Community Resources .....	19
6.8 Typical Characteristics .....	9	12.3 Trademarks .....	19
<b>7 Parameter Measurement Information</b> .....	11	12.4 Electrostatic Discharge Caution .....	19
<b>8 Detailed Description</b> .....	15	12.5 Glossary .....	19
8.1 Overview .....	15	<b>13 Mechanical, Packaging, and Orderable Information</b> .....	19

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (September 2015) to Revision C	Page
• Changed the $V_{IN}$ MAX value From: $V_{CC}$ To: 5.5 V in the <i>Recommended Operating Conditions</i> table .....	4

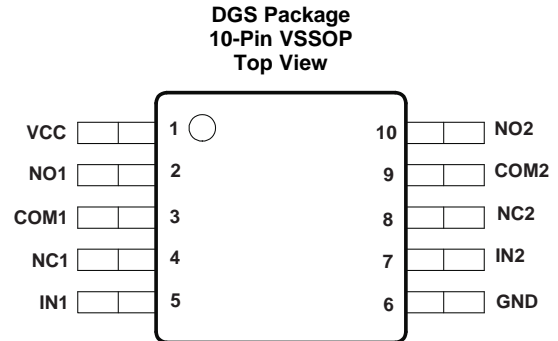
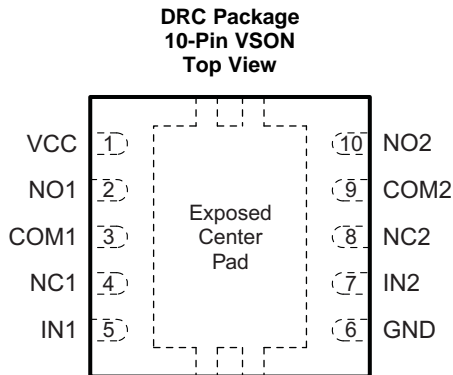
  

Changes from Revision A (August 2015) to Revision B	Page
• Changed $C_L$ TEST CONDITION value for all THD PARAMETERS from 15 pf to 35 pf. ....	6

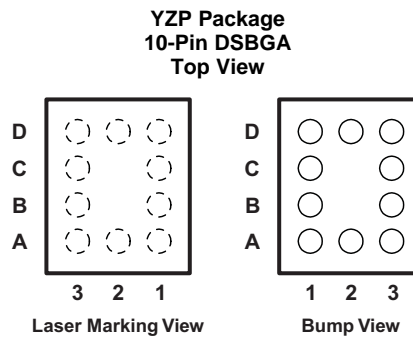
  

Changes from Original (June 2015) to Revision A	Page
• Changed the Functional Block Diagram. ....	15

## 5 Pin Configuration and Functions



\*The exposed center pad, if used, must be connected as a secondary GND or left electrically open.



### Pin Functions

NAME	PIN			TYPE	DESCRIPTION
	VSON	VSSOP	DSBGA		
VCC	1	1	A2	—	Power Supply
NO1	2	2	A3	I/O	Normally Open (NO) signal path, Switch 1
COM1	3	3	B3	I/O	Common signal path, Switch 1
NC1	4	4	C3	I/O	Normally Closed (NC) signal path, Switch 1
IN1	5	5	D3	I	Digital control pin , Switch 1
GND	6	6	D2	—	Ground
IN2	7	7	D1	I	Digital control pin, Switch 2
NC2	8	8	C1	I/O	Normally Closed (NC) signal path, Switch 2
COM2	9	9	B1	I/O	Common signal path, Switch 2
NO2	10	10	A1	I/O	Normally Open (NO) signal Path, Switch 2

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CC}$ <sup>(2)</sup>	Supply voltage <sup>(3)</sup>	-0.5	6	V
$V_{NC}$ $V_{NO}$ $V_{COM}$	Analog voltage <sup>(3)</sup> <sup>(4)</sup> <sup>(5)</sup>	$V_{CC} - 6$	$V_{CC} + 0.5$	V
$I_{I/OK}$	Analog port diode current $V_{NC}, V_{NO}, V_{COM} < 0$ or $V_{NC}, V_{NO}, V_{COM} > V_{CC}$	-50	50	mA
$I_{INC}$ $I_{INO}$ $I_{ICOM}$	ON-state switch current ON-state peak switch current <sup>(6)</sup>	-150 -300	150 300	mA
$I_{INC}$ <sup>(3)</sup> <sup>(7)</sup> <sup>(8)</sup> $I_{INO}$ <sup>(3)</sup> <sup>(7)</sup> <sup>(8)</sup> $I_{ICOM}$ <sup>(3)</sup> <sup>(7)</sup> <sup>(8)</sup>	ON-state switch current ON-state peak switch current <sup>(6)</sup>	-350 -500	350 500	mA
$V_I$	Digital input voltage	-0.5	6.5	V
$I_{IK}$	Digital input clamp current <sup>(3)</sup> <sup>(4)</sup> $V_I < 0$	-50	50	mA
$I_{CC}$ $I_{GND}$	Continuous current through $V_{CC}$ or GND	-100	100	mA
$T_{stg}$	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
- (3) All voltages are with respect to ground, unless otherwise specified.
- (4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (5) This value is limited to 5.5 V maximum.
- (6) Pulse at 1-ms duration < 10% duty cycle.
- (7)  $V_{CC} = 3.0$  V to 5.0 V,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ .
- (8) For YZP package only.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2500	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2.3	5.5	V
$V_{NC}$ $V_{NO}$ $V_{COM}$	Signal path voltage	$V_{CC} - 5.5$	$V_{CC}$	V
$V_{IN}$	Digital control	GND	5.5	V

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TS5A22362			UNIT
		DGS (VSSOP)	DRC (VSON)	YZP (DSBGA)	
		10 PINS	10 PINS	10 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	163.3	44.3	90.9	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	56.4	70.1	0.3	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	83.1	19.3	8.3	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	6.8	2.0	3.2	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	81.8	19.4	8.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics for 2.5-V Supply

V<sub>CC</sub> = 2.3 V to 2.7 V, T<sub>A</sub> = –40°C to 85°C (unless otherwise noted) <sup>(1)</sup>

PARAMETER		TEST CONDITIONS		T <sub>A</sub>	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
<b>Analog Switch</b>									
V <sub>COM</sub> , V <sub>NO</sub> , V <sub>NC</sub>	Analog signal range					V <sub>CC</sub> – 5.5		V <sub>CC</sub>	V
R <sub>on</sub>	ON-state resistance	V <sub>NC</sub> or V <sub>NO</sub> = V <sub>CC</sub> , 1.5 V, V <sub>CC</sub> – 5.5 V I <sub>COM</sub> = –100 mA,	COM to NO or NC, see <a href="#">Figure 13</a>	25°C Full	2.7 V		0.65 0.94	1.3	Ω
ΔR <sub>on</sub>	ON-state resistance match between channels	V <sub>NC</sub> or V <sub>NO</sub> = 1.5 V, I <sub>COM</sub> = –100 mA,	COM to NO or NC, see <a href="#">Figure 13</a>	25°C Full	2.7 V		0.023 0.11	0.15	Ω
R <sub>on(flat)</sub>	ON-state resistance flatness	V <sub>NC</sub> or V <sub>NO</sub> = V <sub>CC</sub> , 1.5 V, V <sub>CC</sub> – 5.5 V I <sub>COM</sub> = –100 mA,	COM to NO or NC, see <a href="#">Figure 13</a>	25°C Full	2.7 V		0.18 0.46	0.5	Ω
I <sub>NC(OFF)</sub> , I <sub>NO(OFF)</sub>	NC, NO OFF leakage current	V <sub>NC</sub> = 2.25 V, V <sub>CC</sub> – 5.5 V V <sub>COM</sub> = V <sub>CC</sub> – 5.5 V, 2.25 V V <sub>NO</sub> = Open COM to NO or V <sub>NO</sub> = 2.25 V, V <sub>CC</sub> – 5.5 V, V <sub>COM</sub> = V <sub>CC</sub> – 5.5 V, 2.25 V V <sub>NC</sub> = Open COM to NC	See <a href="#">Figure 14</a>	25°C Full	2.7 V	–50 –375		50 375	nA
I <sub>COM(ON)</sub>	COM ON leakage current	V <sub>NC</sub> and V <sub>NO</sub> = Floating, V <sub>COM</sub> = V <sub>CC</sub> , V <sub>CC</sub> – 5.5 V	See <a href="#">Figure 15</a>	25°C Full	2.7 V	–50 –375		50 375	nA
<b>Digital Control Inputs (IN) <sup>(2)</sup></b>									
V <sub>IH</sub>	Input logic high			Full		1.4		5.5	V
V <sub>IL</sub>	Input logic low			Full				0.6	V
I <sub>IH</sub> , I <sub>IL</sub>	Input leakage current	V <sub>IN</sub> = V <sub>CC</sub> or 0		25°C Full	2.7 V	–250 –250		250 250	nA
<b>Dynamic</b>									
t <sub>ON</sub>	Turnon time	V <sub>COM</sub> = V <sub>CC</sub> , R <sub>L</sub> = 300 Ω,	C <sub>L</sub> = 35 pF, see <a href="#">Figure 17</a>	25°C Full	2.5 V 2.3 V to 2.7 V		44 120	80	ns
t <sub>OFF</sub>	Turnoff time	V <sub>COM</sub> = V <sub>CC</sub> , R <sub>L</sub> = 300 Ω,	C <sub>L</sub> = 35 pF, see <a href="#">Figure 17</a>	25°C Full	2.5 V 2.3 V to 2.7 V		22 70	70	ns
t <sub>BMM</sub>	Break-before-make time	See <a href="#">Figure 18</a>		25°C	2.5 V	1	7		ns
Q <sub>C</sub>	Charge injection	V <sub>GEN</sub> = 0, R <sub>GEN</sub> = 0,	C <sub>L</sub> = 1 nF, see <a href="#">Figure 22</a>	25°C	2.5 V		150		pC
C <sub>NC(OFF)</sub> , C <sub>NO(OFF)</sub>	NC, NO OFF capacitance	V <sub>NC</sub> or V <sub>NO</sub> = V <sub>CC</sub> or GND,	See <a href="#">Figure 16</a>	25°C	2.5 V		70		pF
C <sub>COM(ON)</sub>	NC, NO, COM ON capacitance	V <sub>COM</sub> = V <sub>CC</sub> or GND, Switch ON, f = 10 MHz	See <a href="#">Figure 16</a>	25°C	2.5 V		370		pF

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

**Electrical Characteristics for 2.5-V Supply (continued)**
 $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ ,  $T_A = -40^\circ\text{C to } 85^\circ\text{C}$  (unless otherwise noted) <sup>(1)</sup>

PARAMETER		TEST CONDITIONS		$T_A$	$V_{CC}$	MIN	TYP	MAX	UNIT
$C_i$	Digital input capacitance	$V_i = V_{CC}$ or GND	See Figure 16	25°C	2.5 V		2.6		pF
BW	Bandwidth	$R_L = 50 \Omega$ , -3 dB	See Figure 18	25°C	2.5 V		17		MHz
$O_{ISO}$	OFF isolation	$R_L = 50 \Omega$	f = 100 kHz, see Figure 20	25°C	2.5 V		-66		dB
$X_{TALK}$	Crosstalk	$R_L = 50 \Omega$	f = 100 kHz, see Figure 21	25°C	2.5 V		-75		dB
THD	Total harmonic distortion	$R_L = 600 \Omega$ , $C_L = 35 \text{ pF}$	f = 20 Hz to 20 kHz, see Figure 23	25°C	2.5 V		0.01%		
<b>Supply</b>									
$I_{CC}$	Positive supply current	$V_{COM}$ and $V_{IN} = V_{CC}$ or GND, $V_{NC}$ and $V_{NO} = \text{Floating}$		25°C	2.7 V		0.2	1.1	$\mu\text{A}$
				Full			1.3		
$I_{CC}$	Positive supply current	$V_{COM} = V_{CC} - 5.5 \text{ V}$ , $V_{IN} = V_{CC}$ or GND, $V_{NC}$ and $V_{NO} = \text{Floating}$		Full	2.7 V			3.3	$\mu\text{A}$

**6.6 Electrical Characteristics for 3.3-V Supply**
 $V_{CC} = 3 \text{ V to } 3.6 \text{ V}$ ,  $T_A = -40^\circ\text{C to } 85^\circ\text{C}$  (unless otherwise noted) <sup>(1)</sup>

PARAMETER		TEST CONDITIONS		$T_A$	$V_{CC}$	MIN	TYP	MAX	UNIT
<b>ANALOG SWITCH</b>									
$V_{COM}$ , $V_{NO}$ , $V_{NC}$	Analog signal range					$V_{CC} - 5.5$		$V_{CC}$	V
$R_{on}$	ON-state resistance	$V_{NC}$ or $V_{NO} \leq V_{CC}$ , 1.5 V, $V_{CC} - 5.5 \text{ V}$ , $I_{COM} = -100 \text{ mA}$	COM to NO or NC, see Figure 13	25°C	3 V		0.61	0.87	$\Omega$
				Full			0.97		
$\Delta R_{on}$	ON-state resistance match between channels	$V_{NC}$ or $V_{NO} = 1.5 \text{ V}$ , $I_{COM} = -100 \text{ mA}$	COM to NO or NC, see Figure 13	25°C	3 V		0.024	0.13	$\Omega$
				Full			0.13		
$R_{on(Flat)}$	ON-state resistance flatness	$V_{NC}$ or $V_{NO} \leq V_{CC}$ , 1.5 V, $V_{CC} - 5.5 \text{ V}$ , $I_{COM} = -100 \text{ mA}$	COM to NO or NC, see Figure 13	25°C	3 V		0.12	0.46	$\Omega$
				Full			0.5		
$I_{NC(OFF)}$ , $I_{NO(OFF)}$	NC, NO OFF leakage current	$V_{NC} = 3 \text{ V}$ , $V_{CC} - 5.5 \text{ V}$ $V_{COM} = V_{CC} - 5.5 \text{ V}$ , 3 V $V_{NO} = \text{Open}$ COM to NO or $V_{NO} = 3 \text{ V}$ , $V_{CC} - 5.5 \text{ V}$ , $V_{COM} = V_{CC} - 5.5 \text{ V}$ , 3 V $V_{NC} = \text{Open}$ COM to NC	See Figure 14	25°C	3.6 V		-50	50	nA
				Full			-375	375	
$I_{COM(ON)}$	COM ON leakage current	$V_{NC}$ and $V_{NO} = \text{Floating}$ , $V_{COM} = V_{CC}$ , $V_{CC} - 5.5 \text{ V}$	COM to NO or NC, see Figure 15	25°C	3.6 V		-50	50	nA
				Full			-375	375	
<b>DIGITAL CONTROL INPUTS (IN) <sup>(2)</sup></b>									
$V_{IH}$	Input logic high			Full			1.4	5.5	V
$V_{IL}$	Input logic low						0.8		
$I_{IH}$ , $I_{IL}$	Input leakage current	$V_{IN} = V_{CC}$ or 0		25°C	3.6 V		-250	250	nA
				Full			-250	250	
<b>DYNAMIC</b>									
$t_{ON}$	Turnon time	$V_{COM} = V_{CC}$ , $R_L = 300 \Omega$	$C_L = 35 \text{ pF}$ , see Figure 17	25°C	3.3 V		34	80	ns
				Full	3 V to 3.6 V		120		

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

## Electrical Characteristics for 3.3-V Supply (continued)

 $V_{CC} = 3\text{ V to }3.6\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted) <sup>(1)</sup>

PARAMETER		TEST CONDITIONS		$T_A$	$V_{CC}$	MIN	TYP	MAX	UNIT
$t_{OFF}$	Turnoff time	$V_{COM} = V_{CC}$ , $R_L = 300\ \Omega$	$C_L = 35\text{ pF}$ , see Figure 17	25°C	3.3 V		19	70	ns
				Full	3 V to 3.6 V			70	
$t_{BBM}$	Break-before-make time	See Figure 18		25°C	3.3 V	1	7		ns
$Q_C$	Charge injection	$V_{GEN} = 0$ , $R_{GEN} = 0$	$C_L = 1\text{ nF}$ , see Figure 22	25°C	3.3 V		150		pC
$C_{NC(OFF)}$ , $C_{NO(OFF)}$	NC, NO OFF capacitance	$V_{NC}$ or $V_{NO} = V_{CC}$ or $V_{CC} - 5.5\text{ V}$	See Figure 16	25°C	3.3 V		70		pF
$C_{COM(ON)}$	NC, NO, COM ON capacitance	$V_{COM} = V_{CC}$ or GND, $f = 10\text{ MHz}$	See Figure 16	25°C	3.3 V		370		pF
$C_I$	Digital input capacitance	$V_I = V_{CC}$ or GND	See Figure 16	25°C	3.3 V		2.6		pF
BW	Bandwidth	$R_L = 50\ \Omega$ , -3 dB	Switch ON, see Figure 18	25°C	3.3 V		17.5		MHz
$O_{ISO}$	OFF isolation	$R_L = 50\ \Omega$	$f = 100\text{ kHz}$ , see Figure 20	25°C	3.3 V		-68		dB
$X_{TALK}$	Crosstalk	$R_L = 50\ \Omega$	$f = 100\text{ kHz}$ , see Figure 21	25°C	3.3 V		-76		dB
THD	Total harmonic distortion	$R_L = 600\ \Omega$ , $C_L = 35\text{ pF}$	$f = 20\text{ Hz to }20\text{ kHz}$ , see Figure 23	25°C	3.3 V		0.008%		
<b>SUPPLY</b>									
$I_{CC}$	Positive supply current	$V_{COM}$ and $V_{IN} = V_{CC}$ or GND, $V_{NC}$ and $V_{NO} = \text{Floating}$		25°C	3.6 V		0.1	1.2	$\mu\text{A}$
				Full				1.3	
				Full	3.6 V			3.4	$\mu\text{A}$

## 6.7 Electrical Characteristics for 5-V Supply

 $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted) <sup>(1)</sup>

PARAMETER		TEST CONDITIONS		$T_A$	$V_{CC}$	MIN	TYP	MAX	UNIT
<b>ANALOG SWITCH</b>									
$V_{COM}$ , $V_{NO}$ , $V_{NC}$	Analog signal range					$V_{CC} - 5.5$		$V_{CC}$	V
$R_{on}$	ON-state resistance	$V_{NC}$ or $V_{NO} = V_{CC}$ , 1.6 V, $V_{CC} = -5.5\text{ V}$ , $I_{COM} = -100\text{ mA}$	COM to NO or NC, see Figure 13	25°C	4.5 V		0.52	0.74	$\Omega$
				Full				0.83	
$\Delta R_{on}$	ON-state resistance match between channels	$V_{NC}$ or $V_{NO} = 1.6\text{ V}$ , $I_{COM} = -100\text{ mA}$	COM to NO or NC, see Figure 13	25°C	4.5 V		0.04	0.23	$\Omega$
				Full				0.30	
$R_{on(Flat)}$	ON-state resistance flatness	$V_{NC}$ or $V_{NO} = V_{CC}$ , 1.6 V, $V_{CC} = -5.5\text{ V}$ , $I_{COM} = -100\text{ mA}$	COM to NO or NC, see Figure 13	25°C	4.5 V		0.076	0.46	$\Omega$
				Full				0.5	
$I_{NC(OFF)}$ , $I_{NO(OFF)}$	NC, NO OFF leakage current	$V_{NC} = 4.5\text{ V}$ , $V_{CC} = 5.5\text{ V}$ , $V_{COM} = V_{CC} - 5.5\text{ V}$ , 4.5 V, $V_{NO} = \text{Open}$ , COM to NO or $V_{NO} = 4.5\text{ V}$ , $V_{CC} = 5.5\text{ V}$ , $V_{COM} = V_{CC} - 5.5\text{ V}$ , 4.5 V, $V_{NC} = \text{Open}$ , COM to NC	See Figure 14	25°C	5.5 V		-50	50	nA
				Full				-375	
$I_{COM(ON)}$	COM ON leakage current	$V_{NC}$ and $V_{NO} = \text{Floating}$ , $V_{COM} = V_{CC}$ , $V_{CC} = 5.5\text{ V}$	See Figure 15	25°C	5.5 V		-50	50	nA
				Full				-375	
<b>DIGITAL CONTROL INPUTS (IN) <sup>(2)</sup></b>									

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

**Electrical Characteristics for 5-V Supply (continued)**
 $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ ,  $T_A = -40^\circ\text{C to } 85^\circ\text{C}$  (unless otherwise noted) <sup>(1)</sup>

PARAMETER		TEST CONDITIONS		$T_A$	$V_{CC}$	MIN	TYP	MAX	UNIT
$V_{IH}$	Input logic high			Full		2.4		5.5	V
$V_{IL}$	Input logic low						0.8		
$I_{IH}, I_{IL}$	Input leakage current	$V_{IN} = V_{CC}$ or 0		25°C	5.5 V	-250		250	nA
				Full		-250	250		
<b>DYNAMIC</b>									
$t_{ON}$	Turnon time	$V_{COM} = V_{CC}$ , $R_L = 300 \Omega$	$C_L = 35 \text{ pF}$ , see <a href="#">Figure 17</a>	25°C	5 V		27	80	ns
				Full	4.5 V to 5.5 V			80	
$t_{OFF}$	Turnoff time	$V_{COM} = V_{CC}$ , $R_L = 300 \Omega$	$C_L = 35 \text{ pF}$ , see <a href="#">Figure 17</a>	25°C	5 V		13	70	ns
				Full	4.5 V to 5.5 V			70	
$t_{BBM}$	Break-before-make time	$V_{NC} = V_{NO} = V_{CC}/2$ $R_L = 300 \Omega$	$C_L = 35 \text{ pF}$ , see <a href="#">Figure 18</a>	25°C	5 V	1	3.5		ns
$Q_C$	Charge injection	$V_{GEN} = 0$ , $R_{GEN} = 0$	$C_L = 1 \text{ nF}$ , see <a href="#">Figure 22</a>	25°C	5 V		10		pC
$C_{NC(OFF)}, C_{NO(OFF)}$	NC, NO OFF capacitance	$V_{NC}$ or $V_{NO} = V_{CC}$ or $V_{CC} - 5.5 \text{ V}$	See <a href="#">Figure 16</a>	25°C	5 V		70		pF
$C_{COM(ON)}$	NC, NO, COM ON capacitance	$V_{COM} = V_{CC}$ or GND,	See <a href="#">Figure 16</a>	25°C	5 V		370		pF
$C_i$	Digital input capacitance	$V_i = V_{CC}$ or GND	See <a href="#">Figure 16</a>	25°C	5 V		2.6		pF
BW	Bandwidth	$R_L = 50 \Omega$	See <a href="#">Figure 18</a>	25°C	5 V		18.3		MHz
$O_{ISO}$	OFF isolation	$R_L = 50 \Omega$	$f = 100 \text{ kHz}$ , see <a href="#">Figure 20</a>	25°C	5 V		-70		dB
$X_{TALK}$	Crosstalk	$R_L = 50 \Omega$	$f = 100 \text{ kHz}$ , see <a href="#">Figure 21</a>	25°C	5 V		-78		dB
THD	Total harmonic distortion	$R_L = 600 \Omega$ , $C_L = 35 \text{ pF}$	$f = 20 \text{ Hz to } 20 \text{ kHz}$ , see <a href="#">Figure 23</a>	25°C	5 V		0.009%		
<b>SUPPLY</b>									
$I_{CC}$	Positive supply current	$V_{COM}$ and $V_{IN} = V_{CC}$ or GND, $V_{NC}$ and $V_{NO} = \text{Floating}$		25°C	5.5 V		0.2	1.3	$\mu\text{A}$
				Full			3.5		
				Full			5		



### 6.8 Typical Characteristics

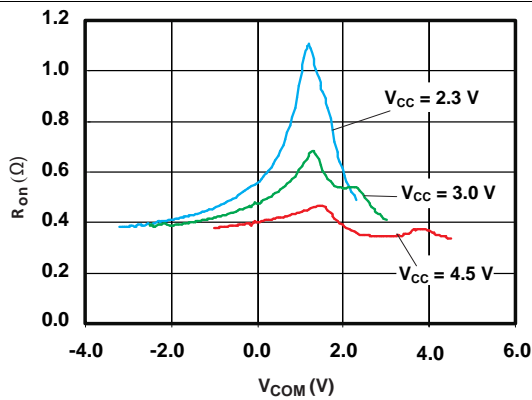


Figure 1.  $R_{on}$  vs  $V_{COM}$

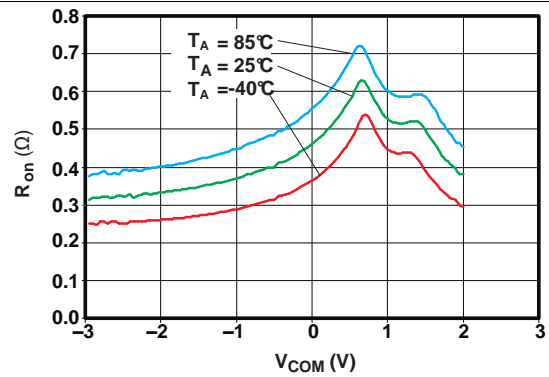


Figure 2.  $R_{on}$  vs  $V_{COM}$  ( $V_{CC} = 2.7\text{ V}$ )

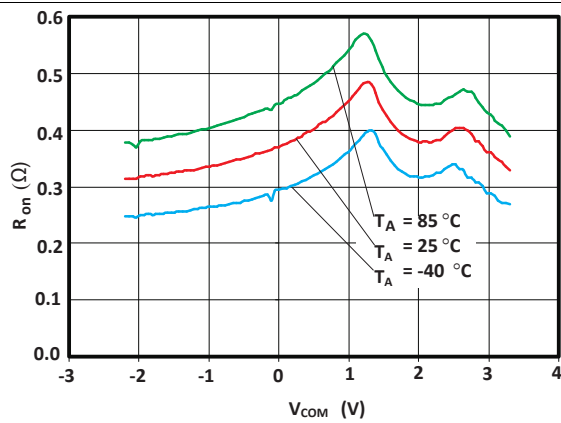


Figure 3.  $R_{on}$  vs  $V_{COM}$  ( $V_{CC} = 3.3\text{ V}$ )

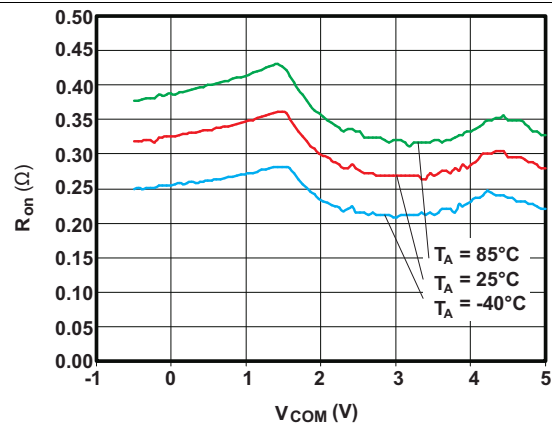


Figure 4.  $R_{on}$  vs  $V_{COM}$  ( $V_{CC} = 5\text{ V}$ )

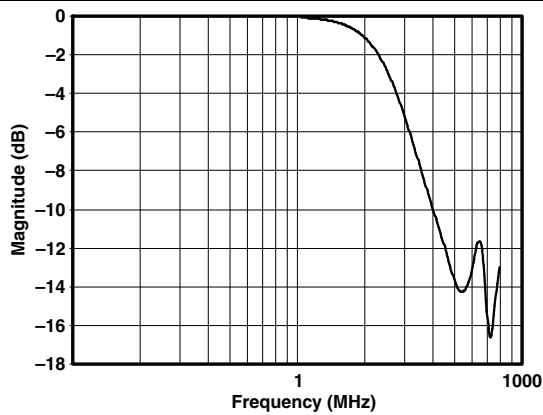


Figure 5. Insertion Loss

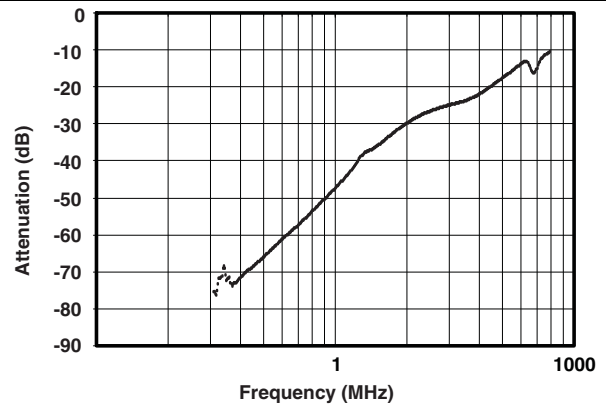


Figure 6. Off Isolation vs Frequency

Typical Characteristics (continued)

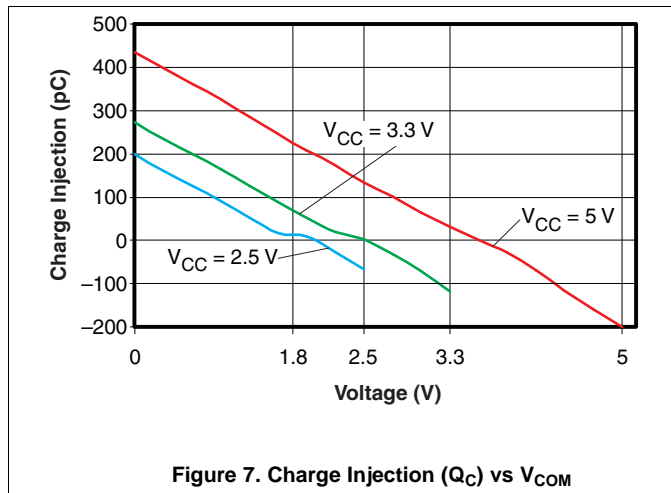


Figure 7. Charge Injection ( $Q_C$ ) vs  $V_{COM}$

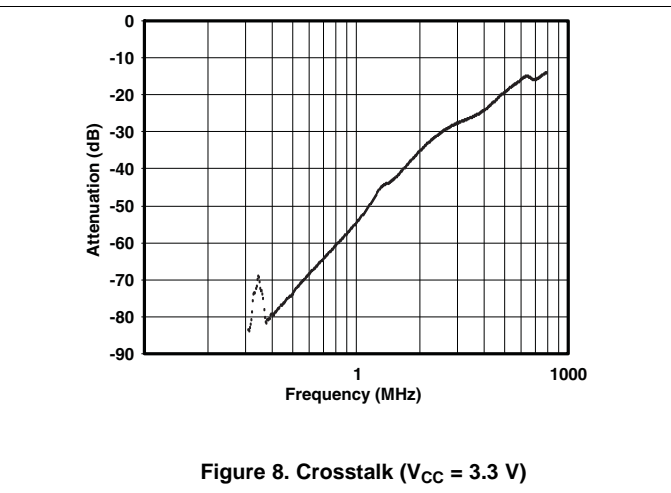


Figure 8. Crosstalk ( $V_{CC} = 3.3\text{ V}$ )

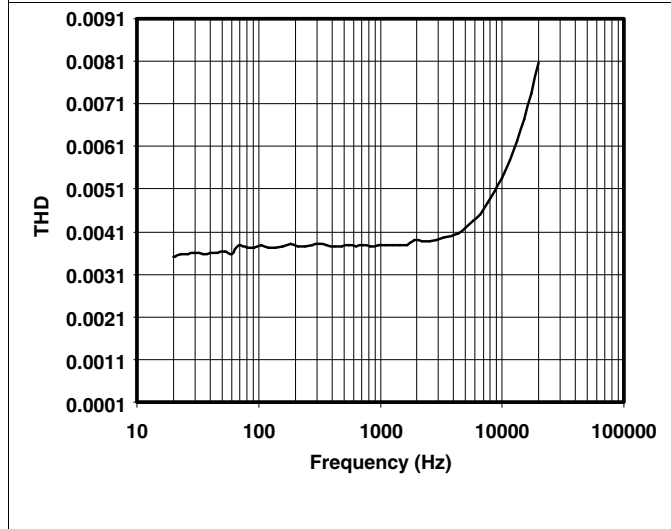


Figure 9. Total Harmonic Distortion vs Frequency

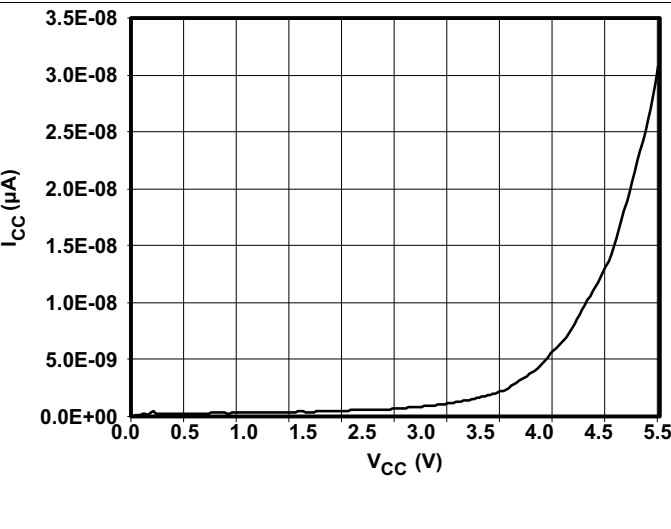


Figure 10. Power-Supply Current vs  $V_{CC}$

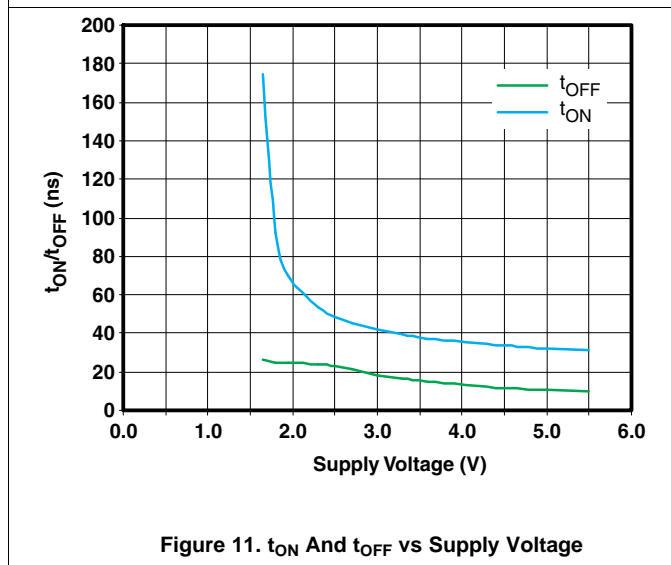


Figure 11.  $t_{ON}$  And  $t_{OFF}$  vs Supply Voltage

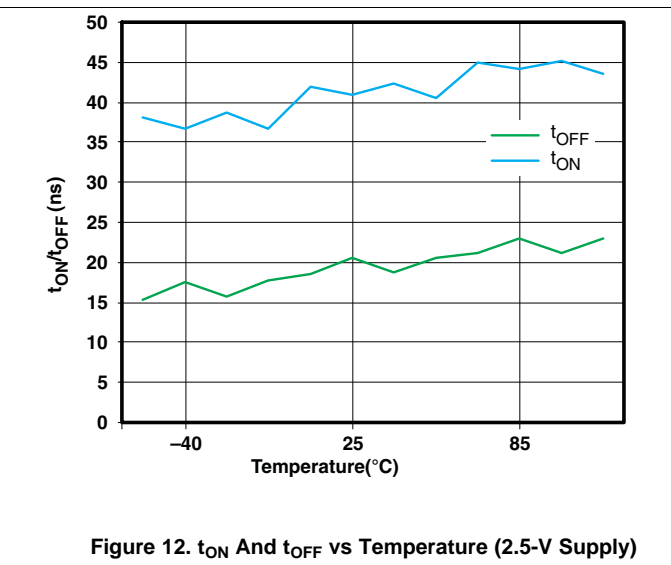


Figure 12.  $t_{ON}$  And  $t_{OFF}$  vs Temperature (2.5-V Supply)

## 7 Parameter Measurement Information

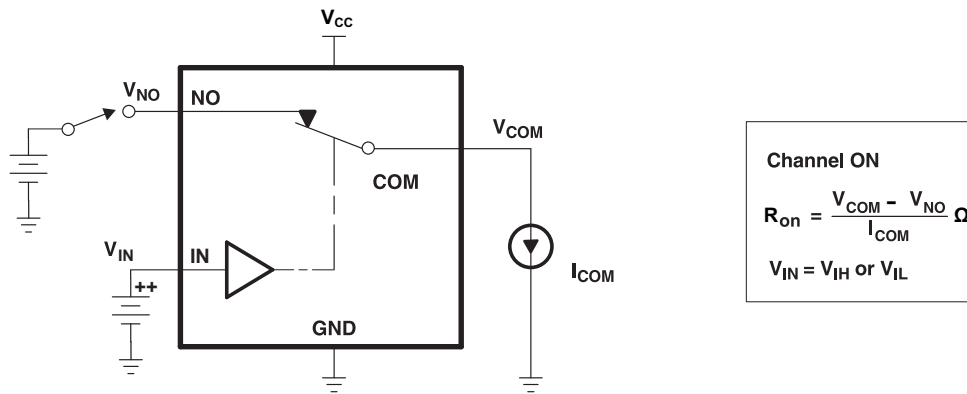


Figure 13. ON-state resistance ( $R_{on}$ )

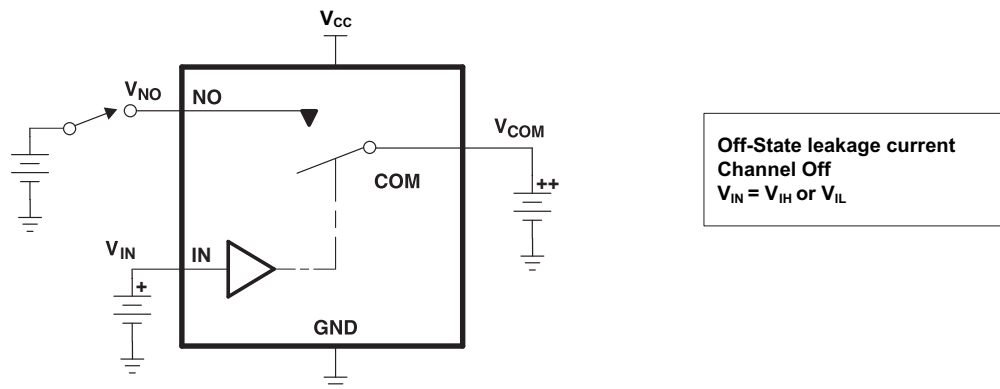


Figure 14. OFF-state leakage current ( $I_{COM(OFF)}$ ,  $I_{NO(OFF)}$ )

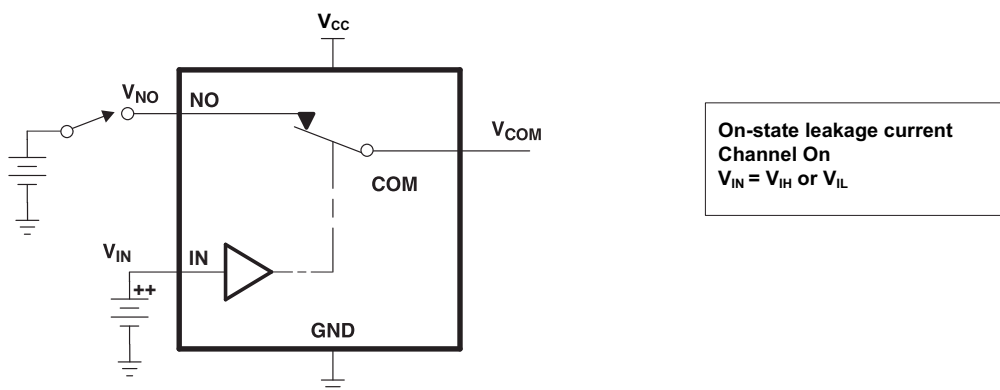


Figure 15. ON-state leakage current ( $I_{COM(ON)}$ ,  $I_{NO(ON)}$ )

Parameter Measurement Information (continued)

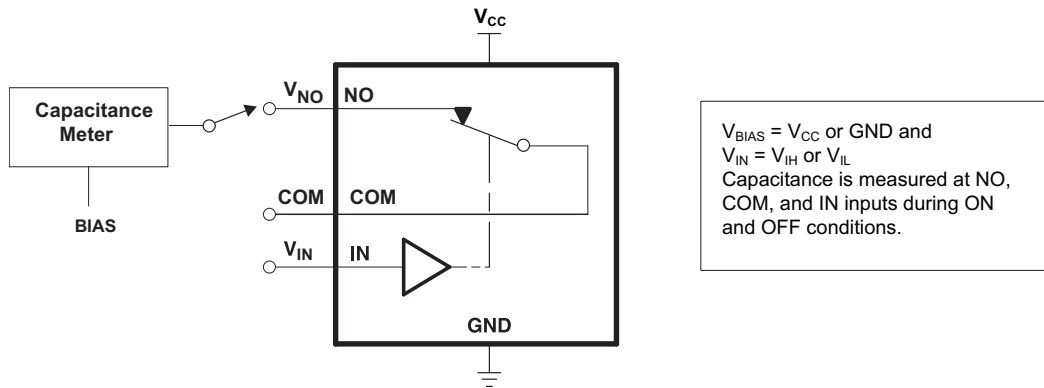
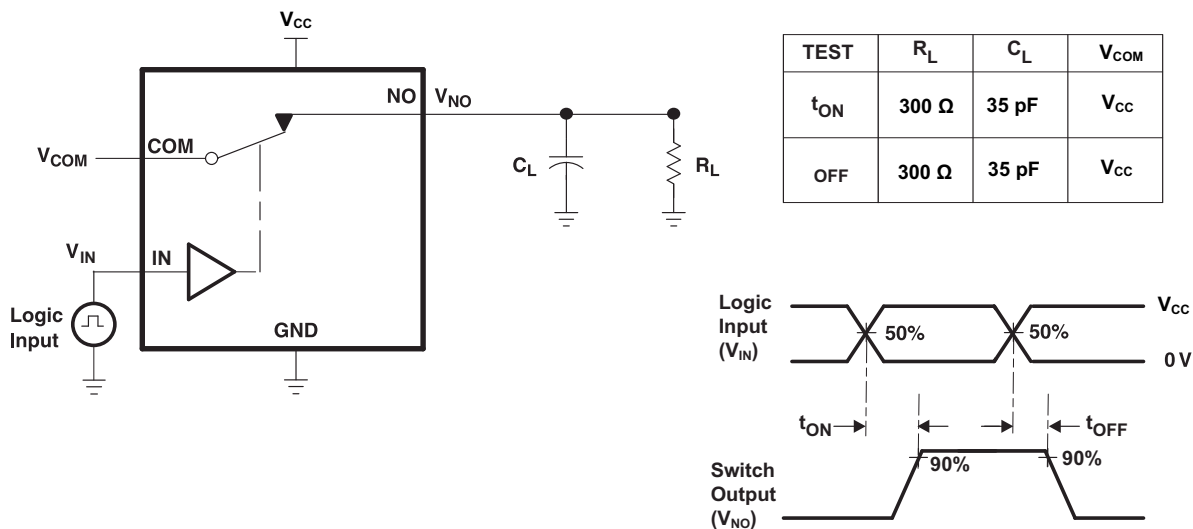


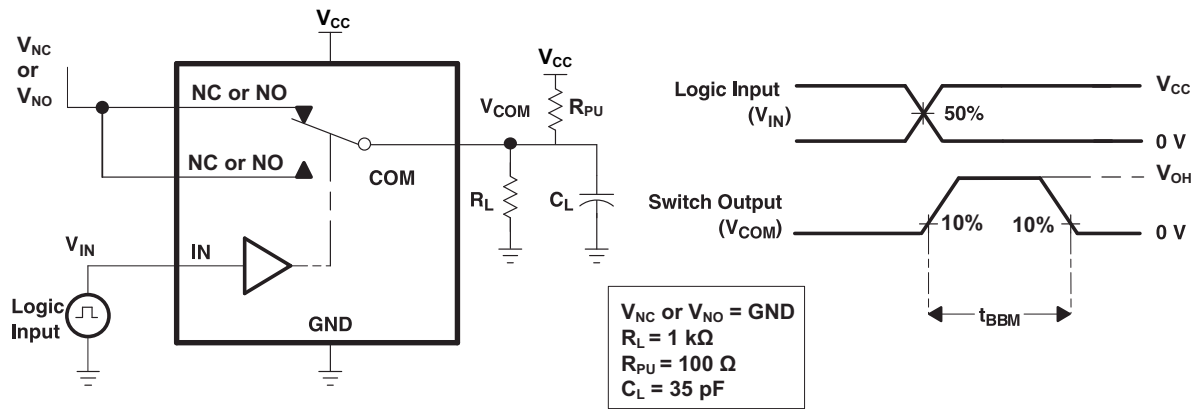
Figure 16. Capacitance ( $C_I$ ,  $C_{COM(OFF)}$ ,  $C_{COM(ON)}$ ,  $C_{NO(OFF)}$ ,  $C_{NO(ON)}$ )



- A. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r < 5$  ns,
- B.  $C_L$  includes probe and jig capacitance.

Figure 17. Turnon ( $t_{ON}$ ) and Turnoff time ( $t_{OFF}$ )

Parameter Measurement Information (continued)



- A.  $C_L$  includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r < 5\text{ ns}$ ,  $t_f < 5\text{ ns}$ .

Figure 18. Break-Before-Make Time ( $t_{BBM}$ )

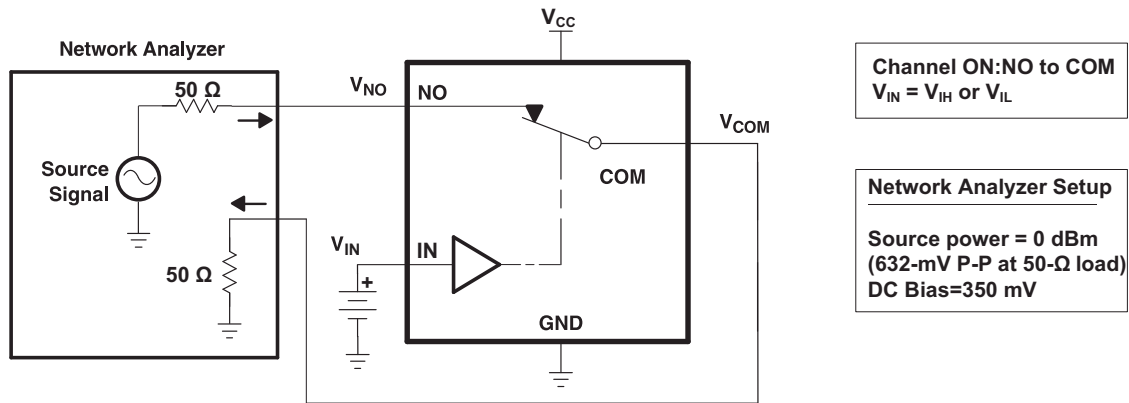


Figure 19. Bandwidth (BW)

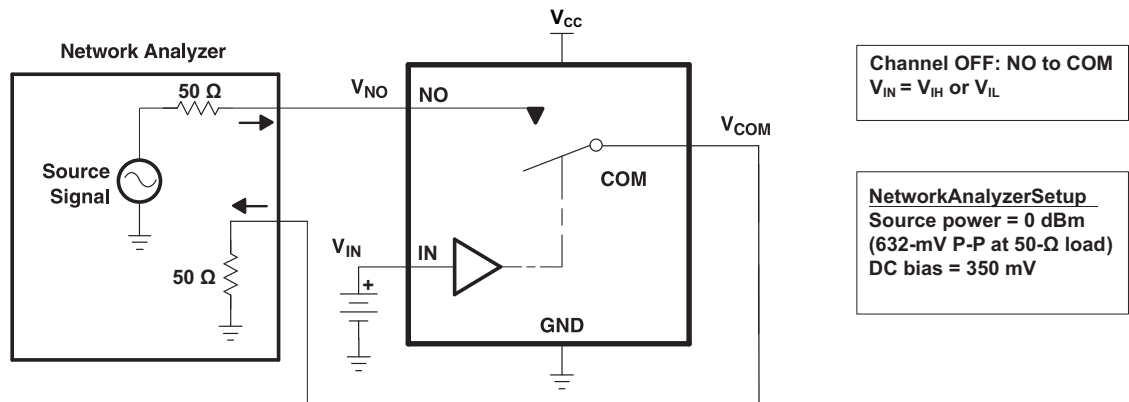


Figure 20. OFF isolation ( $O_{ISO}$ )

Parameter Measurement Information (continued)

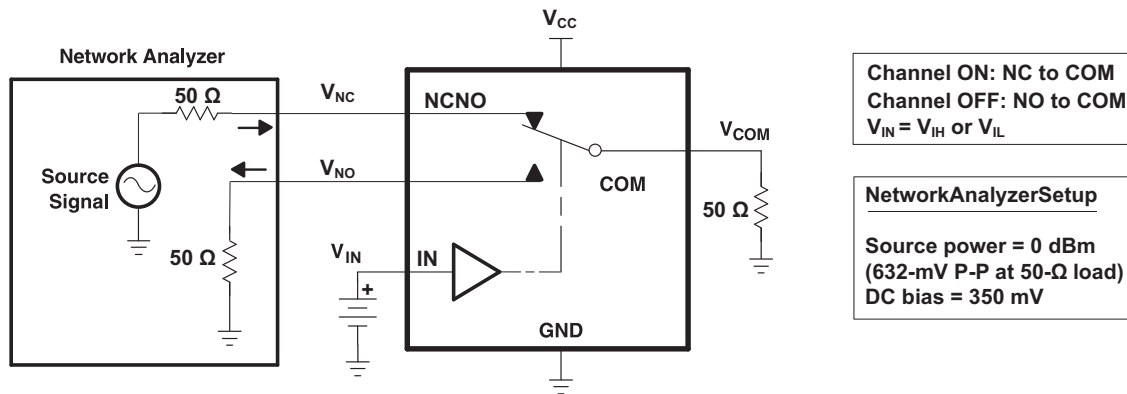
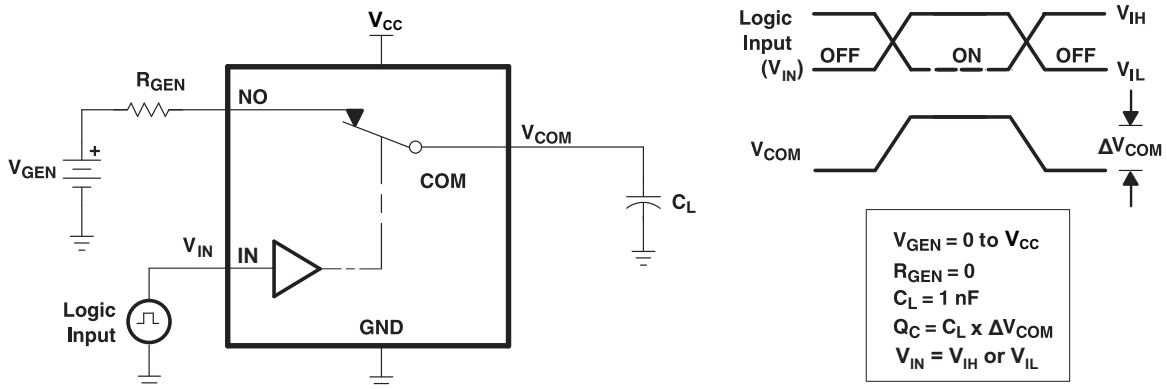
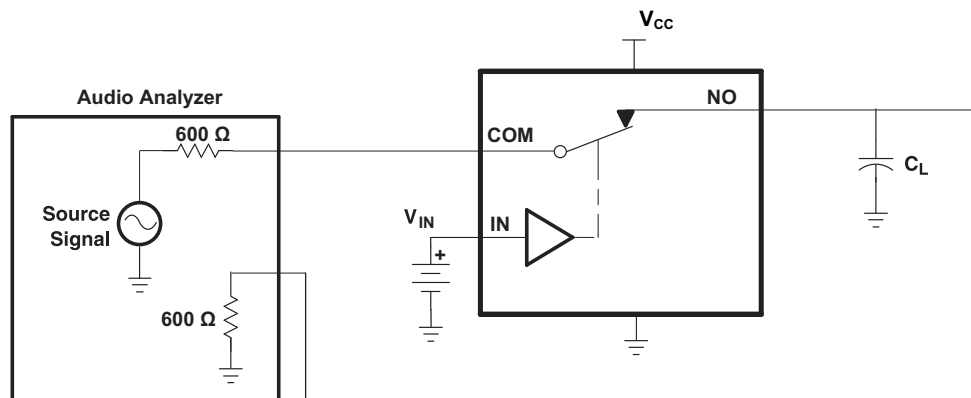
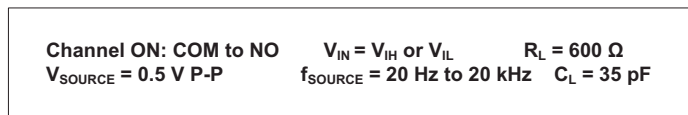


Figure 21. Crosstalk ( $X_{TALK}$ )



- A. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r < 5$  ns,  $t_f < 5$  ns.
- B.  $C_L$  includes probe and jig capacitance.

Figure 22. Charge injection ( $Q_C$ )



- A.  $C_L$  includes probe and jig capacitance.

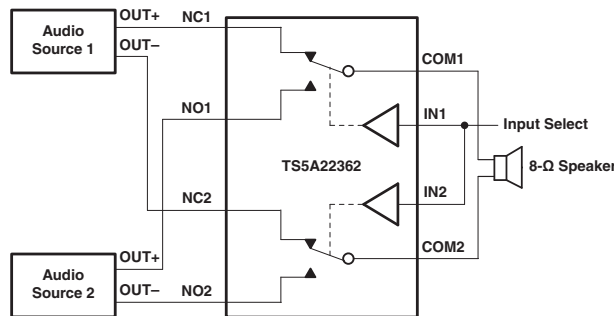
Figure 23. Total Harmonic Distortion (THD)

## 8 Detailed Description

### 8.1 Overview

The TS5A22362 is a bidirectional, 2-channel single-pole double-throw (SPDT) analog switches designed to operate from 2.3 V to 5.5 V. The devices feature negative signal capability that allows signals below ground to pass through the switch without distortion. The break-before-make feature prevents signal distortion during the transferring of a signal from one path to another. Low ON-state resistance, excellent channel-to-channel ON-state resistance matching, and minimal total harmonic distortion (THD) performance are ideal for audio applications.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 Negative Signaling Capacity

The TS5A22362 dual SPDT switches feature negative signal capability that allows signals below ground to pass through without distortion. These analog switches operate from a single +2.3-V to +5.5-V supply. The input and output signal swing of the device is dependant of the supply voltage  $V_{CC}$ : the devices pass signals as high as  $V_{CC}$  and as low as  $V_{CC} - 5.5$  V, including signals below ground with minimal distortion.

Table 1 shows the input/output signal swing the user can get with different supply voltages.

Table 1. Input/Output signal swing

SUPPLY VOLTAGE, $V_{CC}$	MINIMUM ( $V_{NC}, V_{NO}, V_{COM}$ ) = $V_{CC} - 5.5$	MAXIMUM ( $V_{NC}, V_{NO}, V_{COM}$ ) = $V_{CC}$
5.5 V	0 V	5.5 V
4.5 V	-1.9 V	4.5 V
3.6 V	-2.5 V	3.6 V
3.0 V	-2.5 V	3.0 V
2.7 V	-2.8 V	2.7 V
2.3 V	-3.2 V	2.3 V

### 8.4 Device Functional Modes

The function table for TS5A22362 is shown in Table 2

Table 2. Function Table

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

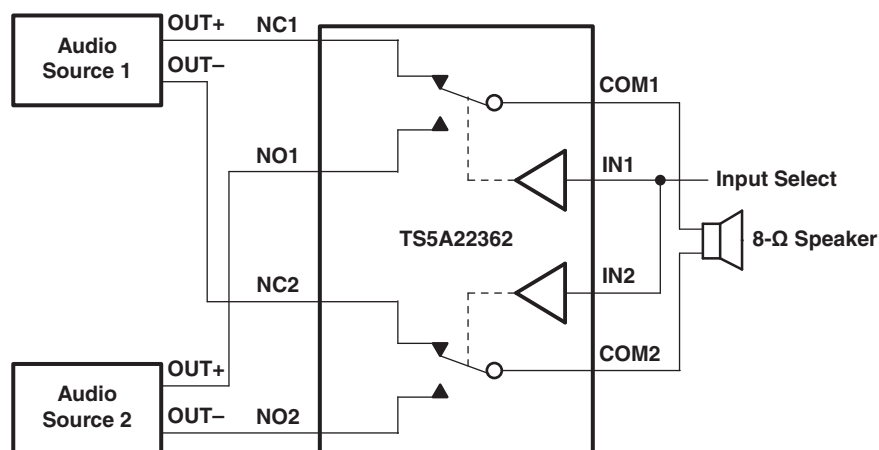
### 9.1 Application Information

Ensure that the device is powered up with a supply voltage on VCC before a voltage can be applied to the signal paths NC and NO.

Tie the digitally controlled inputs select pins IN1 and IN2 to VCC or GND to avoid unwanted switch states that could result if the logic control pins are left floating.

All unused digital inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

### 9.2 Typical Application



**Figure 24. Typical Application**

#### 9.2.1 Design Requirements

Tie the digitally controlled inputs select pins IN1 and IN2 to VCC or GND to avoid unwanted switch states that could result if the logic control pins are left floating.

#### 9.2.2 Detailed Design Procedure

Select the appropriate supply voltage to cover the entire voltage swing of the signal passing through the switch because the TS5A22362 operates from a single +2.3-V to +5.5-V supply and the input/output signal swing of the device is dependant of the supply voltage VCC. The device will pass signals as high as VCC and as low as VCC – 5.5 V. Use table 2 as a guide for selecting supply voltage based on the signal passing through the switch.

Ensure that the device is powered up with a supply voltage on VCC before a voltage can be applied to the signal paths NC and NO.



Typical Application (continued)

9.2.3 Application Curve

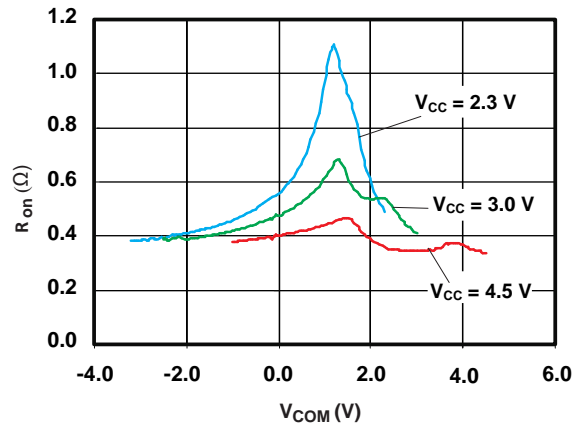


Figure 25. R<sub>on</sub> vs V<sub>COM</sub>

## 10 Power Supply Recommendations

The TS5A22362 operates from a single 2.3-V to 5.5-V supply. The device must be powered up with a supply voltage on VCC before a voltage can be applied to the signal paths NC and NO. It is recommended to include a 100- $\mu$ s delay after VCC is at voltage before applying a signal on NC and NO paths

It is also good practice to place a 0.1- $\mu$ F bypass capacitor on the supply pin VCC to GND to smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

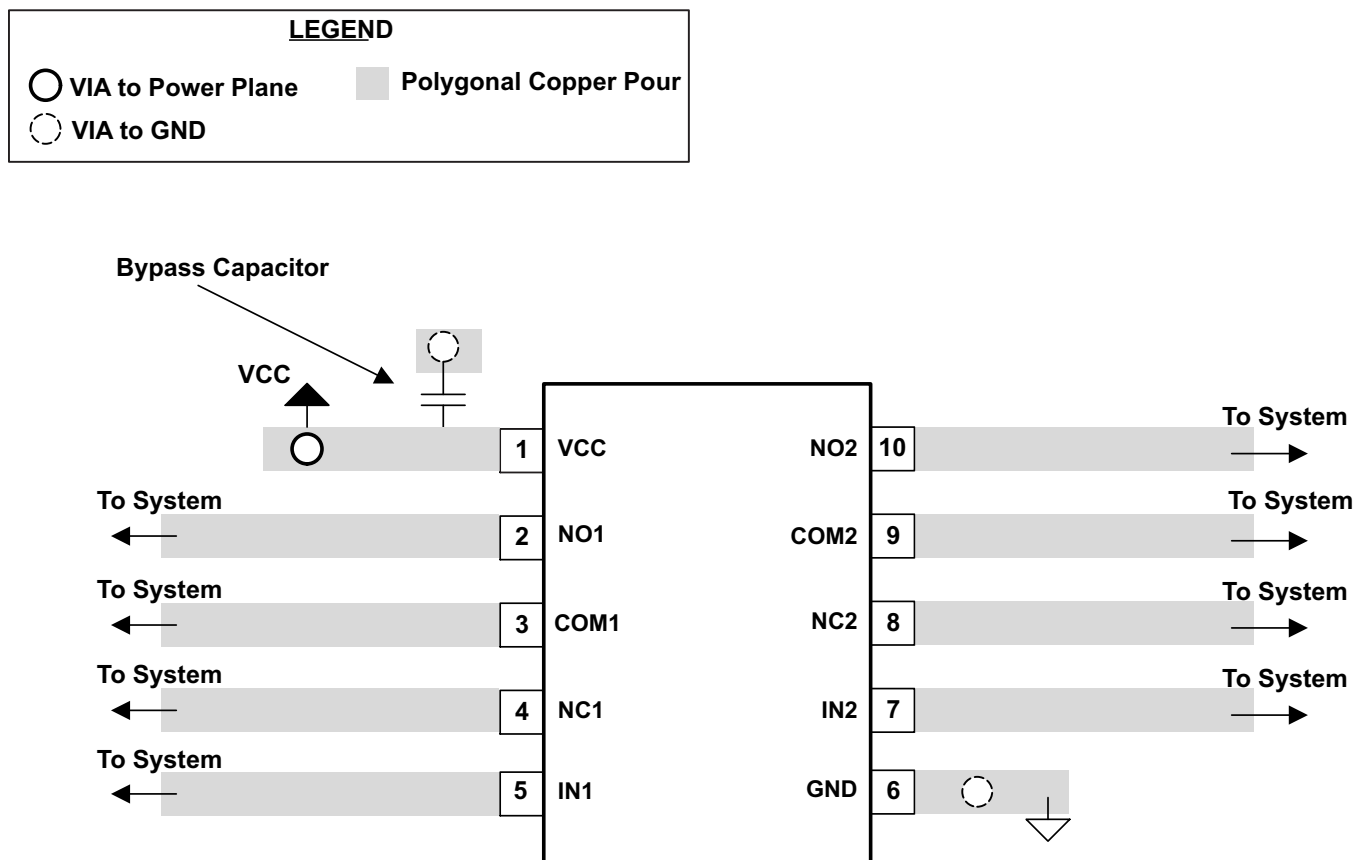
## 11 Layout

### 11.1 Layout Guidelines

TI recommends placing a bypass capacitor as close to the supply pin VCC as possible to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

Minimize trace lengths and vias on the signal paths in order to preserve signal integrity.

### 11.2 Layout Example



## 12 Device and Documentation Support

### 12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.3 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
HPA02208YZPR	ACTIVE	DSBGA	YZP	10	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(39 ~ 392)	<a href="#">Samples</a>
TS5A22362DGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	39R	<a href="#">Samples</a>
TS5A22362DGSRG4	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	39R	<a href="#">Samples</a>
TS5A22362DRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZVG	<a href="#">Samples</a>
TS5A22362DRCT-NM	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	ZVGNM	<a href="#">Samples</a>
TS5A22362YZPR	ACTIVE	DSBGA	YZP	10	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(39 ~ 392)	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



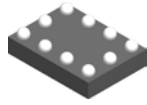
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A22362DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TS5A22362DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TS5A22362DRCT-NM	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TS5A22362YZPR	DSBGA	YZP	10	3000	178.0	9.2	1.49	1.99	0.63	4.0	8.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A22362DGSR	VSSOP	DGS	10	2500	358.0	335.0	35.0
TS5A22362DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TS5A22362DRCT-NM	VSON	DRC	10	250	210.0	185.0	35.0
TS5A22362YZPR	DSBGA	YZP	10	3000	220.0	220.0	35.0

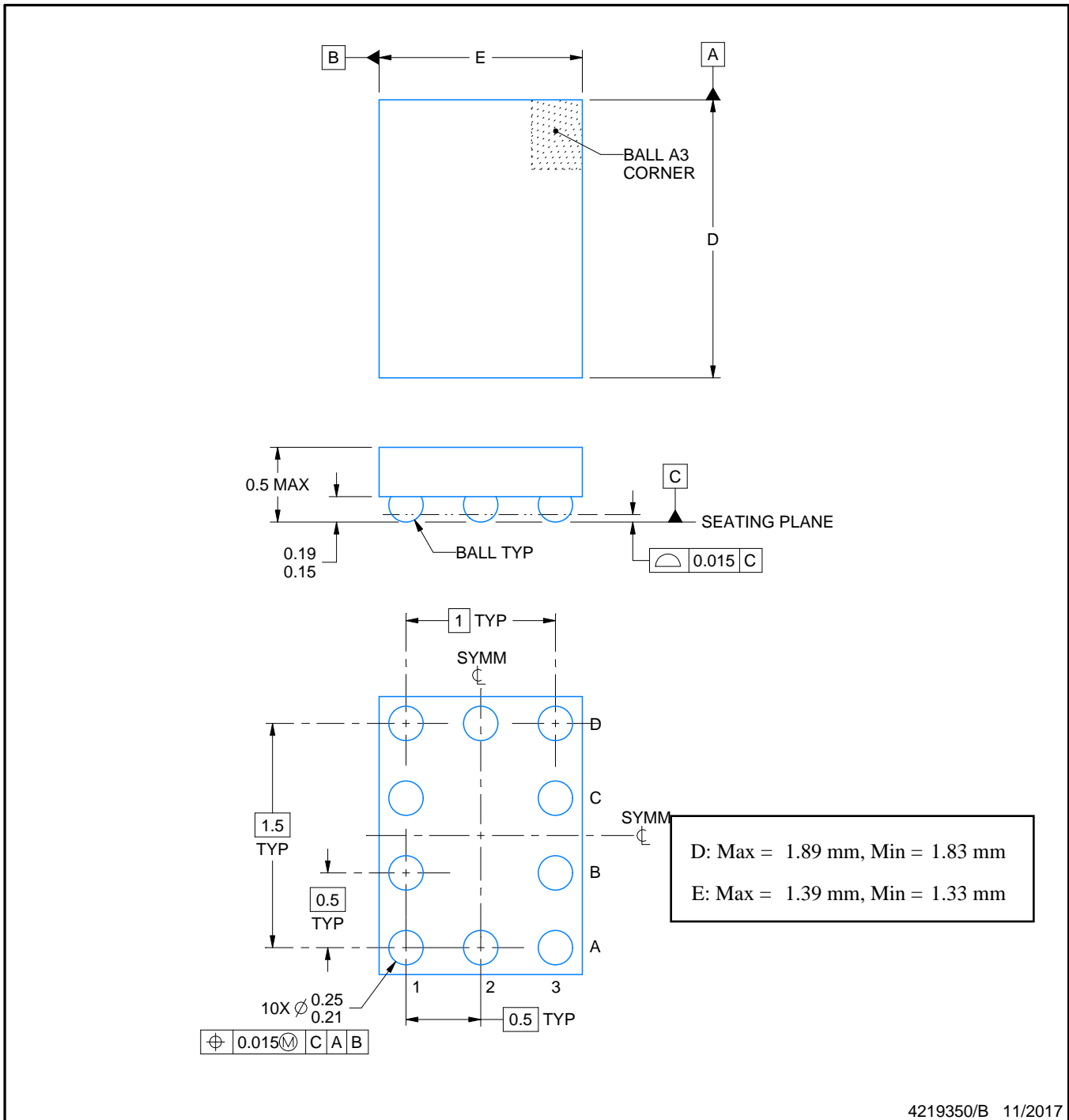


# PACKAGE OUTLINE

YZP0010

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

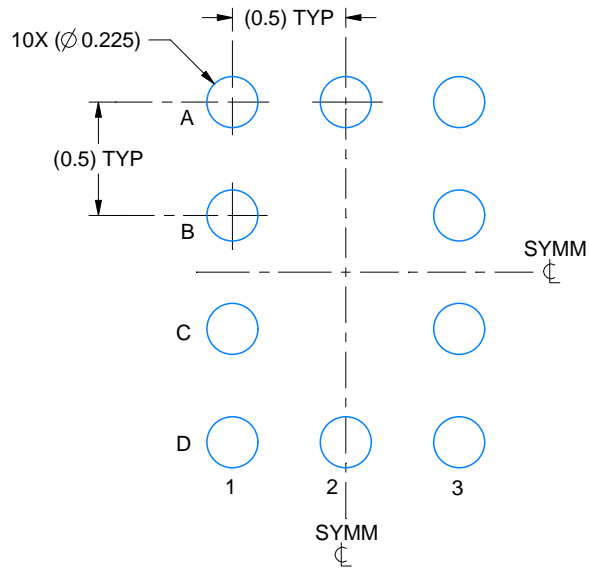


# EXAMPLE BOARD LAYOUT

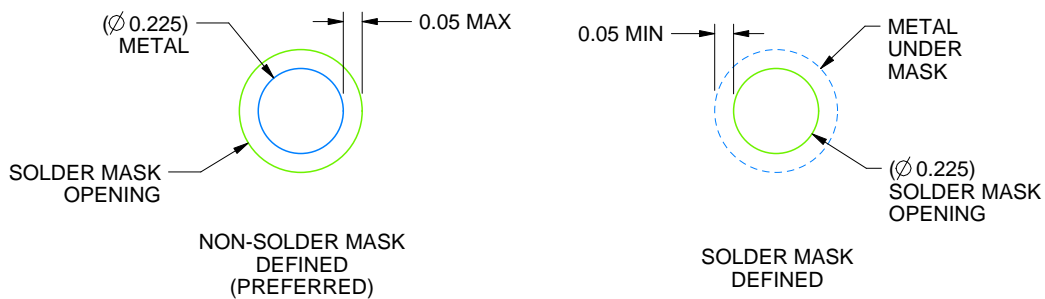
YZP0010

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:30X



SOLDER MASK DETAILS  
NOT TO SCALE

4219350/B 11/2017

NOTES: (continued)

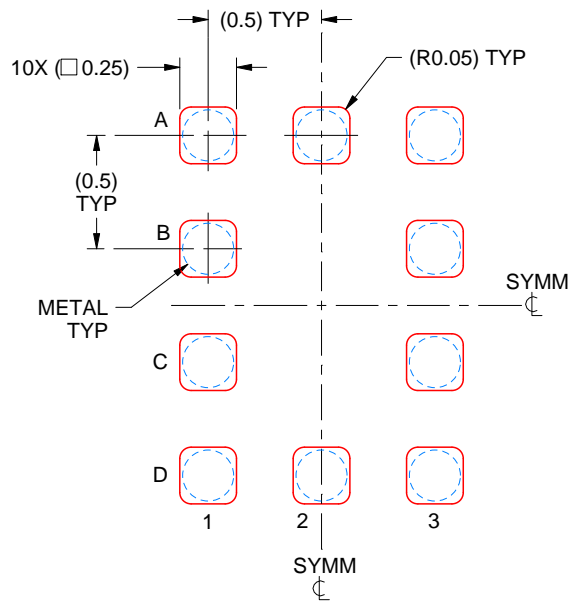
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 ([www.ti.com/lit/sbva017](http://www.ti.com/lit/sbva017)).

# EXAMPLE STENCIL DESIGN

YZP0010

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:30X

4219350/B 11/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

DRC (S-PVSON-N10)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Small Outline No-Lead (SON) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present.

# THERMAL PAD MECHANICAL DATA

DRC (S-PVSON-N10)

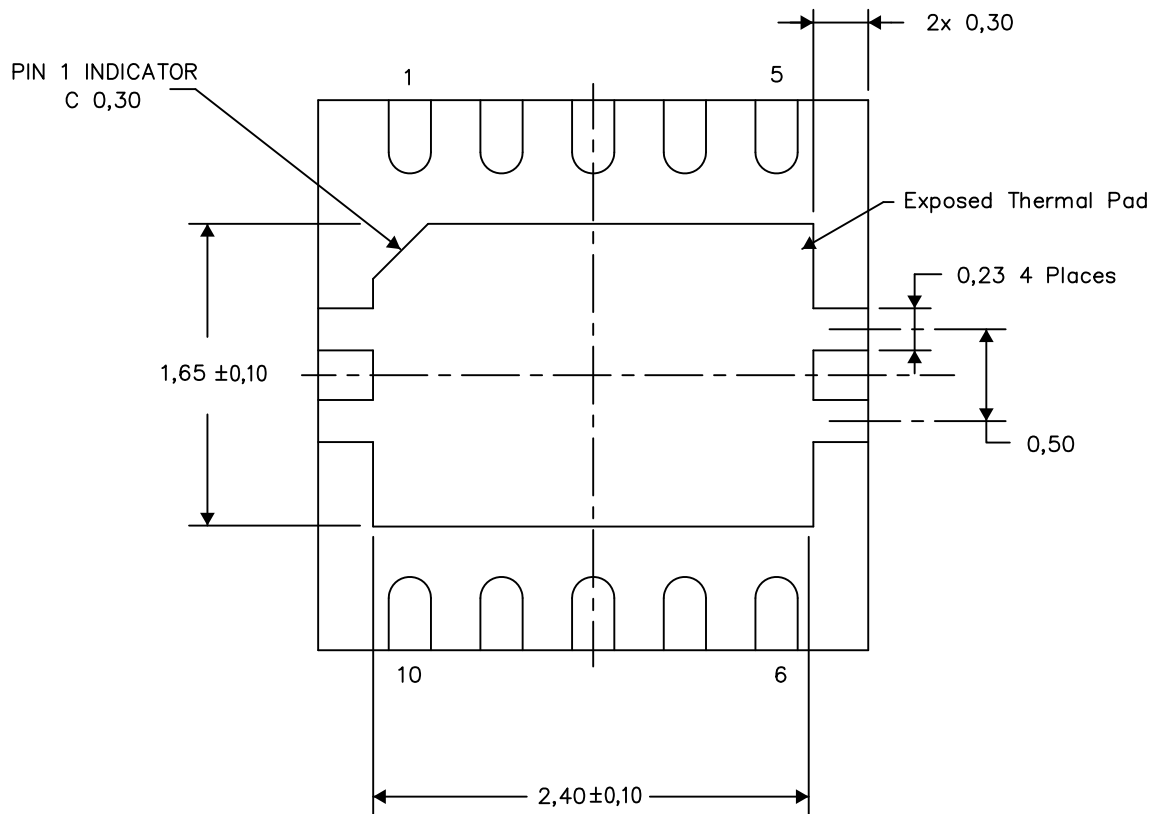
PLASTIC SMALL OUTLINE NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

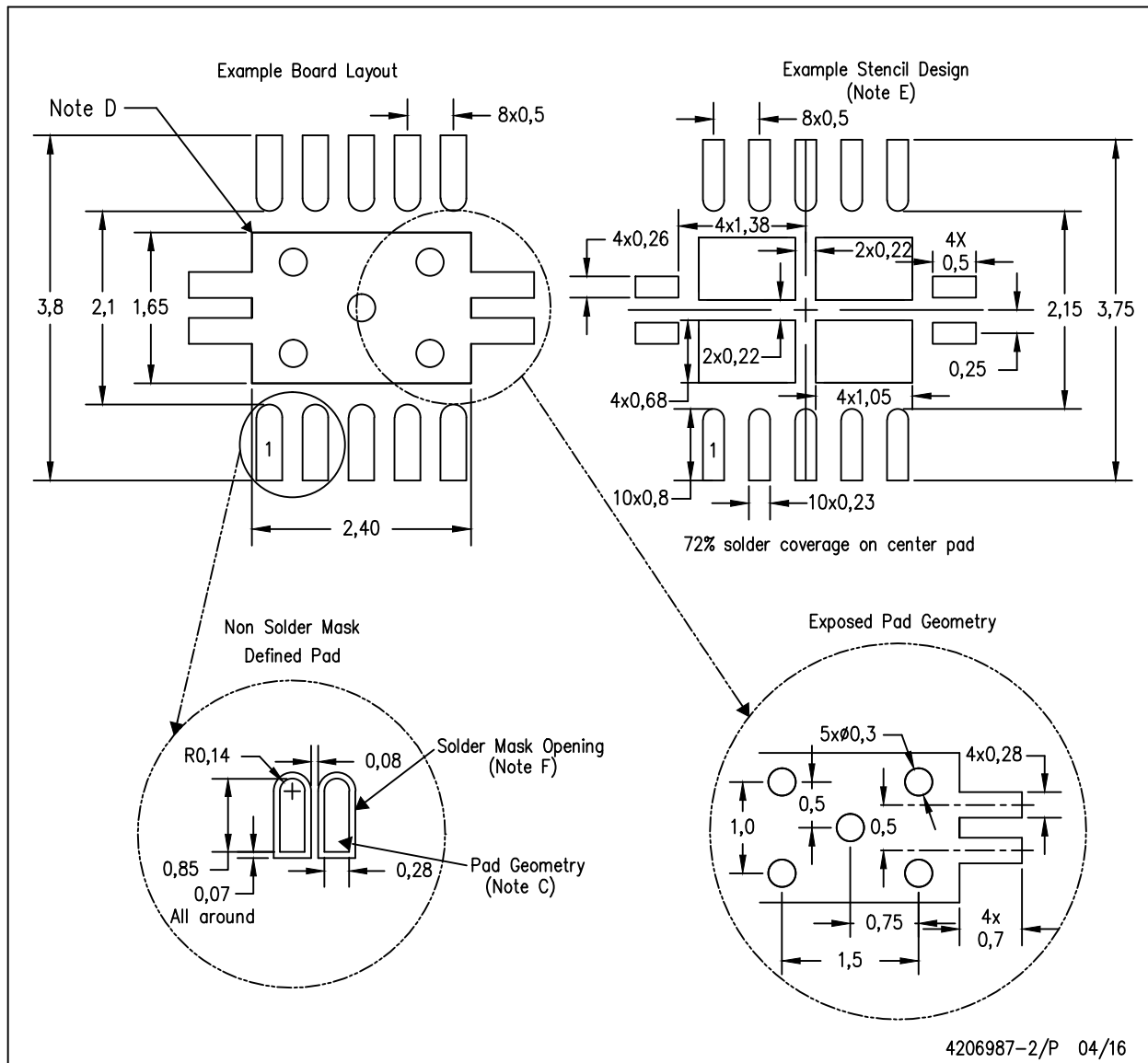
4206565-3/Y 08/15

NOTE: A. All linear dimensions are in millimeters

# LAND PATTERN DATA

DRC (S-PVSON-N10)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

# THERMAL PAD MECHANICAL DATA

DRC (S-PVSON-N10)

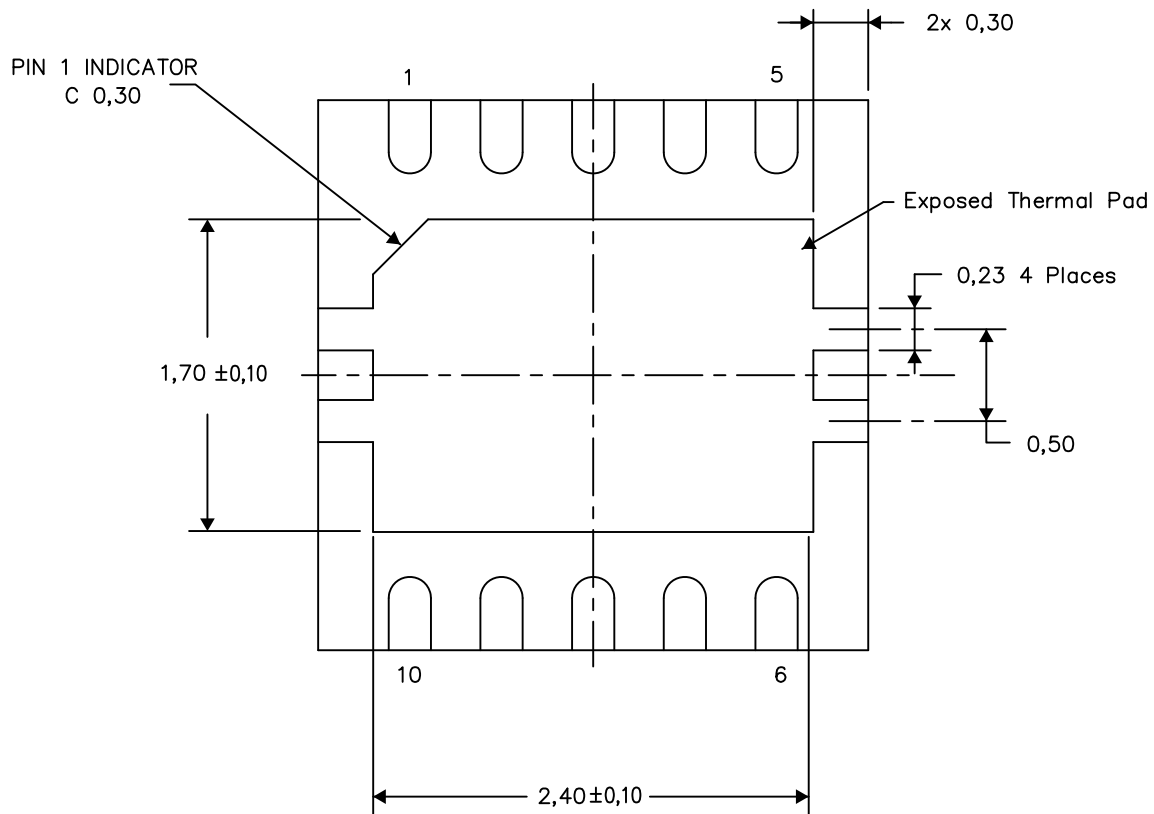
PLASTIC SMALL OUTLINE NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

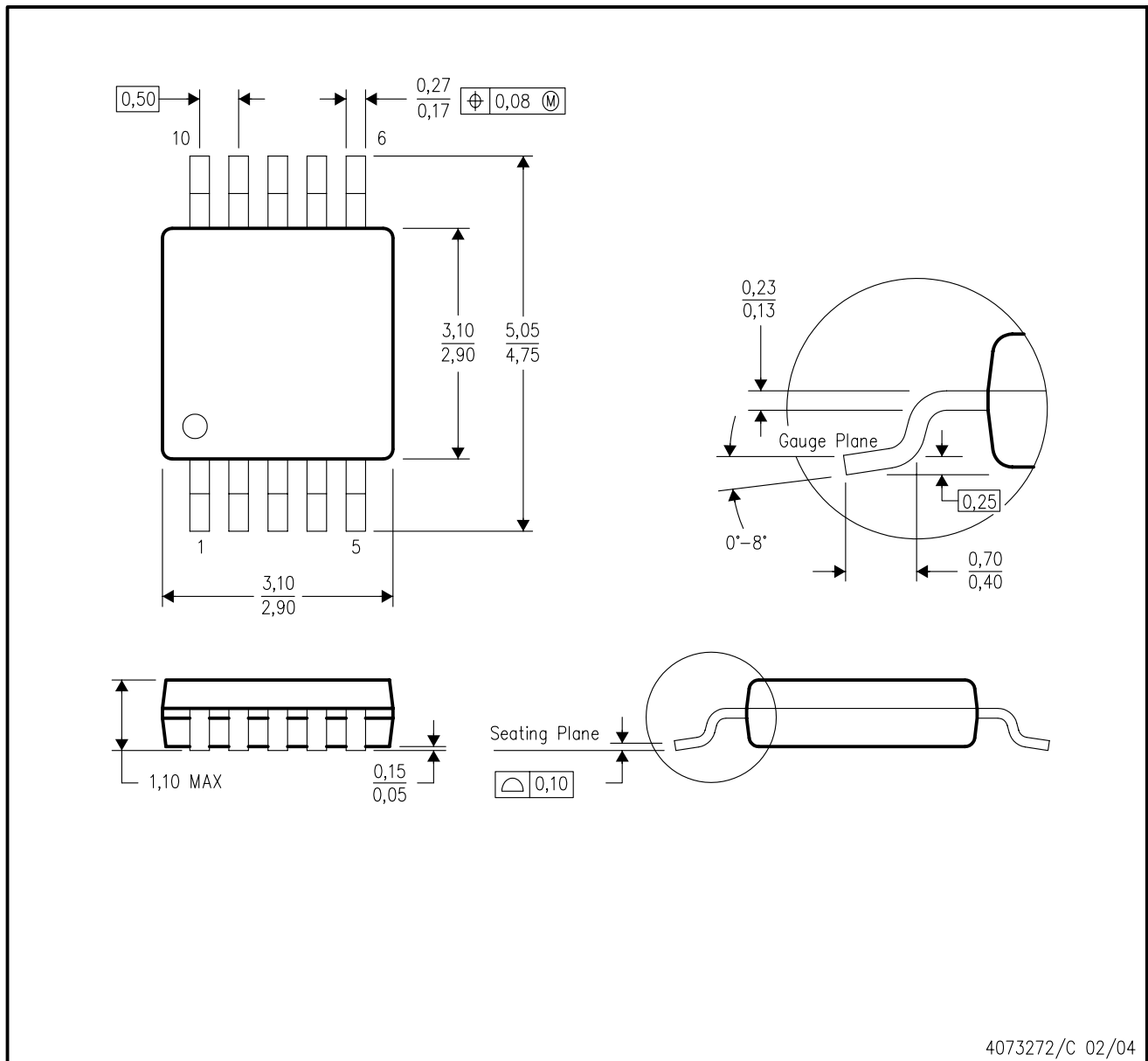
Exposed Thermal Pad Dimensions

4206565-8/Y 08/15

NOTE: A. All linear dimensions are in millimeters

DGS (S-PDSO-G10)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion.
  - D. Falls within JEDEC MO-187 variation BA.

## IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.