PROGRAMMABLE TOUCH SCREEN CONTROLLER WITH INTEGRATED STEREO AUDIO CODEC AND HEADPHONE/SPEAKER AMPLIFIER

FEATURES

- **Integrated Touch Screen Processor With Fully Automated Modes of Operation**
- **Programmable Converter Resolution, Speed, and Averaging**
- **Programmable Autonomous Timing Control**
- **Direct Battery Measurement Accepts up to 6-V Input**
- **On-Chip Temperature Measurement**
- **Stereo Audio DAC and Mono Audio ADC Support Rates up to 48 ksps**
- **High Quality 97-dB Stereo Audio**
- **Integrated PLL for Flexible Audio Clock Generation**
- **Programmable Digital Audio Bass/Treble/EQ/De-Emphasis**
- **On-Chip 325-mW, 8-Ω Speaker Driver**
- **Stereo Headphone Amplifier With Capless Output Option**
- **Microphone Preamp and Hardware Automatic Gain Control**
- **SPI™ and I²S™ Serial Interface**
- **Full Power-Down Control**
- **Low Power: 11-mW Stereo Audio Playback At 48 ksps**
- **32-Pin TSSOP and 32-Pin 5×5 mm QFN Package**

APPLICATIONS

- **Personal Digital Assistants**
- **Smart Cellular Phones**
- **MP3 Players**

DESCRIPTION

The TSC2100 is a highly integrated touch screen controller with on-chip processor and audio codec. The touch screen portion of the TSC2100 contains a 12-bit 4-wire resistive touch screen ADC complete with drivers, and interfaces to the host controller through a standard SPI™ serial interface. The on-chip processor provides extensive features specifically designed to reduce host processor and bus overhead, with capabilities that include fully automated operating modes, programmable conversion resolution up to 12 bits, programmable sampling rates up to 125 kHz, programmable conversion averaging, and programmable on-chip timing generation.

The TSC2100 includes a high-performance audio codec with 16/20/24/32-bit 97-dB stereo playback, mono record functionality at up to 48 ksps. A microphone input includes built-in preamp and hardware automatic gain control, with single-ended or fully-differential input capability. The dual output drivers on the TSC2100 can be programmed for low or high power drive for optimized power saving capability. The drivers can function as a stereo line-level output, a stereo headphone amplifier with capless or ac-coupled configurations, or a bridge-terminated speaker driver, delivering up to 325 mW into an 8-Ω load. A programmable digital audio effects processor enables bass, treble, midrange, or equalization playback processing. The digital audio data format is programmable to work with popular audio standard protocols (I²S, DSP, Left/Right Justified) in master or slave mode, and also includes an on-chip programmable PLL for flexible clock generation capability. Highly configurable software power control is provided, enabling stereo audio playback at 48 ksps at 11 mW with a 3.3-V analog supply level.

The TSC2100 offers a 12-bit measurement ADC and internal reference voltage, as well as two battery measurement inputs capable of reading battery voltages up to 6 V, while operating at an analog supply as low as 2.7 V. It includes an on-chip temperature sensor capable of reading 0.3°C resolution. The TSC2100 is available in a 32 lead TSSOP and a 32 lead QFN.

US Patent No. 624639

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

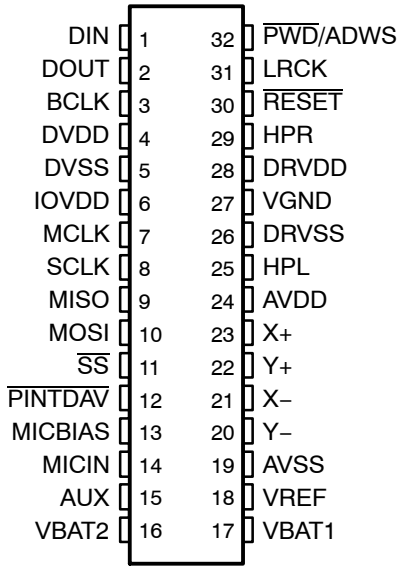
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

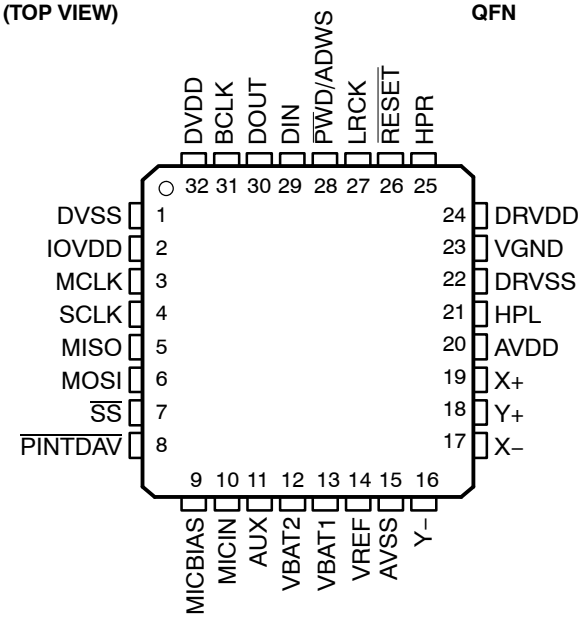
PRODUCT	PACKAGE	PACKAGE DESIGNATOR	OPERATING TEMPERATURE RANGE	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TSC2100IDA	TSSOP-32	DA	–40°C to 85°C	TSC2100IDA	Tubes, 46
				TSC2100IDAR	Tape and Reel, 2000
	QFN-32	RHB		TSC2100IRHB	Tubes, 52
				TSC2100IRHBR	Tape and Reel, 3000

PIN ASSIGNMENTS

(TOP VIEW) TSSOP



(TOP VIEW) QFN



Terminal Functions

QFN PIN	TSSOP PIN	NAME	DESCRIPTION	QFN PIN	TSSOP PIN	NAME	DESCRIPTION
29	1	DIN	Audio data input	13	17	VBAT1	Battery monitor input
30	2	DOUT	Audio data output	14	18	VREF	Reference voltage I/O
31	3	BCLK	Audio bit–clock	15	19	AVSS	Analog ground
32	4	DVDD	Digital core supply	16	20	Y–	Y– position input and driver
1	5	DVSS	Digital core and IO ground	17	21	X–	X– position input and driver
2	6	IOVDD	IO supply	18	22	Y+	Y+ position input and driver
3	7	MCLK	Master clock	19	23	X+	X+ position input and driver
4	8	SCLK	SPI serial clock input	20	24	AVDD	Analog power supply
5	9	MISO	SPI serial data output	21	25	HPL	Left channel audio output
6	10	MOSI	SPI serial data input	22	26	DRVSS	Speaker ground
7	11	$\overline{SS}$	SPI slave select input	23	27	VGND	Virtual ground for audio output
8	12	$\overline{PINTDAV}$	Pen interrupt/data available output	24	28	DRVDD	Speaker /PLL supply
9	13	MICBIAS	Microphone bias voltage	25	29	HPR	Right channel audio output
10	14	MICIN	Microphone input	26	30	$\overline{RESET}$	Device reset
11	15	AUX	Auxiliary input	27	31	LRCK	Audio DAC word-clock
12	16	VBAT2	Battery monitor input	28	32	$\overline{PWD}$/ADWS	Hardware powerdown/ADC word clock

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)(2)(3)

		UNITS
AVDD to AVSS		–0.3 V to 3.9 V
DRVDD to DRVSS		–0.3 V to 3.9 V
IOVDD to DVSS		–0.3 V to 3.9 V
DVDD to DVSS		–0.3 V to 2.5 V
AVDD to DRVDD		–0.1 V to 0.1 V
AVSS to DRVSS to DVSS		–0.1 V to 0.1 V
Analog inputs (except VBAT1 and VBAT2) to AVSS		–0.3 V to AVDD + 0.3 V
VBAT1 / VBAT2 to AVSS		–0.3 V to 6 V
Digital input voltage to DVSS		–0.3 V to IOVDD + 0.3 V
Operating temperature range		–40°C to 85°C
Storage temperature range		–65°C to 105°C
Junction temperature (T_J Max)		105°C
TSSOP package	Power dissipation	$(T_J \text{ Max} - T_A)/\theta_{JA}$
	θ_{JA} Thermal impedance	86°C/W
QFN package	Power dissipation	$(T_J \text{ Max} - T_A)/\theta_{JA}$
	θ_{JA} Thermal impedance	123°C/W
Lead temperature	Soldering vapor phase (60 sec)	215°C
	Infrared (15 sec)	220°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) If the TSC2100 QFN version is used to drive high power levels to an 8-Ω load for extended intervals at ambient temperatures above 70°C, multiple vias should be used to electrically and thermally connect the thermal pad on the QFN package to an internal heat-dissipating ground plane on the user’s PCB.

(3) The TSC2100 TSSOP version provides full output power into an 8-Ω load at ambient temperatures of 70°C and below. TI does not recommend using the TSC2100 TSSOP version to drive high power levels to an 8-Ω load for extended intervals at ambient temperatures above 70°C. All other device functionality, including driving of stereo 16-Ω loads at full volume, is supported up to 85°C.

ELECTRICAL CHARACTERISTICS

At +25°C, AVDD,DRVDD,IOVDD = 3.3 V, DVDD = 1.8 V, Int. V_{ref} = 2.5 V, Fs (Audio) = 48 kHz, unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TOUCH SCREEN					
AUXILIARY ANALOG INPUT					
Input voltage range	AUX selected as input to touch screen ADC	0		+VREF	V
Input capacitance			25		pF
Input leakage current			±1		µA
BATTERY MONITOR INPUTS					
Input voltage range		0.5		6.0	V
Input leakage current	Battery conversion not selected		±1		µA
TOUCH SCREEN A/D CONVERTER					
Resolution	Programmable: 8-, 10-,12-bits			12	Bits
No missing codes	12-bit resolution		11		Bits
Integral nonlinearity		–5		5	LSB
Offset error		–6		6	LSB
Gain error	Calculated with effect of internal reference variation removed.	–6		6	LSB
Noise			53		µVrms
AUDIO CODEC					
ADC DECIMATION FILTER	Sample rate of 48 ksps				
Filter gain from 0 to 0.39Fs			±0.1		dB
Filter gain at 0.4125Fs			–0.25		dB
Filter gain at 0.45Fs			–3		dB
Filter gain at 0.5Fs			–17.5		dB
Filter gain from 0.55Fs to 64Fs			–75		dB
Filter group delay			17/Fs		Sec
MICROPHONE INPUT TO ADC	1 kHz sine wave input, Fs = 48 ksps				
Full scale input voltage (0 dB)	By design, not tested in production		0.707		Vrms
Input common mode	By design, not tested in production		1.35		V
SNR	Measured as idle channel noise, 0-dB gain, A-weighted	80	92		dBA
THD	0.63-Vrms input, 0-dB gain		–89	–72	dB
PSRR	1 kHz, 100 mVpp on AVDD.(1)		57		dB
Mute attenuation	Output code with 0.63-Vrms sine wave input at 1 kHz		0000H		
Input resistance			20		kΩ
Input capacitance			10		pF
MICROPHONE BIAS					
Voltage	D4 = 0 control register 05H/Page2		2.5		V
	D4 = 1 control register 05H/Page2		2.0		V
Sourcing current			4.7		mA

(1) ADC PSRR measurement is calculated as:

$$PSRR = 20 \log_{10}\left(\frac{VSIG_{sup}}{V_{ADCOUT}}\right)$$

ELECTRICAL CHARACTERISTICS

At +25°C, AVDD,DRVDD,IOVDD = 3.3 V, DVDD = 1.8 V, Int. V_{ref} = 2.5 V, Fs (Audio) = 48 kHz, unless otherwise noted (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DAC INTERPOLATION FILTER					
Pass band		20		0.45Fs	Hz
Pass band ripple			±0.06		dB
Transition band		0.45Fs		0.5501Fs	Hz
Stop band		0.5501Fs		7.455Fs	Hz
Stop band attenuation			65		dB
Filter group delay			21/Fs		Sec
De–emphasis error			±0.1		dB
DAC LINE OUTPUT	1-kHz sine wave input, 48 ksps, output drivers in low power mode, load = 10 kΩ, 10 pF				
Full scale output voltage (0 dB)	By design, D10–D9 = *00* in control register 06H/Page2 corresponding to 2-V_{PP} output swing		0.707		Vrms
Output common mode	By design, D10–D9 = *00* in control register 06H/Page2 corresponding to 2-V_{PP} output swing		1.35		V
SNR	Measured as idle channel noise, A-weighted	85	97		dBA
THD	0-dB FS input, 0-dB gain		–95		dB
PSRR	1 kHz, 100mVpp on AVDD(2) VGND powered down		56		dB
Interchannel isolation	Coupling from ADC to DAC		84		dB
DAC HEADPHONE OUTPUT	1-kHz sine wave input, 48 ksps, output drivers in high power mode, load = 16 Ω, 10 pF				
Full scale output voltage (0 dB)	By design, D10–D9 = *00* in control register 06H/Page2 corresponding to 2-V_{PP} output swing		0.707		Vrms
SNR	Measured as idle channel noise, A-weighted	85	97		dBA
THD	–1 dBFS input, 0-dB gain		–91	–55	dB
PSRR	1 kHz, 100 mVpp on AVDD(1) VGND powered down		54		dB
Interchannel isolation	Coupling from ADC to DAC		85		dB
Mute attenuation			121		dB
Maximum output power	D10–D9 = *00* in control register 06H/Page2		30		mW
Digital volume control gain		–63.5		0	dB
Digital volume control step size			0.5		dB
Channel separation	Between HPL and HPR		80		dB
DAC SPEAKER OUTPUT	Output driver in high power mode, load = 8 Ω,, connected between HPR and HPL pins. D10–D9 = *10* in control register 06H/Page2 corresponding to 2.402-V_{PP} output swing				
Output power	0 dB input to DAC		325		mW
SNR	Measured as idle channel noise, A-weighted		102		dBA
THD	0 dBFS input, 0-dB gain		–33		dB
	–6 dBFS input, 0-dB gain		–88		dB

(1) DAC PSRR measurement is calculated as:

$$PSRR = 20 \log_{10}\left(\frac{VSIG_{sup}}{V_{HPR/L}}\right)$$

ELECTRICAL CHARACTERISTICS

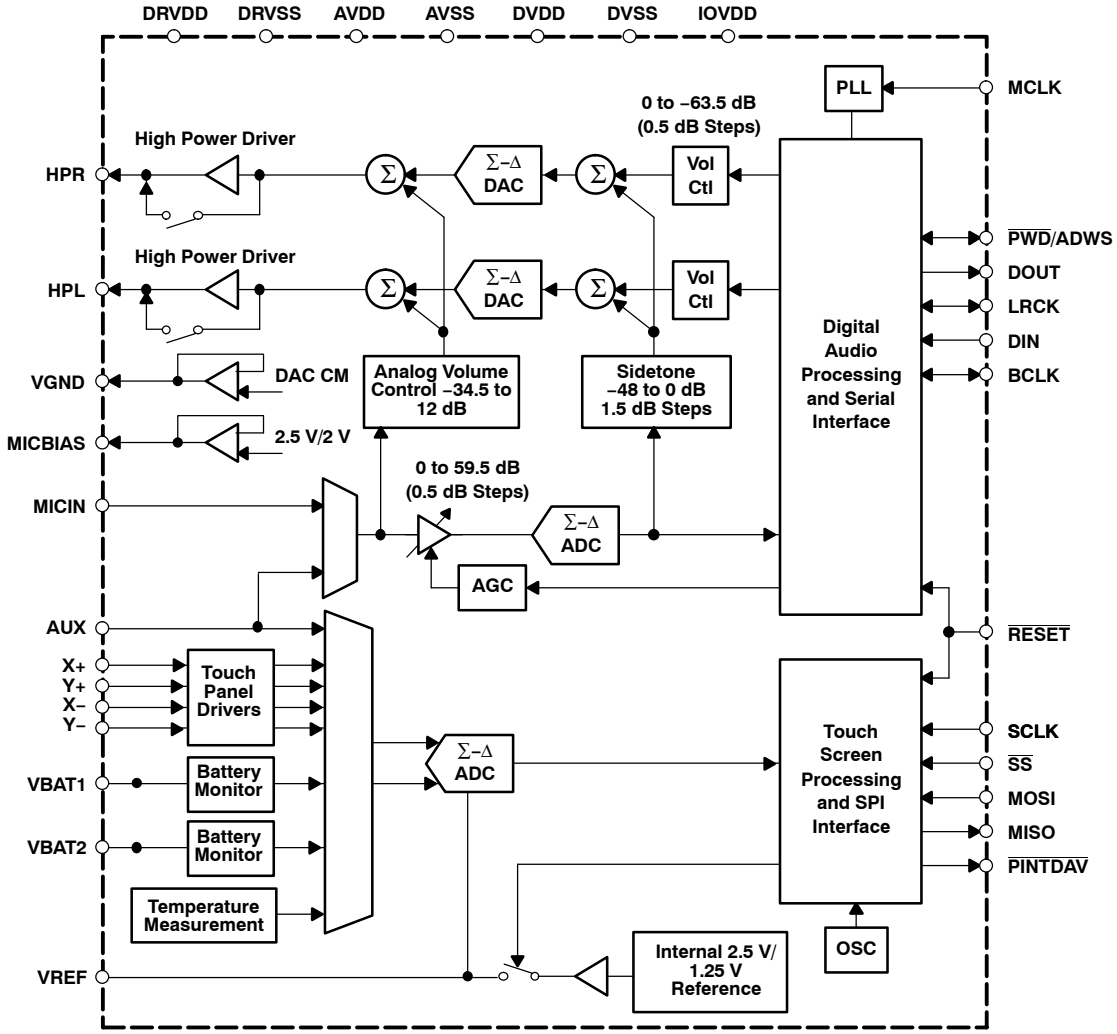
At +25°C, AVDD,DRVDD,IOVDD = 3.3 V, DVDD = 1.8 V, Int. V_{ref} = 2.5 V, Fs (Audio) = 48 kHz, unless otherwise noted (continued)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
VOLTAGE REFERENCE						
Voltage range	VREF output programmed as 2.5 V		2.3	2.5	2.7	V
	VREF output programmed as 1.25 V		1.15	1.25	1.35	
Voltage range	External VREF. By design, not tested in production.		1.2		2.55	V
Reference drift	Internal VREF = 1.25 V			29		ppm/°C
Current drain	Extra current drawn when the internal reference is turned on.			650		µA
DIGITAL INPUT / OUTPUT(1)						
Internal clock frequency				8.8		MHz
Logic family				CMOS		
Logic level: V_{IH}	I_{IH} = +5 µA		0.7xIOVDD			V
V_{IL}	I_{IL} = +5 µA		–0.3		0.3xIOVDD	V
V_{OH}	I_{OH} = 2 TTL loads		0.8xIOVDD			V
V_{OL}	I_{OL} = 2 TTL loads				0.1xIOVDD	V
Capacitive load				10		pF
POWER SUPPLY REQUIREMENTS						
Power supply voltage						
AVDD(2)			2.7		3.6	V
DRVDD(2)			2.7		3.6	V
IOVDD			1.1		3.6	V
DVDD			1.525		1.95	V
Touch-screen ADC quiescent current	IAVDD	Host controlled AUX conversion at 10 ksps with external reference.		47		µA
	IDRVDD			0		
	IDVDD			65		
Stereo audio playback	IAVDD	48 ksps, output drivers in low power mode, VGND off, PLL off		2.2		mA
	IDRVDD			0		
	IDVDD			2.4		
Microphone record	IAVDD	48 ksps, no playback, PLL off		2.9		mA
	IDRVDD			0		
	IDVDD			1.4		
PLL	IAVDD	Additional power consumed when PLL is enabled.		0.1		mA
	IDRVDD			1.3		
	IDVDD			0.9		
VGND	IAVDD	Additional power consumed when VGND is powered.		0.3		mA
	IDRVDD			0.9		
	IDVDD			0		
Hardware power down	All currents			2		µA

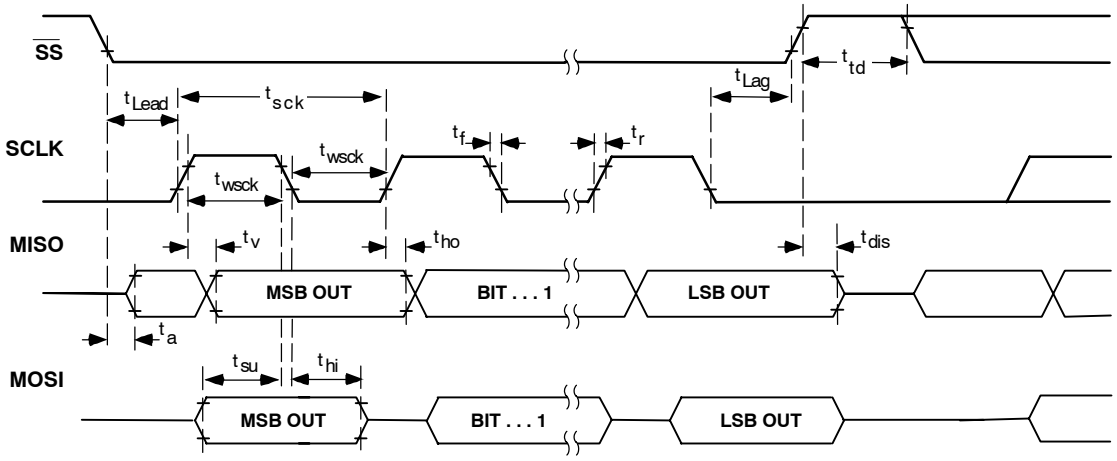
(1) Internal oscillator is designed to give nominally 8-MHz clock frequency. However, due to process variations, this frequency can vary from device to device. All calculations for delays and wait times in the data sheet assume an 8-MHz oscillator clock.

(2) It is recommended that AVDD and DRVDD be set to the same voltage for the best performance. It is also recommended that these supplies be separated on the user's PCB.

FUNCTIONAL BLOCK DIAGRAM



SPI TIMING DIAGRAM



TYPICAL TIMING REQUIREMENTS

All specifications at 25°C, DVDD = 1.8 V (1)

PARAMETER		IOVDD = 1.1 V		IOVDD = 3.3 V		UNITS
		MIN	MAX	MIN	MAX	
t_{wsck}	SCLK pulse width	27		18		ns
t_{Lead}	Enable lead time	18		15		ns
t_{Lag}	Enable lag time	18		15		ns
t_{td}	Sequential transfer delay	18		15		ns
t_a	Slave MISO access time		18		15	ns
t_{dis}	Slave MISO disable time		18		15	ns
t_{su}	MOSI data setup time	6		6		ns
t_{hi}	MOSI data hold time	6		6		ns
t_{ho}	MISO data hold time	4		4		ns
t_v	MISO data valid time		22		13	ns
t_r	Rise time		6		4	ns
t_f	Fall time		6		4	ns

(1) These parameters are based on characterization and are not tested in production.

AUDIO INTERFACE TIMING DIAGRAMS

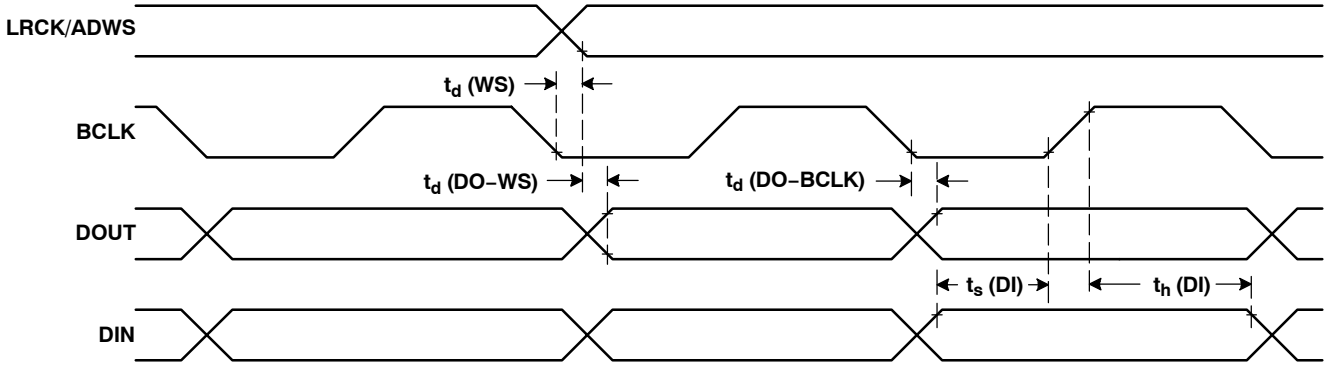


Figure 1. I2S/LJF/RJF Timing in Master Mode

TYPICAL TIMING REQUIREMENTS (FIGURE 1)

All specifications at 25°C, DVDD = 1.8 V (1)

PARAMETER		IOVDD = 1.1 V		IOVDD = 3.3 V		UNITS
		MIN	MAX	MIN	MAX	
t_d (WS)	ADWS/LRCK delay		25		15	ns
t_d (DO–WS)	ADWS to DOUT delay (for LJF mode)		25		15	ns
t_d (DO–BCLK)	BCLK to DOUT delay		25		15	ns
t_s(DI)	DIN setup	6		6		ns
t_h(DI)	DIN hold	6		6		ns
t_r	Rise time		10		6	ns
t_f	Fall time		10		6	ns

(1) These parameters are based on characterization and are not tested in production.

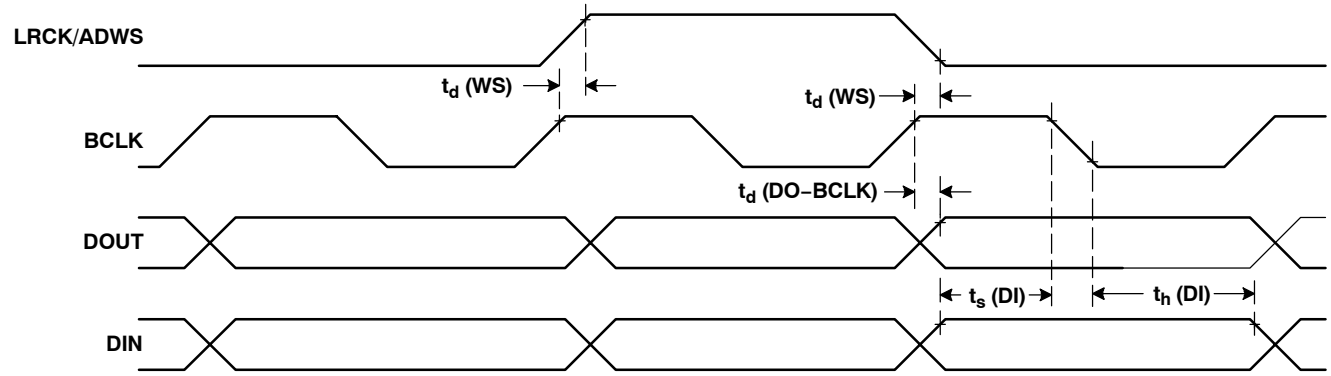


Figure 2. DSP Timing in Master Mode

TYPICAL TIMING REQUIREMENTS (FIGURE 2)

All specifications at 25°C, DVDD = 1.8 V(1)

PARAMETER		IOVDD = 1.1 V		IOVDD = 3.3 V		UNITS
		MIN	MAX	MIN	MAX	
t_d (WS)	ADWS/LRCK delay		25		15	ns
t_d (DO–BCLK)	BCLK to DOUT delay		25		15	ns
t_s(DI)	DIN setup	6		6		ns
t_h(DI)	DIN hold	6		6		ns
t_r	Rise time		10		6	ns
t_f	Fall time		10		6	ns

(1) These parameters are based on characterization and are not tested in production.

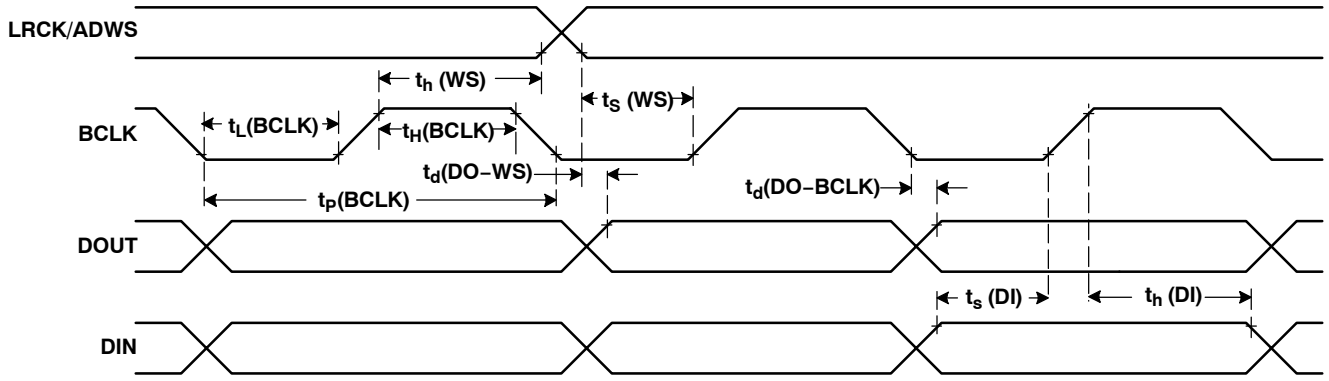


Figure 3. I2S/LJF/RJF Timing in Slave Mode

TYPICAL TIMING REQUIREMENTS (FIGURE 3)

All specifications at 25°C, DVDD = 1.8 V (1)

PARAMETER		IOVDD = 1.1 V		IOVDD = 3.3 V		UNITS
		MIN	MAX	MIN	MAX	
t_H (BCLK)	BCLK high period	35		35		ns
t_L (BCLK)	BCLK low period	35		35		ns
t_s(WS)	ADWS/LRCK setup	6		6		ns
t_h(WS)	ADWS/LRCK hold	6		6		ns
t_d (DO–WS)	ADWS to DOUT delay (for LJF mode)		25		18	ns
t_d (DO–BCLK)	BCLK to DOUT delay		25		15	ns
t_s(DI)	DIN setup	6		6		ns
t_h(DI)	DIN hold	6		6		ns
t_r	Rise time		5		4	ns
t_f	Fall time		5		4	ns

(1) These parameters are based on characterization and are not tested in production.

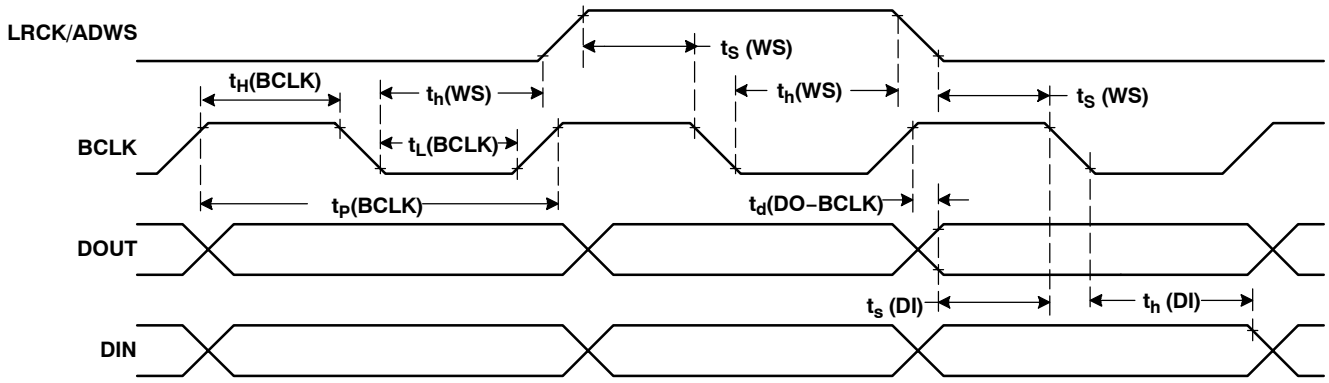


Figure 4. DSP Timing in Slave Mode

TYPICAL TIMING REQUIREMENTS (FIGURE 4)

All specifications at 25°C, DVDD = 1.8 V (1)

PARAMETER		IOVDD = 1.1 V		IOVDD = 3.3 V		UNITS
		MIN	MAX	MIN	MAX	
t_H (BCLK)	BCLK high period	35		35		ns
t_L (BCLK)	BCLK low period	35		35		ns
t_s(WS)	ADWS/LRCK setup	6		6		ns
t_h(WS)	ADWS/LRCK hold	6		6		ns
t_d (DO–BCLK)	BCLK to DOUT delay		25		15	ns
t_s(DI)	DIN setup	6		6		ns
t_h(DI)	DIN hold	6		6		ns
t_r	Rise time		5		4	ns
t_f	Fall time		5		4	ns

(1) These parameters are based on characterization and are not tested in production.

TYPICAL CHARACTERISTICS

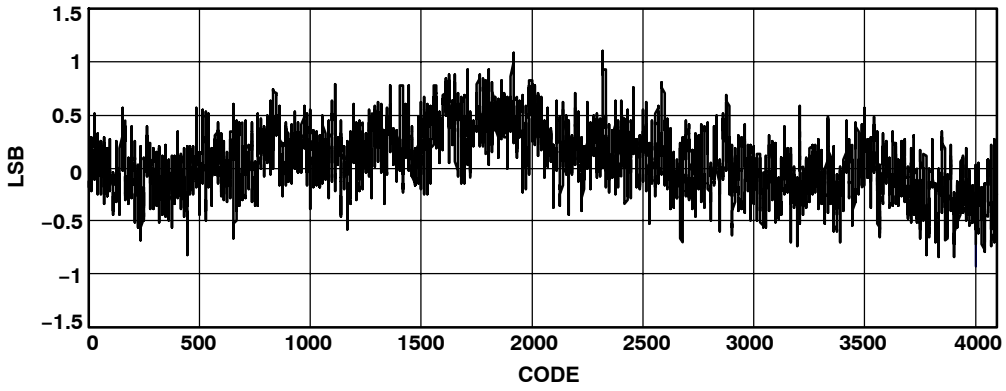


Figure 5. SAR INL (T_A = 25°C, Internal Ref = 2.5 V, 12 bit, AVDD = 3.3 V)

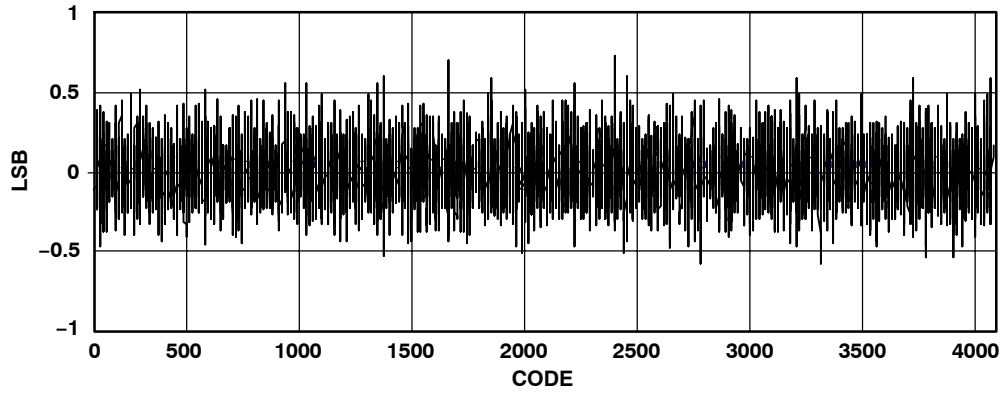


Figure 6. SAR DNL (T_A = 25°C, Internal Ref = 2.5 V, AVDD = 3.3 V)

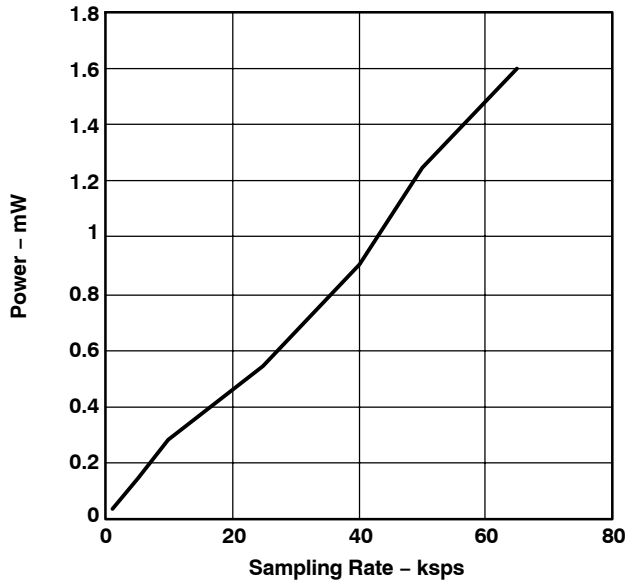


Figure 7. Touch Screen Power Consumption With Speed (T_A = 25°C, External Ref, Host Controlled AUX Conversion, AVDD = 3.3 V)

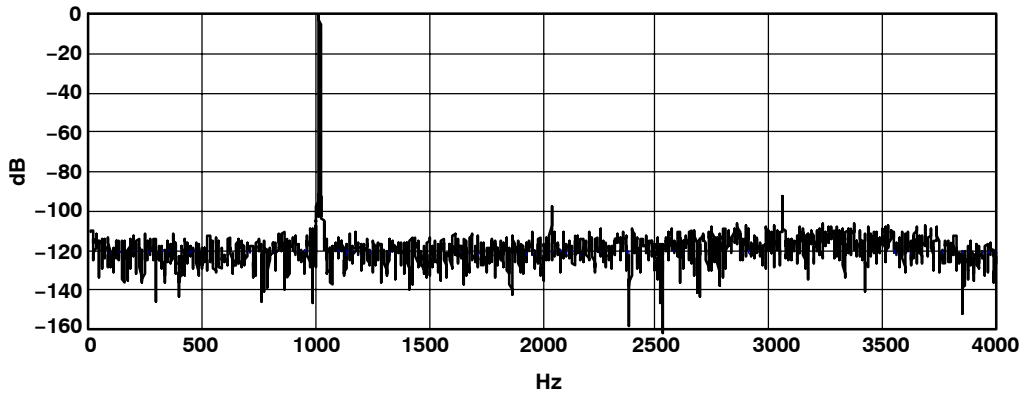


Figure 8. ADC FFT Plot at 8 ksps (T_A = 25°C, –1 dB, 1 kHz Input, AVDD = 3.3 V)

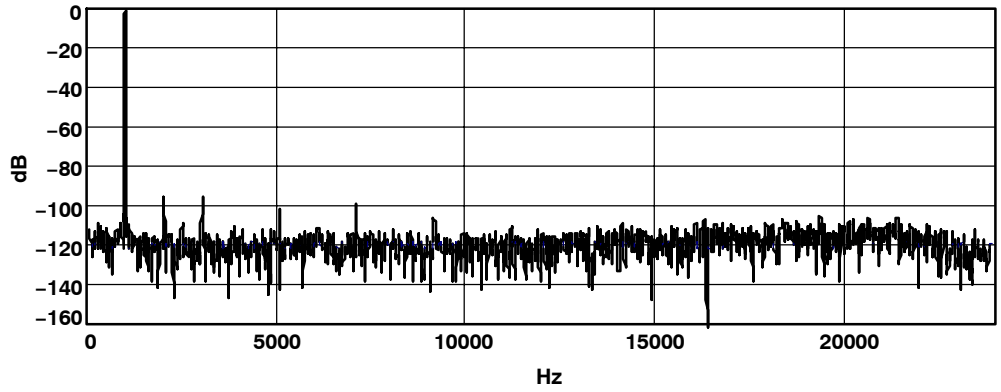


Figure 9. ADC FFT Plot at 48 ksps (T_A = 25°C, –1 dB, 1 kHz Input, AVDD = 3.3 V)

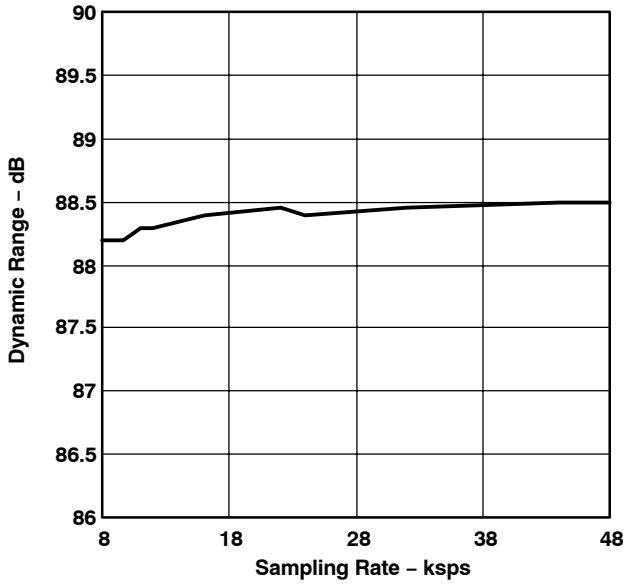


Figure 10. ADC Dynamic Range vs Sampling Speed (T_A = 25°C, AVDD = 3.3 V)

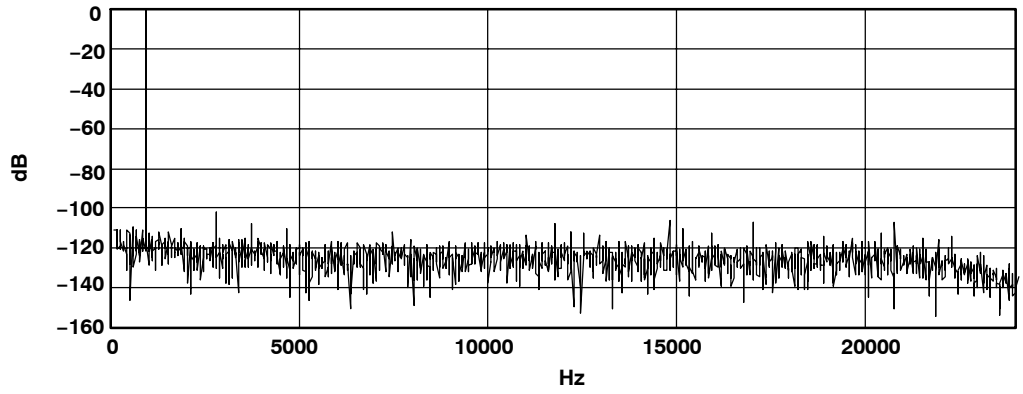


Figure 11. DAC FFT Plot (T_A = 25°C, 48 ksps, 0 dB, 1 kHz Input, AVDD = 3.3 V, R_L = 10 kΩ)

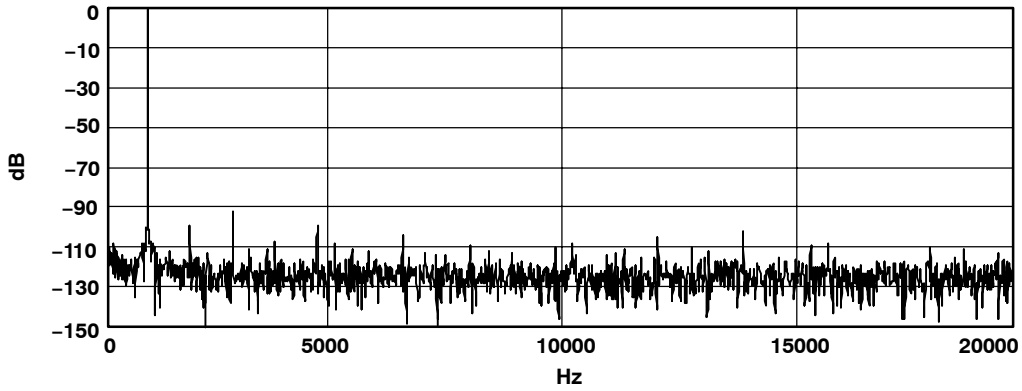


Figure 12. DAC FFT Plot (T_A = 25°C, 48 ksps, –1 dB, 1 kHz Input, AVDD = DRVDD = 3.3 V, DVDD = 1.8 V, R_L = 16 Ω)

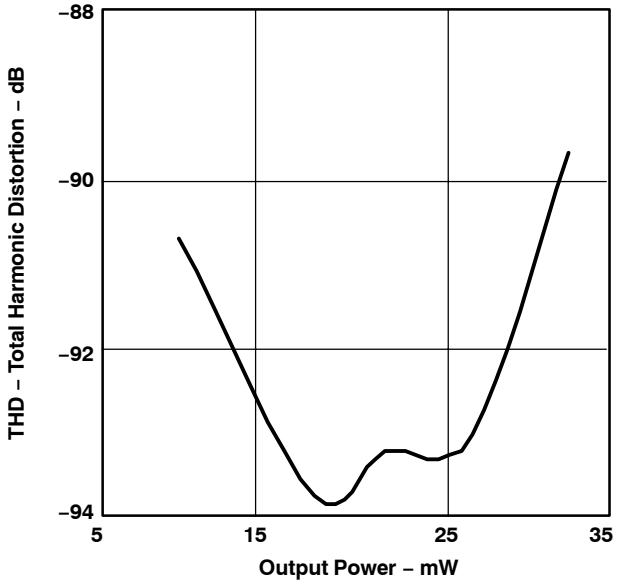


Figure 13. High Power Output Driver THD vs Output Power (T_A =25°C, AVDD, DRVDD = 3.3 V, R_L = 16 Ω)

OVERVIEW

The TSC2100 is a highly integrated touch screen controller with stereo audio codec for portable computing, communication, and entertainment applications. A register-based architecture eases integration with microprocessor-based systems through a standard SPI bus. All peripheral functions are controlled through the registers and onboard state machines.

The TSC2100 consists of the following blocks (refer to the block diagram):

- Touch Screen Interface
- Battery Monitors
- Auxiliary Inputs
- Temperature Monitor
- Audio Codec

Communication to the TSC2100 is via a standard SPI serial interface. This interface requires that the slave select signal be driven low to communicate with the TSC2100. Data is then shifted into or out of the TSC2100 under control of the host microprocessor, which also provides the serial data clock.

Control of the TSC2100 and its functions is accomplished by writing to different registers in the TSC2100. A simple command protocol is used to address the 16–bit registers. Registers control the operation of the A/D converter and audio codec.

A typical application of the TSC2100 is shown in Figure 14.

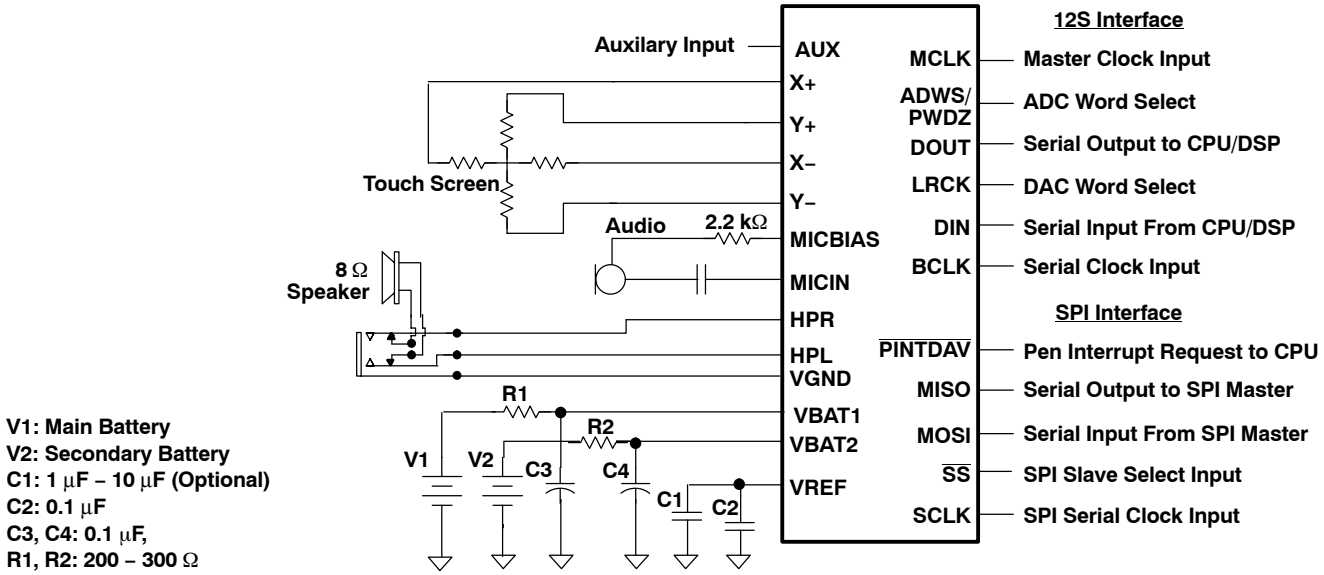


Figure 14. Typical Circuit Configuration

OPERATION—TOUCH SCREEN

A resistive touch screen works by applying a voltage across a resistor network and measuring the change in resistance at a given point on the matrix where a screen is touched by an input stylus, pen, or finger. The change in the resistance ratio marks the location on the touch screen.

The TSC2100 supports the resistive 4-wire configurations (see Figure 14). The circuit determines location in two coordinate pair dimensions, although a third dimension can be added for measuring pressure.

The 4-Wire Touch Screen Coordinate Pair Measurement

A 4-wire touch screen is constructed as shown in Figure 15. It consists of two transparent resistive layers separated by insulating spacers.

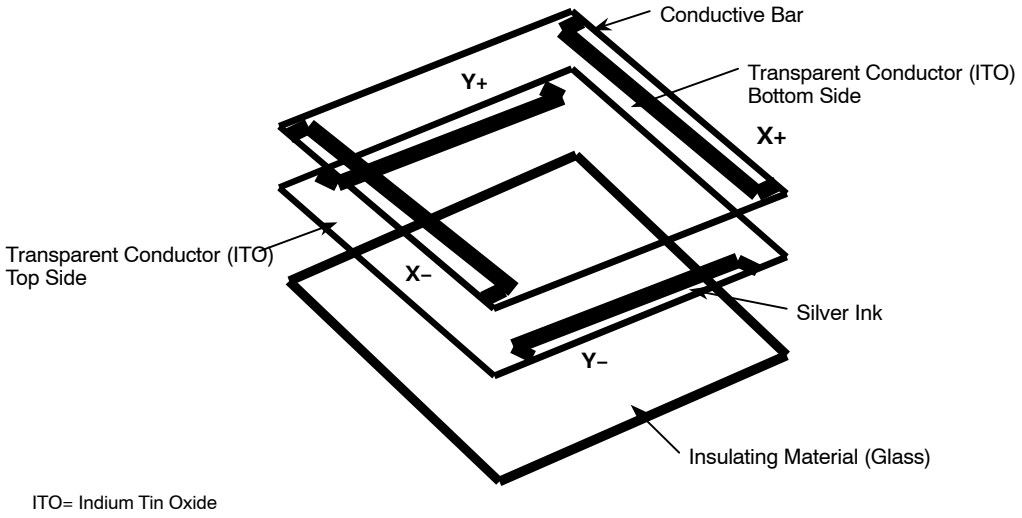


Figure 15. 4-Wire Touch Screen Construction

The 4-wire touch screen panel works by applying a voltage across the vertical or horizontal resistive network. The A/D converts the voltage measured at the point the panel is touched. A measurement of the Y position of the pointing device is made by connecting the X+ input to a A/D converter, turning on the Y drivers, and digitizing the voltage seen at the X+ input. The voltage measured is determined by the voltage divider developed at the point of touch. For this measurement, the horizontal panel resistance in the X+ lead does not affect the conversion due to the high input impedance of the A/D converter.

Voltage is then applied to the other axis, and the A/D converts the voltage representing the X position on the screen. This provides the X and Y coordinates to the associated processor.

Measuring touch pressure (Z) can also be done with the TSC2100. To determine pen or finger touch, the pressure of the *touch* needs to be determined. Generally, it is not necessary to have very high performance for this function; therefore, the 8-bit resolution mode is recommended (however, calculations are shown with the 12-bit resolution mode). There are several different ways of performing this measurement. The TSC2100 supports two methods. The first method requires knowing the X-plate resistance, measurement of the X-Position, and two additional cross panel measurements (Z_2 and Z_1) of the touch screen (see Figure 16). Using equation 1 calculates the touch resistance:

$$R_{TOUCH} = R_{X-plate} \times \frac{X-position}{4096} \left(\frac{Z_2}{Z_1} - 1 \right) \quad (1)$$

The second method requires knowing both the X-plate and Y-plate resistance, measurement of X-Position and Y-Position, and Z_1. Using equation 2 also calculates the touch resistance:

$$R_{TOUCH} = \frac{R_{X-plate} \times X-position}{4096} \left(\frac{4096}{Z_1} - 1 \right) - R_{Y-plate} \times \left(1 - \frac{Y-position}{4096} \right) \quad (2)$$

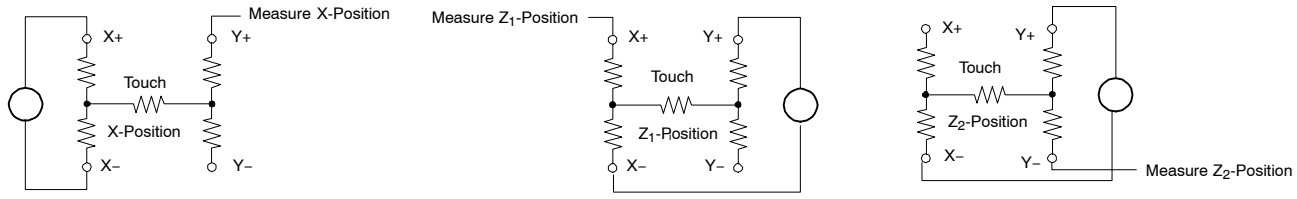


Figure 16. Pressure Measurement

When the touch panel is pressed or touched, and the drivers to the panel are turned on, the voltage across the touch panel often overshoots and then slowly settles (decays) to a stable dc value. This is due to mechanical bouncing which is caused by vibration of the top layer sheet of the touch panel when the panel is pressed. This settling time must be accounted for, or else the converted value is in error. Therefore, a delay must be introduced between the time the driver for a particular measurement is turned on, and the time measurement is made.

In some applications, external capacitors may be required across the touch screen for filtering noise picked up by the touch screen, i.e. noise generated by the LCD panel or back-light circuitry. The value of these capacitors provides a low-pass filter to reduce the noise, but causes an additional settling time requirement when the panel is touched.

Several solutions to this problem are available in the TSC2100. A programmable delay time is available which sets the delay between turning the drivers on and making a conversion. This is referred to as the panel voltage stabilization time, and is used in some of the modes available in the TSC2100. In other modes, the TSC2100 can be programmed to turn on the drivers only without performing a conversion. Time can then be allowed before the command is issued to perform a conversion.

The TSC2100 touch screen interface can measure position (X, Y) and pressure (Z). Determination of these coordinates is possible under three different modes of the A/D converter: (1) conversion controlled by the TSC2100, initiated by detection of a touch; (2) conversion controlled by the TSC2100, initiated by the host responding to the $\overline{\text{PINTDAV}}$ signal; or (3) conversion completely controlled by the host processor.

Touch Screen A/D Converter

The analog inputs of the TSC2100 are shown in Figure 17. The analog inputs (X, Y, and Z touch panel coordinates, battery voltage monitors, chip temperature and auxiliary input) are provided via a multiplexer to the successive approximation register (SAR) analog-to-digital (A/D) converter. The A/D architecture is based on a capacitive redistribution architecture, which inherently includes a sample/hold function.

A unique configuration of low on-resistance switches allows an unselected A/D input channel to provide power and an accompanying pin to provide ground for driving the touch panel. By maintaining a differential input to the converter and a differential reference input architecture, it is possible to negate errors caused by the driver switch on-resistances.

The A/D is controlled by an A/D converter control register. Several modes of operation are possible, depending upon the bits set in the control register. Channel selection, scan operation, averaging, resolution, and conversion rate may all be programmed through this register. These modes are outlined in the sections below for each type of analog input. The results of conversions made are stored in the appropriate result register.

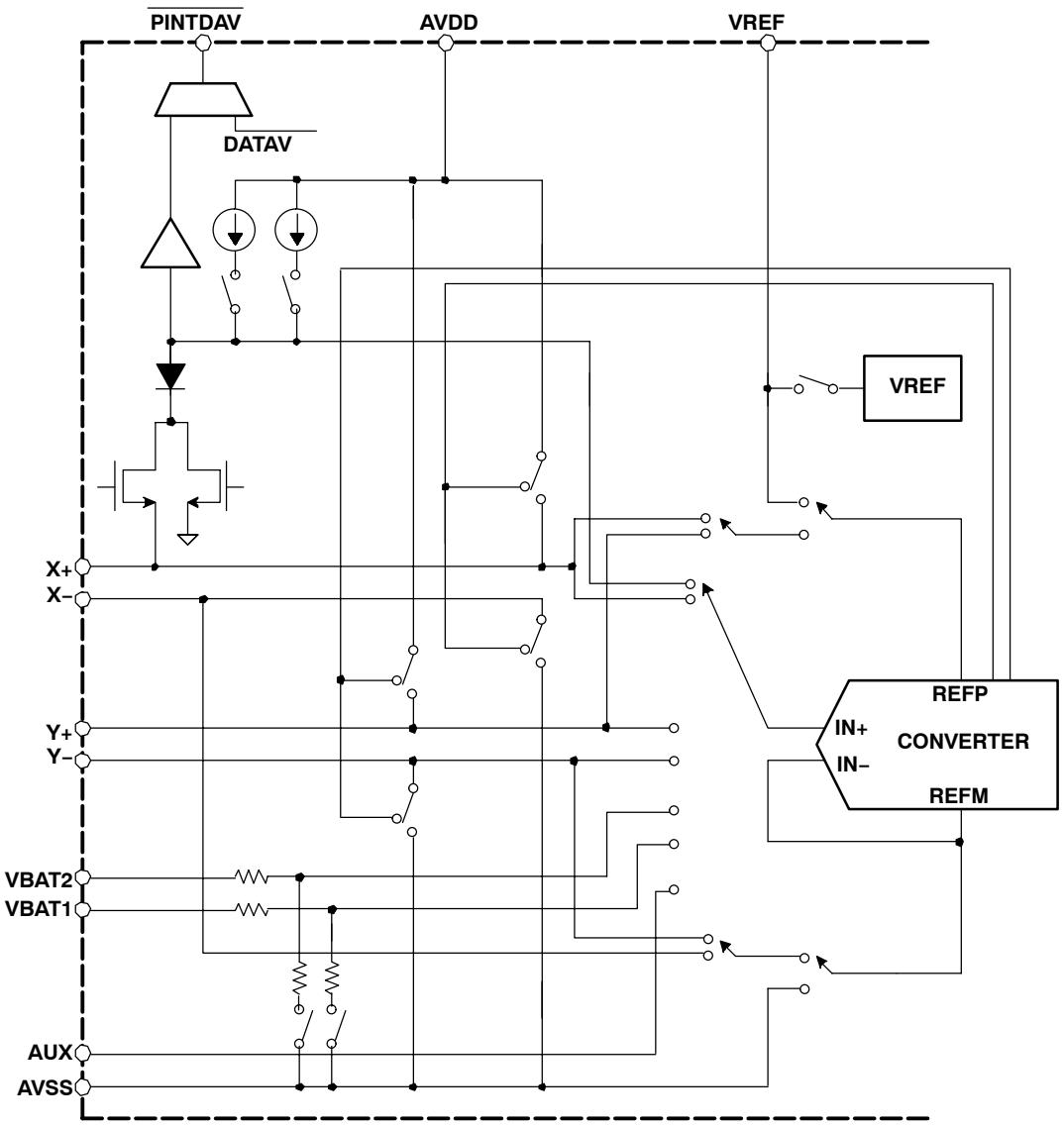


Figure 17. Simplified Diagram of the Analog Input Section

Data Format

The TSC2100 output data is in unsigned binary format and can be read from the registers over the SPI interface.

Reference

The TSC2100 has an internal voltage reference that can be set to 1.25 V or 2.5 V,through the reference control register.

The internal reference voltage should only be used in the single-ended mode for battery monitoring, temperature measurement, and for measuring the auxiliary inputs. Optimal touch screen performance is achieved when using a ratiometric conversion, thus all touch screen measurements are done automatically in the ratiometric mode.

An external reference can also be applied to the VREF pin, and the internal reference can be turned off.

Variable Resolution

The TSC2100 provides three different resolutions for the A/D converter: 8-, 10- or 12-bits. Lower resolutions are often practical for measurements such as touch pressure. Performing the conversions at lower resolution reduces the amount of time it takes for the A/D converter to complete its conversion process, which lowers power consumption.

Conversion Clock and Conversion Time

The TSC2100 contains an internal 8-MHz clock, which is used to drive the state machines inside the device that perform the many functions of the part. This clock is divided down to provide a clock to run the A/D converter. The division ratio for this clock is set in the A/D converter control register. The ability to change the conversion clock rate allows the user to choose the optimal value for resolution, speed, and power. If the 8-MHz clock is used directly, the A/D converter is limited to 8-bit resolution; using higher resolutions at this speed may not result in accurate conversions. Using a 4-MHz conversion clock is suitable for 10-bit resolution; 12-bit resolution requires that the conversion clock run at 1 or 2 MHz.

Regardless of the conversion clock speed, the internal clock runs nominally at 8 MHz. The conversion time of the TSC2100 is dependent upon several functions (see the section *Touch Screen Conversion Initiated at Touch Detect* in this data sheet). While the conversion clock speed plays an important role in the time it takes for a conversion to complete, a certain number of internal clock cycles is needed for proper sampling of the signal. Moreover, additional times, such as the panel voltage stabilization time, can add significantly to the time it takes to perform a conversion. Conversion time can vary depending upon the mode in which the TSC2100 is used. Throughout this data sheet, internal and conversion clock cycles are used to describe the times that many functions take to execute. Considering the total system design, these times must be taken into account by the user.

When both the audio ADC and DAC are powered down, the touch screen A/D uses an internal oscillator for conversions. However, to save power whenever audio ADC or DAC are powered up, the internal oscillator is powered down and MCLK and BCLK are used to clock the touch screen A/D.

The TSC2100 uses the programmed value of Page2, Reg 06H D13 and the PLL programmability to derive a clock from MCLK. The various combinations are listed in Table 1.

Table 1. Conversion Clock Frequency

	Page2, Reg 06H, D13 = 0	Page2, Reg 06H, D13 = 1
PLL enabled	$\frac{MCLK \times K \times 13}{P \times 160}$	$\frac{MCLK \times K \times 17}{P \times 192}$
PLL disabled	$\frac{MCLK \times 13}{Q \times 10}$	$\frac{MCLK \times 17}{Q \times 12}$

Touch Detect/Data Available

The pen interrupt/data available ($\overline{\text{PINTDAV}}$) output function is detailed in Figure 18. While in the power-down mode, the Y– driver is ON and connected to AVSS and the X+ pin is connected through an on-chip pullup resistor to AVDD. In this mode, the X+ pin is also connected to a digital buffer and mux to drive the $\overline{\text{PINTDAV}}$ output. When the panel is touched, the X+ input is pulled to ground through the touch screen, and the pen–interrupt signal goes LOW due to the current path through the panel to AVSS, initiating an interrupt to the processor. During the measurement cycles for X– and Y– position, the X+ input is disconnected from the pen-interrupt circuit to prevent any leakage current from the pullup resistor flowing through the touch screen, and thus causing conversion errors.

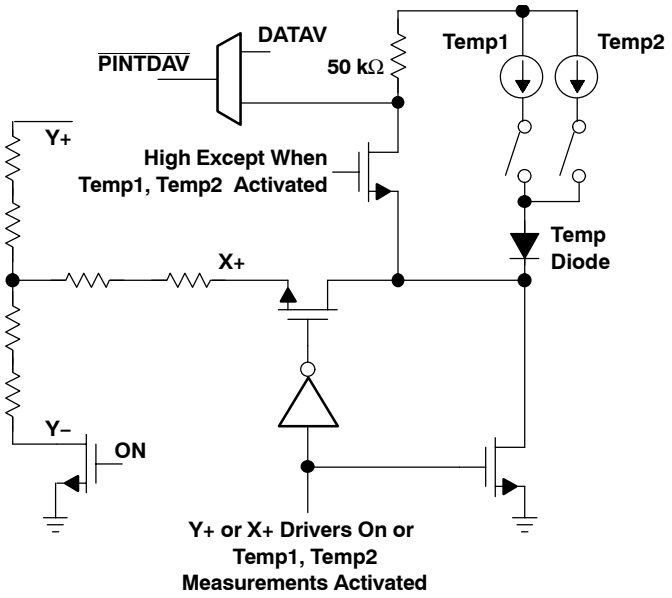


Figure 18. $\overline{\text{PINTDAV}}$ Functional Block Diagram

In modes where the TSC2100 needs to detect if the screen is still touched (for example, when doing a $\overline{\text{PINTDAV}}$ initiated X, Y, and Z conversion), the TSC2100 must reset the drivers so that the 50-kΩ resistor is connected. Because of the high value of this pullup resistor, any capacitance on the touch screen inputs causes a long delay time, and may prevent the detection from occurring correctly. To prevent this, the TSC2100 has a circuit that allows any screen capacitance to be *precharged*, so that the pullup resistor does not have to be the only source for the charging current. The time allowed for this precharge, as well as the time needed to sense if the screen is still touched, can be set in the configuration control register D5–D0 of REG05H/Page1.

This does point out, however, the need to use the minimum capacitor values possible on the touch screen inputs. These capacitors may be needed to reduce noise, but too large a value increases the needed precharge and sense times, as well as panel voltage stabilization time.

The function of $\overline{\text{PINTDAV}}$ output is programmable and controlled by writing to the bits D15–D14 of REG 01H/Page1 as described in the Table 2.

Table 2. Programmable $\overline{\text{PINTDAV}}$ Functionality

D15–D14	$\overline{\text{PINTDAV}}$ FUNCTION
00	Acts as PEN interrupt (active low) only. When PEN touch is detected, $\overline{\text{PINTDAV}}$ goes low.
01	Acts as data available (active low) only. The $\overline{\text{PINTDAV}}$ goes low as soon as one set of ADC conversions are completed for data of X,Y, XYZ, battery input, or auxiliary input selected by D13–D10 in REG00H/Page1. The resulting A/D output is stored in the appropriate registers. The $\overline{\text{PINTDAV}}$ remains low and goes high only after this complete set of registers selected by D13–D10 REG00H/Page1 is read out.
10 11	Acts as both PEN interrupt and data available. When PEN touch is detected, $\overline{\text{PINTDAV}}$ goes low and remains low. The $\overline{\text{PINTDAV}}$ goes high only after one set of A/D conversions is completed for data of X,Y, XYZ, battery input, or auxiliary input selected by D13–D10 in REG00H/Page1.

NOTE: See the section Conversion Time Calculation for the TSC2100 in this data sheet for the timing diagrams.

Pen-touch detect circuit is disabled during hardware power down.

Touch Screen Measurements

The touch screen ADC can be controlled by the host processor or can be self–controlled to offload processing from the host processor. Bit D15 of REG00H/Page1 sets the control mode of the TSC2100 touch screen ADC.

Conversion Controlled by TSC2100 Initiated at Touch Detect

In this mode, the TSC2100 detects when the touch panel is touched and causes the $\overline{\text{PINTDAV}}$ line to go low. At the same time, the TSC2100 starts up its internal clock. Assuming the part was configured to convert XY coordinates, it then turns on the Y drivers, and after a programmed panel voltage stabilization time, powers up the ADC and converts the Y coordinate. If averaging is selected, several conversions may take place; when data averaging is complete, the Y coordinate result is stored in the Y register.

If the screen is still touched at this time, the X drivers are enabled, and the process repeats, but measuring instead the X coordinate, storing the result in the X register.

If only X and Y coordinates are to be measured, then the conversion process is complete. The time it takes to complete this process depends upon the selected resolution, internal conversion clock rate, averaging selected, panel voltage stabilization time, and precharge and sense times.

If the pressure of the touch is also to be measured, the process continues in the same way, measuring the Z1 and Z2 values, and placing them in the Z1 and Z2 registers. As before, this process time depends upon the settings described above.

See the section *Conversion Time Calculation for the TSC2100* in this data sheet for timing diagrams and conversion time calculations.

Conversion Controlled by TSC2100 Initiated by the Host

In this mode, the TSC2100 detects when the touch panel is touched and causes the pen-interrupt signal line to go low. The host recognizes the interrupt request, and then writes to the ADC control register (D13–D10 REG00H/Page1) to select one of the touch screen scan functions. The host can either choose to initiate one of the scan functions, in which case the TSC2100 controls the driver turnons, and wait times (e.g. upon receiving the interrupt the host can initiate the continuous scan function X–Y–Z1–Z2 after which the TSC2100 controls the rest of conversion). The host can also choose to control each aspect of conversion by controlling the driver turnons and start of conversions. For example, upon receiving the interrupt request, the host turns on the X drivers. After waiting for the settling time, the host then addresses the TSC2100 again, this time requesting an X coordinate conversion, and so on.

The main difference between this mode and the previous mode is that the host, not the TSC2100, controls the touch screen scan functions.

See the section *Conversion Time Calculation for the TSC2100* in this data sheet for timing diagrams and conversion time calculations.

Temperature Measurement

In some applications, such as battery recharging, a measurement of ambient temperature is required. The temperature measurement technique used in the TSC2100 relies on the characteristics of a semiconductor junction operating at a fixed current level. The forward diode voltage (V_{BE}) has a well-defined characteristic versus temperature. The ambient temperature can be predicted in applications by knowing the 25°C value of the V_{BE} voltage and then monitoring the delta of that voltage as the temperature changes.

The TSC2100 offers two modes of temperature measurement. The first mode requires a single reading to predict the ambient temperature. A diode, as shown in Figure 19, is used during this measurement cycle. This voltage is typically 600 mV at 25°C with a 20-μA current through it. The absolute value of this diode voltage can vary a few millivolts. During the final test of the end product, the diode voltage must be stored at a known temperature. Further calibration can be done to calculate the precise temperature coefficient of the particular device. This method has a temperature resolution of approximately 0.3 °C/LSB and accuracy of approximately 1°C.

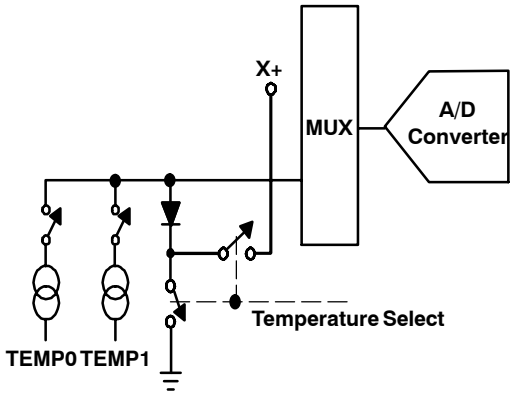


Figure 19. Functional Block Diagram of Temperature Measurement Mode

The second mode uses a two-measurement (differential) method. This mode requires a second conversion with a current 82 times larger. The voltage difference between the first (TEMP1) and second (TEMP2) conversion, using 82 times the bias current, is represented by:

$$\left(\frac{kT}{q}\right) \times \ln(N)$$

where:

N is the current ratio = 82

k = Boltzmann's constant ($1.38054 \bullet 10^{-23}$ electrons volts/degrees Kelvin)

q = the electron charge ($1.602189 \bullet 10^{-19}$ °C)

T = the temperature in degrees Kelvin

This method provides resolution of approximately 1.5°C/LSB and accuracy of approximately 1°C. The equation for the relation between differential code and temperature may vary slightly from device to device and can be calibrated at final system test by the user.

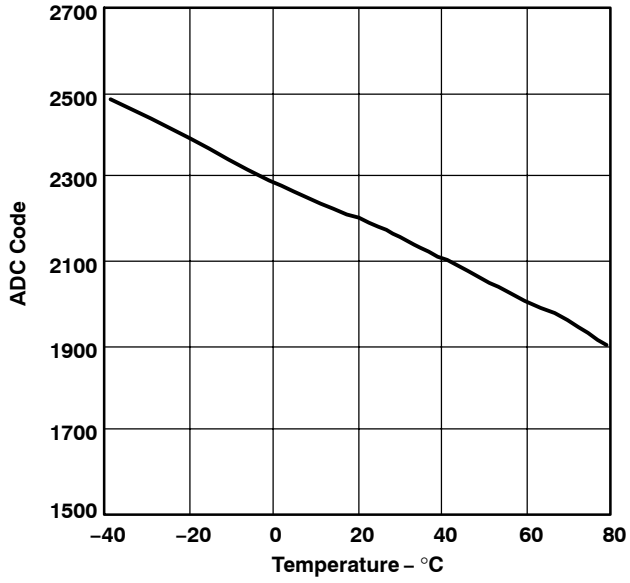


Figure 20. Typical Plot for Single Measurement Method

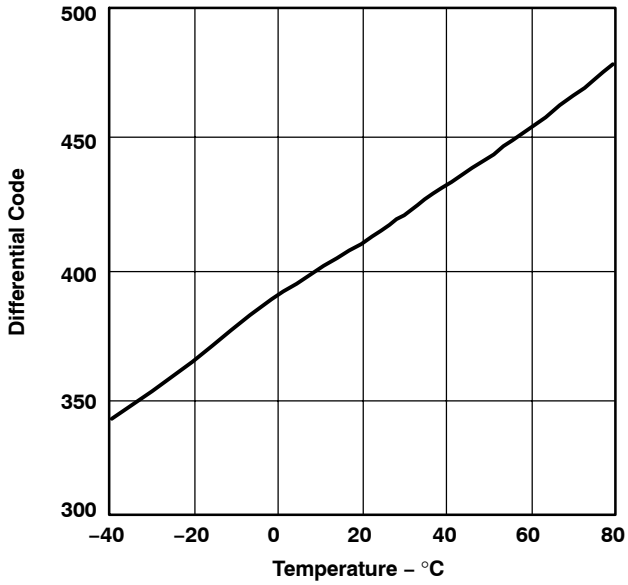


Figure 21. Typical Plot for Differential Measurement Method

Temperature measurement can only be done in host controlled mode.

Battery Measurement

An added feature of the TSC2100 is the ability to monitor the battery voltage on the other side of a voltage regulator (dc/dc converter), as shown in Figure 22. The battery voltage can vary from 0.5 V to 6 V while maintaining the analog supply voltage to the TSC2100 in the range of 2.7 V to 3.6 V. The input voltage (VBAT1 or VBAT2) is divided down by a factor of 6 so that a 6.0-V battery voltage is represented as 1.0 V to the ADC. In order to minimize the power consumption, the divider is only on during the sampling of the battery input. If the battery conversion results in a ADC output code of B, the voltage at the battery pin can be calculated as

Vbat = (B/2^N)*6*Vref

where N is the programmed resolution of ADC and Vref the programmed value of internal reference or the applied external reference.

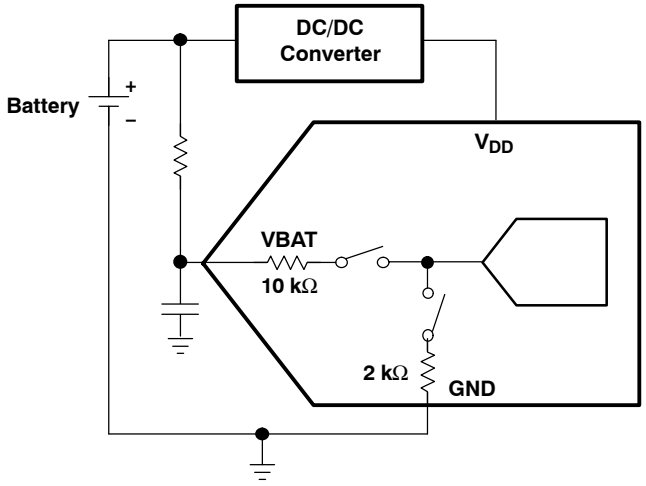


Figure 22. Battery Measurement Functional Block Diagram

For increased protection and robustness, TI recommends a minimum 100 Ω resistor be added in series between the system battery and the VBAT pin. The 100 Ω resistor will cause an approximately 1% gain change in the battery voltage measurement, which can easily be corrected in software when the battery conversion data is read by the operating system.

Battery measurement can only be done in host controlled mode.

See the section *Conversion Time Calculation for the TSC2100* and subsection *Non Touch Measurement Operation* in this data sheet for timing diagrams and conversion time calculations.

Auxiliary Measurement

The auxiliary voltage input (AUX) can be measured in much the same way as the battery inputs. Applications might include external temperature sensing, ambient light monitoring for controlling the back-light, or sensing the current drawn from the battery. The auxiliary input can also be monitored continuously in scan mode.

Auxiliary measurement can only be done in host controlled mode.

See the section *Conversion Time Calculation for the TSC2100* and subsection *Non Touch Measurement Operation* in this data sheet for timing diagrams and conversion time calculations.

Port Scan

If making measurements of BAT1, BAT2, and AUX is desired on a periodic basis, the port scan mode can be used. This mode causes the TSC2100 to sample and convert both battery inputs and the auxiliary input. At the end of this cycle, the battery and auxiliary result registers contain the updated values. Thus, with one write to the TSC2100, the host can cause three different measurements to be made.

Port scan can only be done in host–controlled mode.

See the section *Conversion Time Calculation for the TSC2100* and subsection *Port Scan Operation* in this data sheet for timing diagrams and conversion time calculations.

Hardware Reset

The device requires hardware reset (active low) pulse after power up for correct operation. A hardware reset pulse initializes all the internal registers, counters and logic.

Hardware Power Down

By default the $\overline{\text{PWD}}$/ADWS pin is configured as a hardware power down (active low) signal. The device powers down all the internal circuitry to save power. All the register contents are maintained. Some counters maintain their value. The user can optionally use this pin as ADWS (ADC word select) by register programming. Putting the TSC2100 into hardware power-down mode also disables the pen-touch detect circuit.

OPERATION–AUDIO CODEC

Audio Analog I/O

The TSC2100 has one mono audio input (MICIN) typically used for microphone recording, and an auxiliary input (AUX) that can be used as a second microphone or line input. The dual audio output drivers have programmable power level and can be configured to drive up to 325 mW into an 8-Ω speaker, or to drive 16-Ω stereo headphones at over 30-mW per channel, or to provide a stereo line-level output. The power level of the output drivers is controlled using BIT–D12 in control register REG–05H/Page2. The TSC2100 also has a virtual ground (VGND) output driver, which can optionally be used to connect the return terminal of headphones, to eliminate the ac-coupling capacitors needed at the headphone output. The VGND amplifier is controlled by BIT-D8 of REG–05H/Page2. A special circuit has also been included in the TSC2100 to insert a short keyclick sound into the stereo audio output, even when the audio DAC is powered down. The keyclick sound is used to provide feedback to the user when a particular button is pressed or item is selected. The specific sound of the keyclick can be adjusted by varying several register bits that control its frequency, duration, and amplitude.

Audio Digital Interface

Digital audio data samples are transmitted between the TSC2100 and the CPU via the serial bus (BCLK, ADWS, DOUT, LRCK, DIN) that can be configured to transfer digital data in four different formats: right justified, left justified, I2S, and DSP. The four modes are MSB-first and operate with variable word length of 16, 20, 24, or 32 bits. The digital audio serial bus of the TSC2100 can operate in master or slave mode, depending on its register settings. The word-select signals (ADWS, LRCK) and bit clock signal (BCLK) are configured as outputs when the bus is in master mode. They are configured as inputs when the bus is in slave mode. The ADWS is representative of the sampling rate of the audio ADC and is synchronized with DOUT. The LRCK is representative of the audio DAC sampling rate and is synchronized with DIN. Although the DOUT signal can contain two channels of information (a left and right channel), the TSC2100 sends the same ADC data in both channels.

- **ADC/DAC SAMPLING RATE**

  The Audio Control 1 register (Register 00H, Page2) determines the sampling rates of the audio DAC and ADC, which are scaled down from a reference rate (Fsref). The ADC and DAC can operate with either a common LRCK (equal sampling rates) or separate ADWS and LRCK (unequal sampling rates). When the audio codec is powered up, it is by default configured as an I^2S slave with both the DAC and ADC operating at Fsref.

- **WORD SELECT SIGNALS**

  The word select signal (LRCK, ADWS) indicates the channel being transmitted:

  – LRCK/ADWS = 0: left channel for I2S mode

  – LRCK/ADWS = 1: right channel for I2S mode

  For other modes see the timing diagrams below.

Bitclock (BCLK) Signal

In addition to flexibility as master or slave mode, the BCLK can also be configured in two transfer modes—256–S and Continuous Transfer Modes, which are described below. These modes are set using BIT–D12/REG–06h/Page2.

- **256–S TRANSFER MODE**

  In the 256–S mode, the BCLK rate always equals 256 times the maximum of the LRCK and ADWS frequencies. In the 256–S mode, the combination of 48 ksps sampling rate (as selected by BIT–D13/REG–06h/Page2) and left–justified mode is not supported.

- **CONTINUOUS TRANSFER MODE**

  In the continuous transfer mode, the BCLK rate always equals two times the word length of the maximum of the LRCK and ADWS frequencies.

- **RIGHT-JUSTIFIED MODE**

  In right-justified mode, the LSB of the left channel is valid on the rising edge of the BCLK preceding the falling edge of ADWS or LRCK. Similarly the LSB of the right channel is valid on the rising edge of the BCLK preceding the rising edge of ADWS or LRCK.

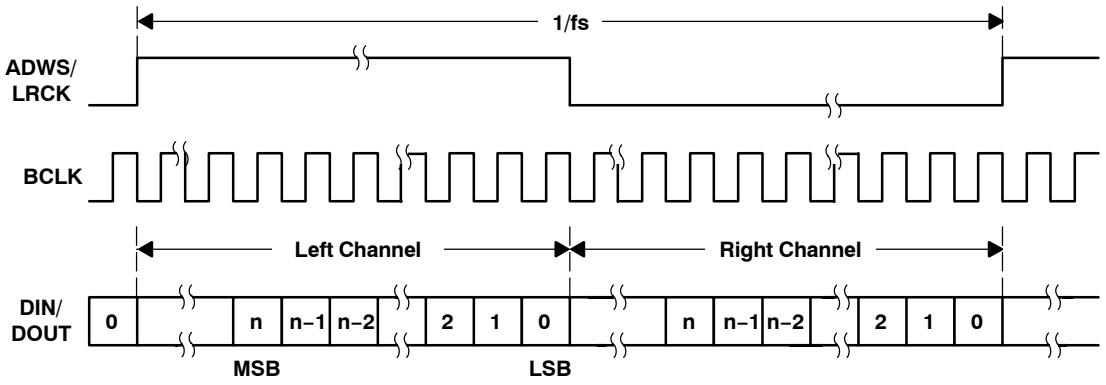


Figure 23. Timing Diagram for Right-Justified Mode

- **LEFT-JUSTIFIED MODE**

  In left–justified mode, the MSB of the right channel is valid on the rising edge of the BCLK, following the falling edge of ADWS or LRCK. Similarly the MSB of the left channel is valid on the rising edge of the BCLK following the rising edge of ADWS or LRCK.

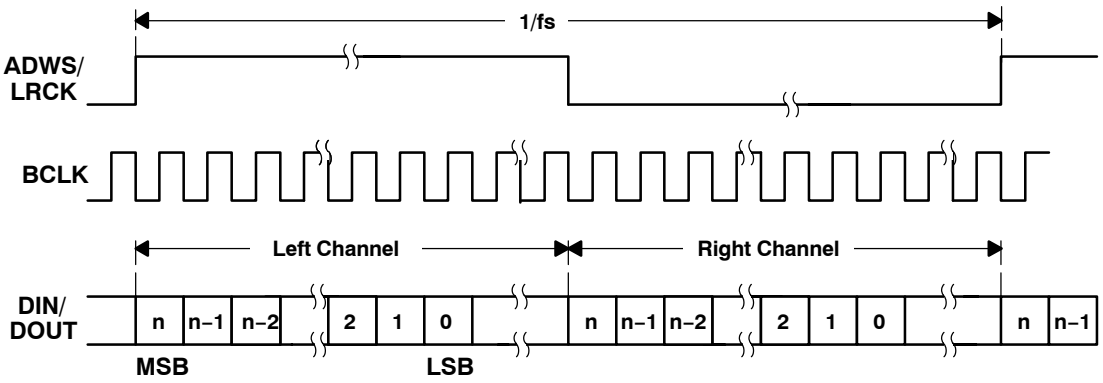


Figure 24. Timing Diagram for Left-Justified Mode

- **I2S MODE**

In I2S mode, the MSB of the left channel is valid on the second rising edge of the BCLK after the falling edge of ADWS or LRCK. Similarly the MSB of the right channel is valid on the second rising edge of the BCLK after the rising edge of ADWS or LRCK.

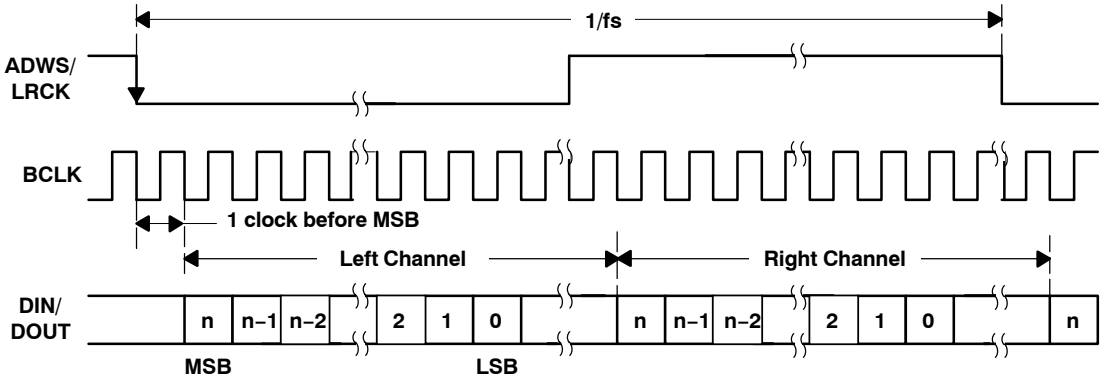


Figure 25. Timing Diagram for I2S Mode

- **DSP MODE**

In DSP mode, the falling edge of ADWS or LRCK starts the data transfer with the left channel data first and immediately followed by the right channel data. Each data bit is valid on the falling edge of BCLK.

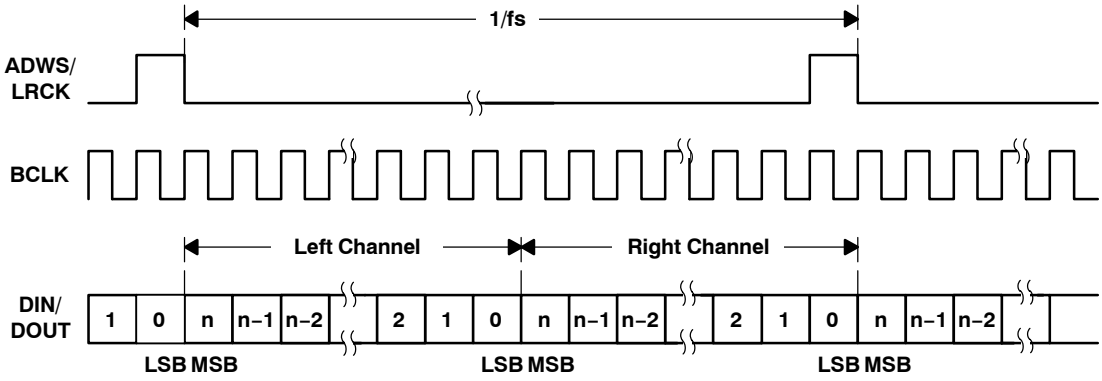


Figure 26. Timing Diagram for DSP Mode

AUDIO DATA CONVERTERS

The TSC2100 includes a stereo audio DAC and a mono audio ADC. Both ADC and DAC can operate with a maximum sampling rate of 53 kHz and support all audio standard rates of 8 kHz, 11.025 kHz, 12kHz, 16kHz, 22.05 kHz, 24 kHz, 32kHz, 44.1 kHz, and 48 kHz. By utilizing the flexible clock generation capability and internal programmable interpolation, a wide variety of sampling rates up to 53 kHz can be obtained from many possible MCLK inputs. In addition, the DAC and ADC can independently operate at different sampling rates as indicated in control register REG–00H/Page2.

When the ADC or DAC is operating, the TSC2100 requires an applied audio MCLK input. The user should also set BIT–D13/REG–06H/Page2 to indicate which Fsref rate is being used. If the codec ADC or DAC is powered up, then the touch screen ADC uses MCLK and BCLK for its internal clocking, and the internal oscillator is powered down to save power.

Typical audio DACs can suffer from poor out-of-band noise performance when operated at low sampling rates, such as 8 kHz or 11.025 kHz. The TSC2100 includes programmable interpolation circuitry to provide improved audio performance at such low sampling rates, by first upsampling low-rate data to a higher rate, filtering to reduce audible images, and then passing the data to the internal DAC, which is actually operating at the Fsref rate. This programmable interpolation is determined using BIT–D5–D3/REG–00H/Page2.

For example, if playback of 11.025-kHz data is required, the TSC2100 can be configured such that Fsref = 44.1 kHz. Then using BIT–D5–D3/REG–00H/Page2, the DAC sampling rate (Fs) can be set to Fsref/4, or Fs = 11.025 kHz. In operation, the 11.025-kHz digital input data is received by the TSC2100, upsampled to 44.1 kHz, and filtered for images. It is then provided to the audio DAC operating at 44.1 kHz for playback. In reality, the audio DAC further upsamples the 44.1 kHz data by a ratio of 128 x and performs extensive interpolation filtering and processing on this data before conversion to a stereo analog output signal.

PLL

The TSC2100 has an on-chip PLL to generate the needed internal ADC and DAC operational clocks from a wide variety of clocks available in the system. The PLL supports an MCLK varying from 2 MHz to 50 MHz and is register programmable to enable generation of required sampling rates with fine precision.

ADC and DAC sampling rates are given by

DAC_FS = Fsref/N1 and ADC_FS = Fsref/N2

where, Fsref must fall between 39 kHz and 53 kHz, and N1, N2 =1, 1.5, 2, 3, 4, 5, 5.5, 6 are register programmable.

The PLL can be enabled or disabled using register programming.

- When PLL is disabled

$$\text{Fsref} = \frac{\text{MCLK}}{128 \times \text{Q}}$$

Q = 2, 3…17

  - Note: For ADC, with N2 = 1.5 or 5.5, odd values of Q are not allowed.
  - In this mode, the MCLK can operate up to 50 MHz, and Fsref should fall within 32 kHz to 53 kHz.

- When PLL is enabled

$$\text{Fsref} = \frac{\text{MCLK} \times \text{K}}{2048 \times \text{P}}$$

P = 1, 2, 3, …, 8

K = J.D

J = 1, 2, 3, ….,64

D = 0, 1, 2, …, 9999

P, J, and D are register programmable, where J is integer part of K before the decimal point, and D is four-digit fractional part of K after the decimal point, including lagging zeros.

Examples: If K = 8.5, Then J = 8, D = 5000
If K = 7.12, Then J = 7, D = 1200
If K = 7.012, Then J = 7, D = 120

The PLL is programmed through Registers 1BH and 1CH of Page2.

- When PLL is enabled and D = 0, the following condition must be satisfied

$$2\ \text{MHz} \leq \frac{\text{MCLK}}{\text{P}} \leq 20\ \text{MHz}$$

$$80\ \text{MHz} \leq \frac{\text{MCLK} \times \text{K}}{\text{P}} \leq 110\ \text{MHz}$$

$$4 \leq \text{J} \leq 55$$

- When PLL is enabled and D ≠ 0, the following condition must be satisfied

$$10\ \text{MHz} \leq \frac{\text{MCLK}}{\text{P}} \leq 20\ \text{MHz}$$

$$80\ \text{MHz} \leq \frac{\text{MCLK} \times \text{K}}{\text{P}} \leq 110\ \text{MHz}$$

$$4 \leq \text{J} \leq 11$$

Example 1:

For MCLK = 12 MHz and Fsref = 44.1 kHz

P = 1, K = 7.5264 $\Rightarrow$ J = 7, D = 5264

Example 2:

For MCLK = 12 MHz and Fsref = 48.0 kHz

P = 1, K = 8.192 $\Rightarrow$ J = 8, D = 1920

MONO AUDIO ADC

Analog Front End

The analog front end of the audio ADC consists of an analog MUX and a programmable gain amplifier (PGA). The MUX can connect either the MICIN or AUX signal through the PGA to the ADC for audio recording. The TSC2100 also has an option of choosing both MICIN and AUX as a differential input pair. The TSC2100 also includes a microphone bias circuit, which can source up to 4 mA of current and is programmable to a 2 V or 2.5 V level. The bias block is powered down when both the ADC and analog mixer blocks are powered down.

Because of the oversampling nature of the audio ADC and the integrated digital dicimation filtering, requirements for analog antialiasing filtering are very relaxed. The TSC2100 integrates a second order analog antialiasing filter with 20-dB attenuation at 1 MHz. This filter, combined with the digital decimal filter, provides sufficient antialiasing filtering without requiring any external components.

The PGA allows analog gain control from 0 dB to 59.5 dB in steps of 0.5 dB. The PGA gain changes are implemented with an internal soft-stepping algorithm that only changes the actual volume level by one 0.5-dB step every one or two ADC output samples, depending on the register programming. This soft-stepping ensures that volume control changes occur smoothly with no audible artifacts. Upon reset, the PGA gain defaults to a mute condition, and upon power down, the PGA soft-steps the volume to mute before shutting down. A read-only flag (D0 control register 04H/Page2) is set whenever the gain applied by PGA equals the desired value set by the register. The soft–stepping control can be disabled by programming D15=1 in register 1DH of Page02. When soft stepping is enabled, the MCLK signal must be applied to the part after the ADC power down register is written to ensure the soft-stepping to mute has completed. When the ADC power down flag is no longer set, the MCLK signal can be shut down.

Delta-Sigma ADC

The analog-to-digital converter is a delta-sigma modulator with 128 times oversampling ratio. The ADC can support a maximum output rate of 53 kHz.

Decimation Filter

The audio ADC includes an integrated digital decimation filter that removes high-frequency content and downsamples the audio data from an initial sampling rate of 128 times Fs to the final output sampling rate of Fs. The decimation filter provides a linear phase output response with a group delay of 17/Fs. The –3-dB bandwidth of the decimation filter extends to 0.45 Fs and scales with the sample rate (Fs)

Automatic Gain Control (AGC)

Automatic gain control (AGC) can be used to maintain nominally constant output signal amplitude when recording speech signals. This circuity automatically adjusts the PGA gain as the input signal becomes overly loud or very weak, such as when a person speaking into a microphone moves closer or farther from the microphone. The AGC algorithm has several programmable settings, including target gain, attack and decay time constants, noise threshold, and maximum PGA gain applicable that allow the algorithm to be fine tuned for any particular application. The algorithm uses the absolute average of the signal (which is the average of the absolute value of the signal) as a measure of the nominal amplitude of the output signal.

Target gain represents the nominal output level at which the AGC attempts to hold the ADC output signal level. The TSC2100 allows programming of eight different target gains, which can be programmed from –5.5 dB to –24 dB relative to a full-scale signal. Since the TSC2100 reacts to the signal absolute average and not to peak levels, it is recommended that the larger gain be set with enough margin to avoid clipping at the occurrence of loud sounds.

Attack time determines how quickly the AGC circuitry reduces the PGA gain when the input signal is too loud. It can be varied from 8 ms to 20 ms.

Decay time determines how quickly the PGA gain is increased when the input signal is too low. It can be varied in the range from 100 ms to 500 ms.

Noise threshold determines level below which if the input speech average value falls, AGC considers it as a silence and hence brings down the gain to 0 dB in steps of 0.5 dB every FS and sets noise threshold flag. The gain stays at 0 dB unless the input speech signal average rises above noise threshold setting. This ensures that noise does not get gained up in the absence of speech. Noise threshold level in the AGC algorithm is programmable from –60 dB to –90 dB relative to full scale. This operation includes debounce and hysteresis to avoid the AGC gain from cycling between high gain and 0 dB when signals are near the noise threshold level. When noise threshold flag is set, status of gain applied by AGC and saturation flag should be ignored.

Maximum PGA applicable allows user to restrict maximum gain applied by AGC. This can be used for limiting PGA gain in situations where environmental noise is greater than programmed noise threshold. It can be programmed from 0 dB to 59.5 dB in steps of 0.5 dB.

See Table 3 for various AGC programming options.

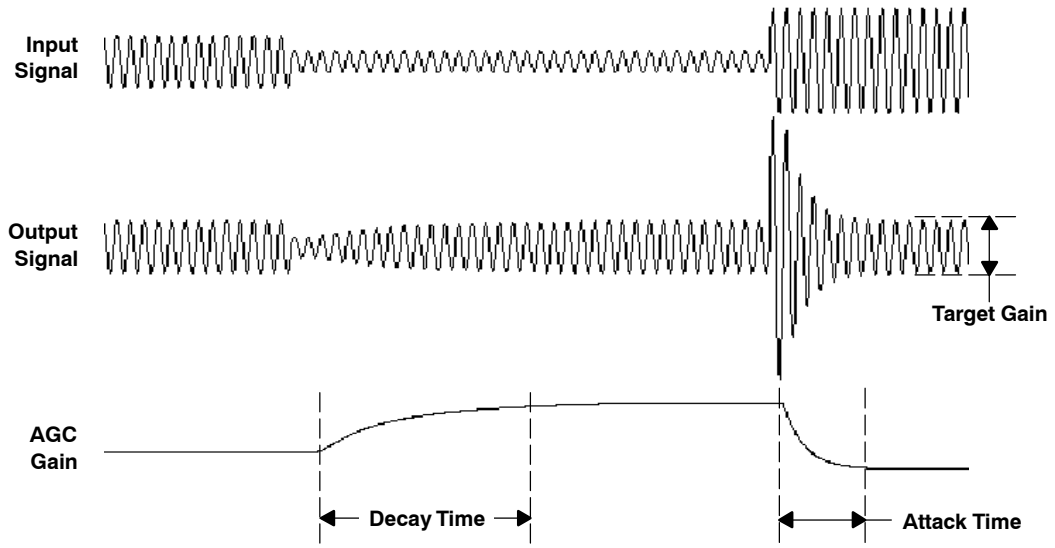


Figure 27. AGC Characteristics

Table 3. AGC Settings

	MIC INPUT	
	BIT	**CONTROL REGISTER**
AGC enable	D0	01H
Target gain	D7–D5	01H
Time constants (attack and decay time)	D4–D1	01H
Noise threshold	D5–D4	06H
Noise threshold flag	D11	04H
Hysteresis	D10–D9	1DH
Debounce time (normal to silence mode)	D8–D6	1EH
Debounce time (silence to normal mode)	D5–D3	1EH
Max PGA applicable	D15–D9	1EH
Gain applied by AGC	D15–D8	01H
Saturation flag	D0	04H
Clip stepping enable	D3	06H

NOTE: All settings shown in Table 2 are located in page2 of control registers.

STEREO AUDIO DAC

Each channel of the stereo audio DAC consists of a digital audio processing block, a digital interpolation filter, digital delta-sigma modulator, and an analog reconstruction filter. The DAC is designed to provide enhanced performance at low sample rates through increased oversampling and image filtering, thereby keeping quantization noise generated within the delta-sigma modulator and signal images strongly suppressed within the audio band to beyond 20 kHz. This is realized by keeping the upsampled rate constant at 128 x Fsref and changing the oversampling ratio as the input sample rate is changed. For Fsref of 48 kHz, the digital delta-sigma modulator always operates at a rate of 6.144 MHz. This ensures that quantization noise generated within the delta-sigma modulator stays low within the frequency band below 20 kHz at all sample rates. Similarly, for Fsref rate of 44.1 kHz, the digital delta-sigma modulator always operates at a rate of 5.6448 MHz.

Digital Audio Processing

The DAC channel consists of optional filters for de-emphasis and bass, treble, midrange level adjustment, or speaker equalization. The de-emphasis function is only available for sample rates of 32 kHz, 44.1 kHz, and 48 kHz. The transfer function consists of a pole with time constant of 50 μs and a zero with time constant of 15 μs. Frequency response plots are given in the *Audio Codec Filter Frequency Responses* section of this data sheet.

The DAC digital effects processing block also includes a fourth order digital IIR filter with programmable coefficients (one set per channel). The filter is implemented as cascade of two biquad sections with frequency response given by:

$$\left(\frac{N0 + 2 \times N1 \times z^{-1} + N2 \times z^{-2}}{32768 - 2 \times D1 \times z^{-1} - D2 \times z^{-2}}\right)\left(\frac{N3 + 2 \times N4 \times z^{-1} + N5 \times z^{-2}}{32768 - 2 \times D4 \times z^{-1} - D5 \times z^{-2}}\right)$$

The N and D coefficients are fully programmable, and the entire filter can be enabled or bypassed. The coefficients for this filter implement a variety of sound effects, with bass-boost or treble boost being the most commonly used in portable audio applications. The default N and D coefficients in the part are given by:

N0 = N3 = 27619 D1 = D4 = 32131

N1 = N4 = –27034 D2 = D5 = –31506

N2 = N5 = 26461

and implement a shelving filter with 0 dB gain from dc to approximately 150 Hz, at which point it rolls off to a 3 dB attenuation for higher frequency signals, thus giving a 3-dB boost to signals below 150 Hz. The N and D coefficients are represented by 16-bit twos complement numbers with values ranging from –32768 to +32767. Frequency response plots are given in the *Audio Codec Filter Frequency Responses* section of this data sheet.

Interpolation Filter

The interpolation filter upsamples the output of the digital audio processing block by the required oversampling ratio. It provides a linear phase output with a group delay of 21/Fs.

In addition, programmable digital interpolation filtering is included to provide enhanced image filtering and reduce signal images caused by the upsampling process that are below 20 kHz. For example, upsampling an 8-kHz signal produces signal images at multiples of 8 kHz (i.e., 8 kHz, 16 kHz, 24 kHz, etc). The images at 8 kHz and 16 kHz are below 20 kHz and still audible to the listener; therefore, they must be filtered heavily to maintain a good quality output. The interpolation filter is designed to maintain at least 65-dB rejection of images that land below 7.455 Fs. In order to utilize the programmable interpolation capability, the Fsref should be programmed to a higher rate (restricted to be in the range of 39 kHz to 53 kHz when the PLL is in use), and the actual Fs is set using the dividers in BIT–D5–D3/REG–00H/Page2. For example, if Fs = 8 kHz is required, then Fsref can be set to 48 kHz, and the DAC Fs set to Fsref/6. This ensures that all images of the 8-kHz data are sufficiently attenuated well beyond a 20-kHz audible frequency range.

Delta-Sigma DAC

The audio digital-to-analog converter incorporates a third order multibit delta-sigma modulator followed by an analog reconstruction filter. The DAC provides high-resolution, low-noise performance, using oversampling and noise shaping techniques. The analog reconstruction filter design consists of a 6 tap analog FIR filter followed by a continuous time RC filter. The analog FIR operates at a rate of 128 x Fsref (6.144 MHz when Fsref = 48 kHz, 5.6448 MHz when Fsref = 44.1 kHz). Note that the DAC analog performance may be degraded by excessive clock jitter on the MCLK input. Therefore, care must be taken to keep jitter on this clock to a minimum.

DAC Digital Volume Control

The DAC has a digital volume control block, which implements programmable gain. The volume level can be varied from 0dB to –63.5 dB in 0.5 dB steps, in addition to a mute bit, independently for each channel. The volume level of both channels can also be changed simultaneously by the master volume control. The gain is implemented with a soft-stepping algorithm, which only changes the actual volume by one step per input sample, either up or down, until the desired volume is reached. The rate of soft-stepping can be slowed to one step per two input samples through bit D1 of control register 04H/Page2.

Because of soft-stepping, the host does not know when the DAC has been actually muted. This may be important if the host wishes to mute the DAC before making a significant change, such as changing sample rates. In order to help with this situation, the TSC2100 provides a flag back to the host via a read-only register bit (D2–D3 of control register 04H/Page2) that alerts the host when the part has completed the soft-stepping and the actual volume has reached the desired volume level. The soft-stepping feature can be disabled by programming D14=1 in register 1DH in Page02. If soft-stepping is enabled, the MCLK signal should be kept applied to the device until the DAC power-down flag is set. When this flag is set, the internal soft-stepping process and power down sequence is complete, and the MCLK can be stopped if desired.

The TSC2100 also includes functionality to detect when the user switches on or off the de-emphasis or digital audio processing functions, to first (1) soft-mute the DAC volume control, (2) change the operation of the digital effects processing, and (3) soft-unmute the part. This avoids any possible pop/clicks in the audio output due to instantaneous changes in the filtering. A similar algorithm is used when first powering up or down the DAC. The circuit begins operation at power up with the volume control muted, then soft-steps it up to the desired volume level. At power down, the logic first soft-steps the volume down to a mute level, then powers down the circuitry.

DAC Powerdown

The DAC powerdown flag (D6 of REG05H/Page2) along with D10 of REG05H/Page2 denotes the powerdown status of the DAC according to Table 4.

Table 4. DAC Powerdown Status

[D10,D6]	POWERUP / DOWN STATE OF DAC
[0,0]	DAC is in stable powerup state
[0,1]	DAC is in the process of powering up. The length of this state is determined by PLL and output driver powerup delays controlled by register programming.
[1,0]	DAC is in the process of powering down. The length of this state is determined by soft-stepping of volume control block and DAC pop reduction sequencing controlled by register programming.
[1,1]	DAC is in a stable powerdown state.

AUDIO OUTPUT DRIVERS

The TSC2100 features audio output drivers which can be configured in either low power mode or high power mode depending on the load and output power required. By default, at reset the output drivers are configured in low power mode. In this mode, the output drivers can drive a full-scale line-level signal into loads of 10 kΩ minimum or drive moderate amplitude signals into loads of 16 Ω minimum.

The output drivers can also be configured in high power mode by setting bit D12 of Reg05H/Page2 to *1*. In this mode, each output driver can deliver up to 30 mW per channel into a headphone speaker load of 16 Ω. The headphones can be connected in a single ended configuration using ac-coupling capacitors, or the capacitors can be removed and virtual ground (VGND) powered for a capless output connection. The typical headphone jack configuration for these two modes is shown in Figure 30. Note that the VGND amplifier must be powered if the capless configuration is used.

In the case of an ac-coupled output, the value of the capacitors is typically chosen based on the amount of low-frequency cut that can be tolerated. The capacitor in series with the load impedance forms a high-pass filter with –3 dB cutoff frequency of $1/(2\pi RC)$ in Hz, where R is the impedance of the headphones. Use of an overly small capacitor reduces low-frequency components in the signal output and lead to low-quality audio. When driving 16-Ω headphones, capacitors of 220-μF (a commonly used value) result in a high-pass filter cutoff frequency of 45 Hz, although reducing these capacitors to 50 μF results in a cutoff frequency of 199 Hz, which is generally considered noticeable when playing music. The cutoff frequency is reduced to half of the above values if 32-Ω headphones are used instead of 16 Ω.

The TSC2100 programmable digital effects block can be used to help reduce the size of capacitors needed by implementing a low frequency boost function to help compensate for the high-pass filter introduced by the ac-coupling capacitors. For example, by using 50-μF capacitors and setting the TSC2100 programmable filter coefficients as shown below, the frequency response can be improved as shown in Figure 29.

Filter coefficients (use the same for both channels):

N0 = 32767, N1 = –32346, N2 = 31925, N3 = 32767, N4 = 0, N5 = 0

D0 = 32738, D1 = –32708 D4 = 0, D5 = 0

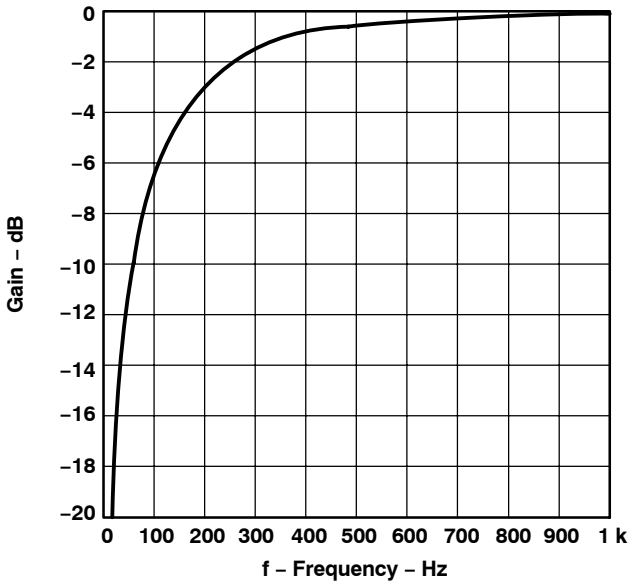


Figure 28. Uncompensated Response For 16-Ω Load and 50-μF Decoupling Capacitor

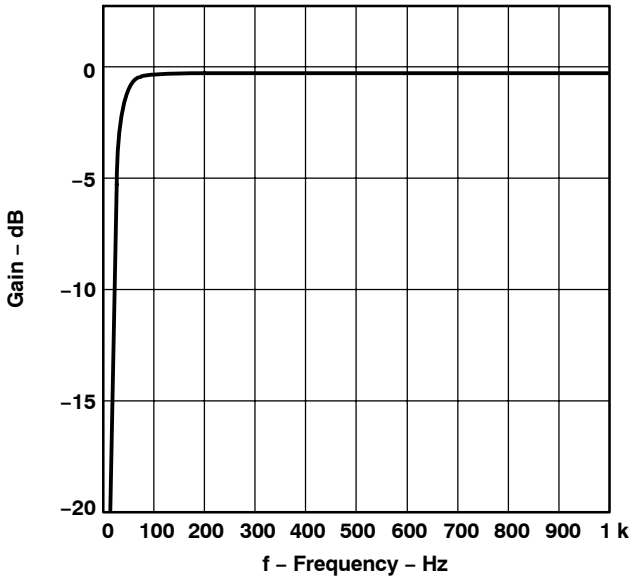


Figure 29. Frequency Response For 16-Ω Load and 50-μF Decoupling Capacitor After Gain Compensation Using Above Set of Coefficients for Audio Effects Filter

Using the capless output configuration eliminates the need for these capacitors and removes the accompanying high-pass filter entirely. However, this configuration does have one drawback – if the RETURN terminal of the headphone jack (which is wired to the TSC2100 VGND pin) is ever connected to a ground, that is shorted to the TSC2100 ground pin, then the VGND amplifier enters short-circuit protection, and the audio output does not function properly.

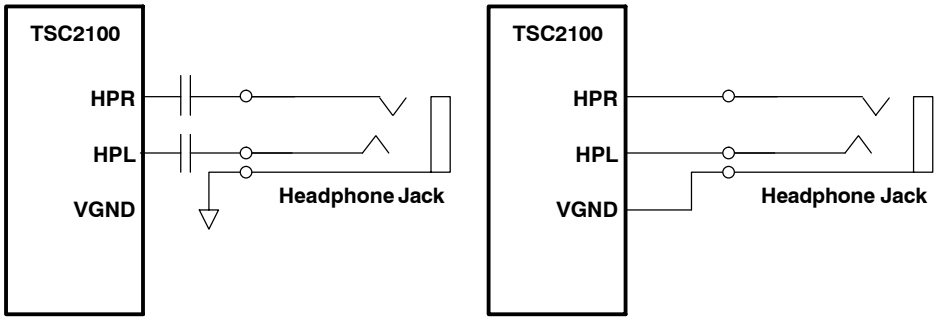


Figure 30. Headphone Configurations, AC-Coupled (left) and Capless (right)

The audio output drivers in high power mode can also be configured to drive a mono differential signal into a speaker load of 8-Ω minimum. The speaker load should be connected differentially between the HPR and HPL outputs. There are several options for playback of DAC data in this case. If a stereo digital signal is available, this signal can be sent in normal stereo fashion to the audio DAC. The programmable digital effects filters can then be used to invert one channel, so that the signal applied across the speaker load is (LEFT + RIGHT), or effectively a mono-mix of the two channels. A simple example of how to implement this inversion using the programmable filters is to set the coefficients as follows:

Left–channel coefficients: N0=32767, N1=0, N2=0, N3=32767, N4=0, N5=0
D1=0, D2=0, D4=0, D5=0

Right–channel coefficients: N0=–32767, N1=0, N2=0, N3=32767, N4=0, N5=0
D1=0, D2=0, D4=0, D5=0

This provides no spectral shaping, it only inverts the right channel relative to the left channel, such that the signals at HPL and HPR are (LEFT) and (–RIGHT), with the signal across the speaker then being LEFT+ RIGHT. In a general case when spectral shaping is also desired, the inversion can be accomplished simply by setting N0, N1, and N2 coefficients of one channel to the negative of the values set for the other channel. Note that the programmable filtering must be enabled by setting BIT–D1/REG–05H/Page2 to *1*.

To enable the output drivers to deliver higher output power, the DAC output swing should be set to its highest level by setting BIT–D10–D9/REG–06H/Page2 to *11*. It is possible to increase power even further by disabling the built-in short-circuit protection by programming bit D8 of Reg1DH/Page2 to *1*. In this case care must be taken so a short-circuit at the output does not occur. Figure 31 shows a typical jack configuration using a capless output configuration. In this configuration, the TSC2100 drives the loudspeaker whenever headphones are not inserted in the jack and drives the headphones whenever it is inserted in the jack.

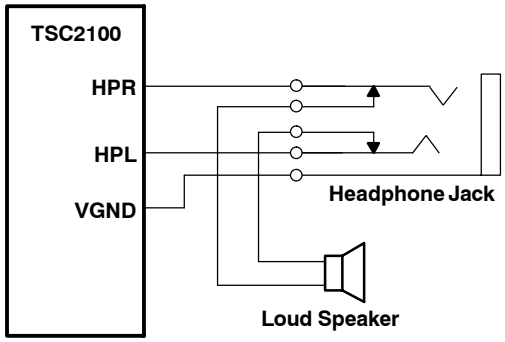


Figure 31. Speaker Connection

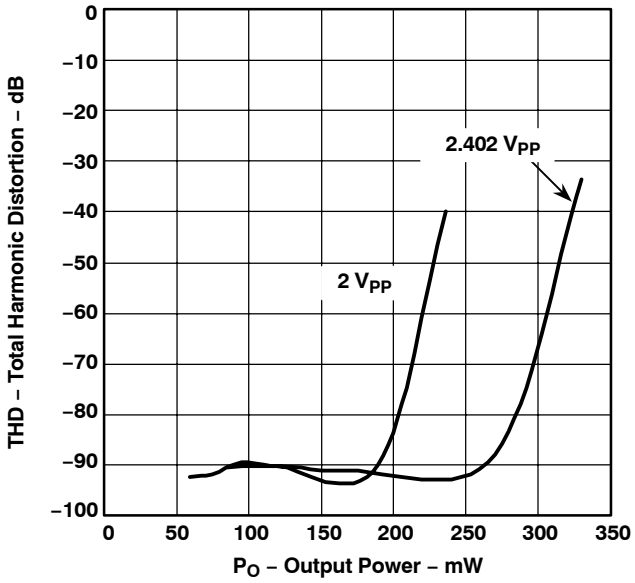


Figure 32. THD vs Output Power Delivered to an an 8-Ω Load (25°C, AVDD = DRVDD = 3.3 V, DVDD = 1.8 V, DAC Output Swing Set to 2 V and 2.4V, and Short-Circuit Protection Disabled)

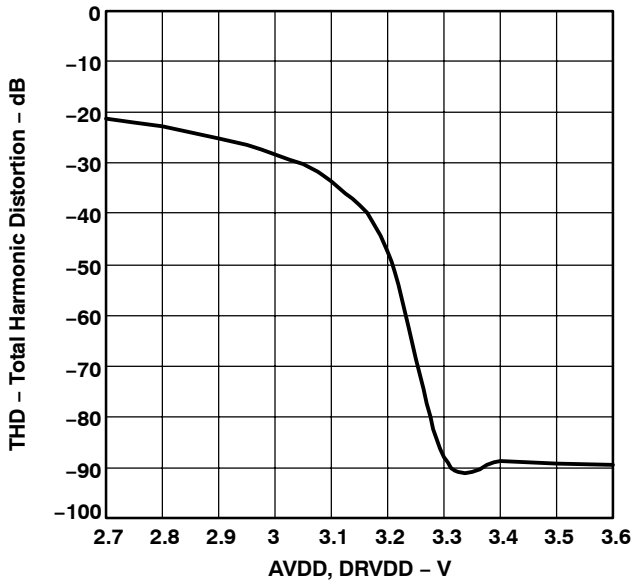


Figure 33. THD vs AVDD, DRVDD Supply Voltage (25°C When Driving a –1 dB, 1-kHz Sinewave From the DAC Into an 8-Ω Load, with DAC Output Swing Set to 2.4 V, and Short-Circuit Protection Disabled)

The TSC2100 incorporates a programmable short-circuit detection/protection function with different modes of operation. During the insertion or removal of a headphone plug from the jack, the output pins of the drivers may be accidentally shorted, causing the part to potentially draw a huge current, which may cause the power supply voltages to dip. Bits D8–D7 of REG–1DH/Page2 control how the short-circuit detection/protection operates in the TSC2100. One option is to fully disable short-circuit protection, which also enables the audio output drivers to deliver more power to a low-impedance load (such as an 8-Ω speaker). However, care must be taken to prevent any short-circuit from occurring while the part is in this mode.

A second programmable configuration enables current-limiting in the audio output drivers, so that excessive currents cannot be provided if the outputs are shorted. It also enables the internal short-circuit detection function, which can detect excess current being drawn from the drivers and set a short circuit detect flag (Page2, REG–1DH, BIT–D6). This flag can be read by the user to powerdown the drivers if desired. This flag is cleared only if the short-circuit condition is removed. If the user does not monitor this flag and powers down the drivers when a short-circuit occurs, the current-limiting prevents excessive currents from being drawn, but power dissipation is higher due to this limited current flowing through the short.

In a third programmable configuration, the TSC2100 can be programmed to monitor and automatically powerdown the audio output drivers upon detection of a short-circuit condition (Page2, REG–1DH, BIT–D7), in addition to setting the short-circuit flag in Page2, REG–1DH, BIT–D6. When the device has detected a short and resulted in this condition, the short-circuit flag is cleared when all the routings to the speaker driver are disabled (i.e. DAC, Analog Mixer, and Keyclick blocks are powered down by user).

AUDIO OUTPUT DRIVER POWER-ON POP REDUCTION SCHEME

The TSC2100 implements a pop reduction scheme to reduce audible artifacts during powerup and powerdown of the audio output drivers. This scheme can be controlled by programming bits D2 and D1 of REG1EH/Page2. By default, the driver pop reduction scheme is enabled and can be disabled by programming bit D2 of Reg1EH/Page2 to *1*. When this scheme is enabled and the virtual ground connection is not used (VGND amplifier is powered down), the audio output driver slowly charges up any external ac-coupling capacitors to reduce audible artifacts. Bit D1 of REG1EH/Page2 provides control of the charging time for the ac-coupling capacitor as either 0.8 sec or 4 sec. When the virtual ground amplifier is powered up and used, the external ac-coupling capacitor is eliminated, and the powerup time becomes either 1 ms or 5 ms. This scheme takes effect whenever the audio output drivers are powered up due to enabling any of the DAC, the Analog Mixer or the Keyclick Generator.

Pop Reduction For DAC Routing

Whenever the audio DAC is powered on or off, there may be a slight change in the output dc offset voltage and can be heard as a weak pop in the output. In order to reduce this artifact, the TSC2100 implements a DAC pop reduction scheme, which is programmable using bits D5–D2 in REG–1DH/Page2. Bit D5 enables the scheme, which implements a slow transition between the starting dc level and the final dc level. For best results program D4–D2 in REG1DH/Page2 to *100*.

AUDIO MIXING

Digital Sidetone

The digital sidetone control attenuates the output from the ADCs decimation filter and routes its output to be mixed with the DAC digital input. If bit D7 of REG–03H/Page2 is reset, the output of the sidetone control is mixed with the stereo DAC input. Care must be taken while selecting the digital sidetone gain such that the output of the digital mixer is not overloaded. The digital sidetone block implements gains from 0 dB to –48 dB in steps of 1.5 dB. Gain changes are implemented at zero-crossings of the signal to avoid any audible artifacts. The digital sidetone block is automatically internally disabled if ADC and DAC are operating at different sampling rates, or if the DAC is powered down.

Analog Mixer

The analog mixer can be used to route the analog input selected for the ADC (MICIN or AUX) through an analog volume control and then mix it with the audio DAC output. The analog mixer feature is available only if single-ended MICIN or AUX is selected as the input to the ADC, not when the ADC input is configured in fully-differential mode. This feature is available even if the ADC and DAC are powered down. The analog volume control in this path has a gain range from 12 dB to –34.5 dB in 0.5-dB steps plus mute and includes soft-stepping logic. The internal oscillator is used for soft stepping whenever the ADC and DAC are powered down.

KEYCLICK

A special circuit has been included for inserting a square–wave signal into the analog output signal path based on register control. This functionality is intended for generating keyclick sounds for user feedback. Register 04H/Page2 contains bits that control the amplitude, frequency, and duration of the square-wave signal. The frequency of the signal can be varied from 62.5 Hz to 8 kHz and its duration can be programmed from 2 periods to 32 periods. Whenever this register is written, the square-wave is generated and coupled into the audio output, going to both audio outputs. The keyclick enable bit D15 of control register 04H/Page2 is reset after the duration of keyclick is played out. This capability is available even when the ADC and DAC are powered down.

SPI DIGITAL INTERFACE

All TSC2100 control registers are programmed through a standard SPI bus. The SPI allows full-duplex, synchronous, serial communication between a host processor (the master) and peripheral devices (slaves). The SPI master generates the synchronizing clock and initiates transmissions. The SPI slave devices depend on a master to start and synchronize transmissions.

A transmission begins when initiated by a master SPI. The byte from the master SPI begins shifting in on the slave SPIDIN (MOSI) pin under the control of the master serial clock. As the byte shifts in on the SPIDIN pin, a byte shifts out on the SPIDOUT (MISO) pin to the master shift register.

The idle state of the serial clock for the TSC2100 is low, which corresponds to a clock polarity setting of 0 (typical microprocessor SPI control bit CPOL = 0). The TSC2100 interface is designed so that with a clock phase bit setting of 1 (typical microprocessor SPI control bit CPHA = 1), the master begins driving its MOSI pin and the slave begins driving its SPIDOUT pin on the first serial clock edge. The $\overline{SS}$ pin can remain low between transmissions; however, the TSC2100 only interprets command words which are transmitted after the falling edge of $\overline{SS}$.

TSC2100 COMMUNICATION PROTOCOL

Register Programming

The TSC2100 is entirely controlled by registers. Reading and writing these registers is controlled by an SPI master and accomplished by the use of a 16-bit command, which is sent prior to the data for that register. The command is constructed as shown in Figure 34.

The command word begins with a R/W bit, which specifies the direction of data flow on the SPI serial bus. The following 4 bits specify the page of memory this command is directed to, as shown in Table 5. The next six bits specify the register address on that page of memory to which the data is directed. The last five bits are reserved for future use and should be written only with zeros.

Table 5. Page Addressing

PG3	PG2	PG1	PG0	PAGE ADDRESSED
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	Reserved
0	1	0	0	Reserved
0	1	0	1	Reserved
0	1	1	0	Reserved
0	1	1	1	Reserved
1	0	0	0	Reserved
1	0	0	1	Reserved
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

To read all the first page of memory, for example, the host processor must send the TSC2100 the command 0x8000 – this specifies a read operation beginning at page 0, address 0. The processor can then start clocking data out of the TSC2100. The TSC2100 automatically increments its address pointer to the end of the page; if the host processor continues clocking data out past the end of a page, the TSC2100 sends back the value 0xFFFF.

Likewise, writing to page 1 of memory consists of the processor writing the command 0x0800, which specifies a write operation, with PG0 set to 1, and all the ADDR bits set to 0. This results in the address pointer pointing at the first location in memory on Page 1. See the section on the TSC2100 memory map for details of register locations

BIT 15 MSB	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 LSB
R/W*	PG3	PG2	PG1	PG0	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0	0	0	0	0	0

Figure 34. TSC2100 Command Word

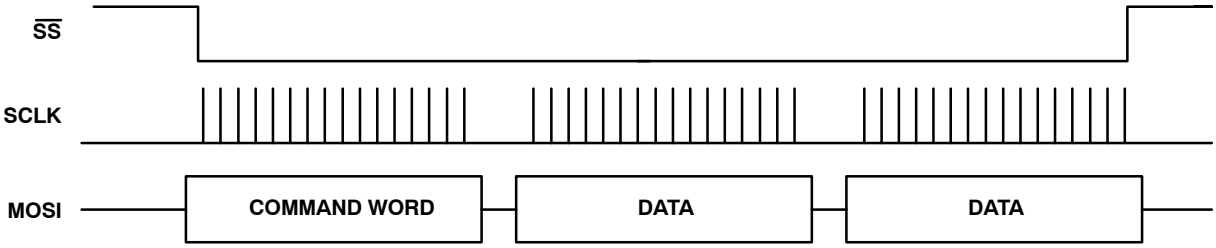


Figure 35. Write Operation for TSC2100 SPI Interface

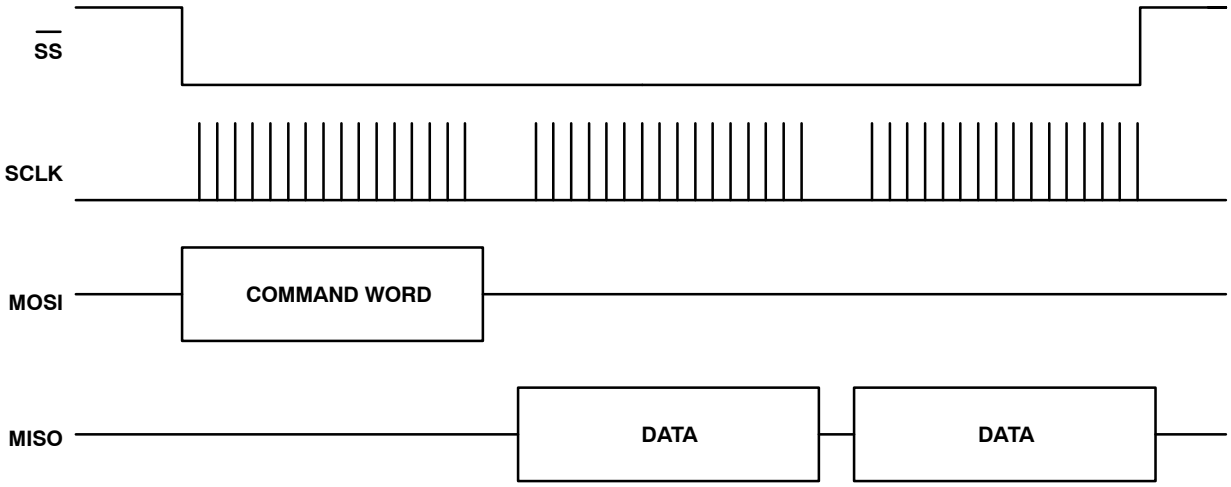


Figure 36. Read Operation for TSC2100 SPI Interface

TSC2100 MEMORY MAP

The TSC2100 has several 16-bit registers which allow control of the device as well as providing a location for results from the TSC2100 to be stored until read by the host microprocessor. These registers are separated into three pages of memory in the TSC2100: a data page (Page 0) and control pages (Page 1 and Page 2). The memory map is shown in Table 6.

Table 6. Memory Map

Page 0: Touch Screen Data Registers		Page 1: Touch Screen Control Registers		Page 2: Audio Control Registers	
ADDR	**REGISTER**	**ADDR**	**REGISTER**	**ADDR**	**REGISTER**
00	X	00	TSC ADC	00	Audio Control 1
01	Y	01	Status	01	Codec ADC Gain
02	Z1	02	Reserved	02	Codec DAC Gain
03	Z2	03	Reference	03	Codec Sidetone
04	Reserved	04	Reset	04	Audio Control 2
05	BAT1	05	Configuration	05	Codec Power Control
06	BAT2	06	Reserved	06	Audio Control 3
07	AUX	07	Reserved	07	Digital Audio Effects Filter Coefficients
08	Reserved	08	Reserved	08	Digital Audio Effects Filter Coefficients
09	TEMP1	09	Reserved	09	Digital Audio Effects Filter Coefficients
0A	TEMP2	0A	Reserved	0A	Digital Audio Effects Filter Coefficients
0B	Reserved	0B	Reserved	0B	Digital Audio Effects Filter Coefficients
0C	Reserved	0C	Reserved	0C	Digital Audio Effects Filter Coefficients
0D	Reserved	0D	Reserved	0D	Digital Audio Effects Filter Coefficients
0E	Reserved	0E	Reserved	0E	Digital Audio Effects Filter Coefficients
0F	Reserved	0F	Reserved	0F	Digital Audio Effects Filter Coefficients
10	Reserved	10	Reserved	10	Digital Audio Effects Filter Coefficients
11	Reserved	11	Reserved	11	Digital Audio Effects Filter Coefficients
12	Reserved	12	Reserved	12	Digital Audio Effects Filter Coefficients
13	Reserved	13	Reserved	13	Digital Audio Effects Filter Coefficients
14	Reserved	14	Reserved	14	Digital Audio Effects Filter Coefficients
15	Reserved	15	Reserved	15	Digital Audio Effects Filter Coefficients
16	Reserved	16	Reserved	16	Digital Audio Effects Filter Coefficients
17	Reserved	17	Reserved	17	Digital Audio Effects Filter Coefficients
18	Reserved	18	Reserved	18	Digital Audio Effects Filter Coefficients
19	Reserved	19	Reserved	19	Digital Audio Effects Filter Coefficients
1A	Reserved	1A	Reserved	1A	Digital Audio Effects Filter Coefficients
1B	Reserved	1B	Reserved	1B	PLL Programmability
1C	Reserved	1C	Reserved	1C	PLL Programmability
1D	Reserved	1D	Reserved	1D	Audio Control 4
1E	Reserved	1E	Reserved	1E	Audio Control 5
1F	Reserved	1F	Reserved	1F	Reserved

TSC2100 CONTROL REGISTERS

This section describes each of the registers shown in the memory map of Table 6. The registers are grouped according to the function they control. In the TSC2100, bits in control registers can refer to slightly different functions depending upon whether you are reading the register or writing to it.

TSC2100 Data Registers (Page 0)

The data registers of the TSC2100 hold data results from conversion of touch screen ADC. All of these registers default to 0000H upon reset. These registers are *read only*.

X, Y, Z1, Z2, BAT1, BAT2, AUX, TEMP1 and TEMP2 Registers

The results of all A/D conversions are placed in the appropriate data register. The data format of the result word, R, of these registers is right-justified, as follows:

BIT 15 MSB	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 LSB
0	0	0	0	R11 MSB	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0 LSB

PAGE 1 CONTROL REGISTER MAP

REGISTER 00H: Touch Screen ADC Control

BIT	NAME	RESET VALUE	FUNCTION
D15	PSTCM	0(for read status) 0(for write status)	Pen Status/Control Mode. READ 0 => There is no screen touch (default) 1 => The pen is down WRITE 0 => Host controlled touch screen conversions(default). 1=> TSC2100 controlled touch screen conversions.
D14	ADST	1(for read status) 0(for write status)	A/D Status. READ 0 => ADC is busy 1 => ADC is not busy (default) WRITE 0 => Normal mode. (default) 1 => Stop conversion and power down. Power down happens immediately
D13–10	ADSCM	0000	A/D Scan Mode. 0000 => No scan 0001 => Touch screen scan function: X and Y coordinates are converted and the results returned to X and Y data registers. Scan continues until either the pen is lifted or a stop bit is sent. 0010 => Touch screen scan function: X, Y, Z1 and Z2 coordinates are converted and the results returned to X, Y, Z1 and Z2 data registers. Scan continues until either the pen is lifted or a stop bit is sent. 0011 => Touch screen scan function: X coordinate is converted and the results returned to X data register. 0100 => Touch screen scan function: Y coordinate is converted and the results returned to Y data register. 0101 => Touch screen scan function: Z1 and Z2 coordinates are converted and the results returned to Z1 and Z2 data registers. 0110 => BAT1 input is converted and the result is returned to the BAT1 data register. 0111 => BAT2 input is converted and the result is returned to the BAT2 data register. 1000 => AUX input is converted and the result is returned to the AUX data register. 1001 => Scan function :AUX input is converted and the result is returned to the AUX data register. Scan continues until stop bit is sent. 1010 => TEMP1 is converted and the result is returned to the TEMP1 data register. 1011 => Port scan function: BAT1, BAT2 and AUX inputs are measured and the results returned to the appropriate data registers. 1100 => TEMP2 is converted and the result is returned to the TEMP2 data register. 1101 => Turn on X+, X– drivers 1110 => Turn on Y+, Y– drivers 1111 => Turn on Y+, X– drivers

BIT	NAME	RESET VALUE	FUNCTION
D9–D8	RESOL	00	Resolution Control. The A/D converter resolution is specified with these bits. 00 => 12–bit resolution 01 => 8–bit resolution 10 => 10–bit resolution 11 => 12–bit resolution
D7–D6	ADAVG	00	Converter Averaging Control. These two bits allow you to specify the number of averages the converter performs selected by bit D0, which selects either mean filter or median filter. Mean Filter / Median filter 00 => No average / No average 01 => 4–data average / 5-data average 10 => 8–data average / 9-data average 11 => 16–data average / 15-data average
D5–D4	ADCR	00	Conversion Rate Control. These two bits specify the internal clock rate which the A/D converter uses to perform a single conversion. These bits are the same whether reading or writing. $t_{conv} = \frac{N + 4}{f_{INTCLK}}$ where f_{INTCLK} is the internal clock frequency. For example, with 12 bit resolution and a 2-MHz internal clock frequency, the conversion time is 8.0 μs. This yields an effective throughput rate of 125 kHz. 00 => 8-MHz internal clock rate (use for 8-bit resolution only) 01 => 4-MHz internal clock rate (use for 8-bit/10-bit resolution only) 10 => 2-MHz internal clock rate 11 => 1-MHz internal clock rate
D3–D1	PVSTC	000	Panel Voltage Stabilization Time Control. These bits allow you to specify a delay time from the time the touch screen drivers are enabled to the time the voltage is sampled and a conversion is started. This allows the user to adjust for the settling of the individual touch panel and external capacitances. 000 => 0-μs stabilization time 001 => 100-μs stabilization time 010 => 500-μs stabilization time 011 => 1-ms stabilization time 100 => 5-ms stabilization time 101 => 10-ms stabilization time 110 => 50-ms stabilization time 111 => 100-ms stabilization time
D0	AVGFS	0	Average Filter select 0 => Mean filter 1 => Median filter

REGISTER 01H: Status Register

BIT	NAME	READ/ WRITE	RESET VALUE	FUNCTION
D15–D14	$\overline{\text{PINTDAV}}$	R/W	10	Pen Interrupt or Data Available. These two bits program the function of the $\overline{\text{PINTDAV}}$ pin. 00 => Acts as PEN interrupt (Active Low) only. When PEN touch is detected, $\overline{\text{PINTDAV}}$ goes low. 01 => Acts as data available (Active Low) only. The $\overline{\text{PINTDAV}}$ goes low as soon as one set of ADC conversion is completed. For scan mode, $\overline{\text{PINTDAV}}$ remains low as long as all the appropriate registers have not been read out. 10 => Acts as both PEN interrupt and data available. When PEN touch is detected, $\overline{\text{PINTDAV}}$ goes low. $\overline{\text{PINTDAV}}$ goes high once all the selected conversions are over. 11 => Same as 10
D13	PWRDN	R	0	TSC–ADC Power down status 0 => TSC–ADC is active 1 => TSC–ADC stops conversion and powers down
D12	HCTLM	R	0	Host Controlled Mode Status 0 => Host controlled mode 1 => Self (TSC2100) controlled mode
D11	DAVAIL	R	0	Data Available Status 0 => No data available. 1 => Data is available(i.e. one set of conversion is done) Note:– This bit gets cleared only after all the converted data have been completely read out.
D10	XSTAT	R	0	X Data Register Status 0 => No new data is available in X–data register 1 => New data for X–coordinate is available in register Note: This bit gets cleared only after the converted data of X coordinate has been completely read out of the register.
D9	YSTAT	R	0	Y Data Register Status 0 => No new data is available in Y–data register 1 => New data for Y–coordinate is available in register Note: This bit gets cleared only after the converted data of Y coordinate has been completely read out of the register.
D8	Z1STAT	R	0	Z1 Data Register Status 0 => No new data is available in Z1–data register 1 => New data is available in Z1–data register Note: This bit gets cleared only after the converted data of Z1 coordinate has been completely read out of the register.
D7	Z2STAT	R	0	Z2 Data Register Status 0 => No new data is available in Z2–data register 1 => New data is available in Z2–data register Note: This bit gets cleared only after the converted data of Z2 coordinate has been completely read out of the register.
D6	B1STAT	R	0	BAT1 Data Register Status 0 => No new data is available in BAT1–data register 1 => New data is available in BAT1–data register Note: This bit gets cleared only after the converted data of BAT1 has been completely read out of the register.
D5	B2STAT	R	0	BAT2 Data Register Status 0 => No new data is available in BAT2–data register 1 => New data is available in BAT2–data register Note: This bit gets cleared only after the converted data of BAT2 has been completely read out of the register.
D4	AXSTAT	R	0	AUX Data Register Status 0 => No new data is available in AUX–data register 1 => New data is available in AUX–data register Note: This bit gets cleared only after the converted data of AUX has been completely read out of the register.
D3		R	0	Reserved

BIT	NAME	READ/ WRITE	RESET VALUE	FUNCTION
D2	T1STAT	R	0	TEMP1 Data Register Status 0 => No new data is available in TEMP1–data register 1 => New data is available in TEMP1–data register Note: This bit gets cleared only after the converted data of TEMP1 has been completely read out of the register.
D1	T2STAT	R	0	TEMP2 Data Register Status 0 => No new data is available in TEMP2–data register 1 => New data is available in TEMP2–data register Note: This bit gets cleared only after the converted data of TEMP2 has been completely read out of the register.
D0		R	0	Reserved

REGISTER 02H: Reserved

BIT	NAME	READ/ WRITE	RESET VALUE	FUNCTION
D15–D0		R	FFFFH	Reserved

REGISTER 03H: Reference Control

BIT	NAME	READ/ WRITE	RESET VALUE	FUNCTION
D15–D5		R	000H	Reserved
D4	VREFM	R/W	0	Voltage Reference Mode. This bit configures the VREF pin as either external reference or internal reference. 0 => External reference 1 => Internal reference
D3–D2	RPWUDL	R/W	00	Reference Power Up Delay. These bits allow for a delay time for measurements to be made after the reference powers up, thereby assuring that the reference has settled 00 => 0 μs 01 => 100 μs 10 => 500 μs 11 => 1000 μs Note: This is valid only when the device is programmed for internal reference and Bit D1 = 1, i.e., reference is powered down between the conversions if not required.
D1	RPWDN	R/W	1	Reference Power Down. This bit controls the power down of the internal reference voltage. 0 => Powered up at all times. 1 => Powered down between conversions. Note: when D4 = 0, i.e. device is in external reference mode, then the internal reference is powered down always.
D0	IREFV	R/W	0	Internal Reference Voltage. This bit selects the internal voltage reference level for the TSC ADC. 0 => VREF = 1.25 V 1 => VREF = 2.50 V

REGISTER 04H: Reset Control

BIT	NAME	READ/ WRITE	RESET VALUE	FUNCTION
D15–D0	RSALL	R/W	FFFFH	Reset All. Writing the code 0xBB00, as shown below, to this register causes the TSC2100 to reset all its registers to their default, power–up values. 1011101100000000 => Reset all registers Others => Do not write other sequences to this register.

REGISTER 05H: Configuration Control

BIT	NAME	READ/ WRITE	RESET VALUE	FUNCTION
D15–D6		R	000H	Reserved. Only write zeros to these bits.
D5–D3	PRECTM	R/W	000	Precharge Time. These bits set the amount of time allowed for precharging any pin capacitance on the touch screen prior to sensing if a screen touch is happening. 000 => 20 µs 001 => 84 µs 010 => 276 µs 011 => 340 µs 100 => 1.044 ms 101 => 1.108 ms 110 => 1.300 ms 111 => 1.364 ms
D2–D0	RPWUDL	R/W	000	Sense Time. These bits set the amount of time the TSC2100 waits to sense whether the screen is being touched, when converting a coordinate value. 000 => 32 µs 001 => 96 µs 010 => 544 µs 011 => 608 µs 100 => 2.080 ms 101 => 2.144 ms 110 => 2.592 ms 111 => 2.656 ms

PAGE 2 CONTROL REGISTER MAP

REGISTER 00H: Audio Control 1

BIT	NAME	READ/ WRITE	RESET VALUE	FUNCTION
D15–D14	ADCHPF	R/W	00	ADC High Pass Filter 00 => Disabled 01 => –3dB point = 0.0045*Fs 10 => –3dB point = 0.0125*Fs 11 => –3dB point = 0.025*Fs Note: Fs is ADC sample rate
D13–D12	ADCIN	R/W	00	ADC Input Mux 00 => ADC Input = Single-ended input MIC 01 => ADC Input = Single-ended input AUX 10 => ADC Input = Differential input MICIN and AUX 11 => ADC Input = Differential input MICIN and AUX
D11–D10	WLEN	R/W	00	Codec Word Length 00 => Word length = 16 bit 01 => Word length = 20 bit 10 => Word length = 24 bit 11 => Word length = 32 bit
D9–D8	DATFM	R/W	00	Digital Data Format 00 => I2S mode 01 => DSP mode 10 => Right justified 11 => Left justified Note: Right justified, valid only when the ratio between DAC and ADC sample rate is an integer. e.g. ADC = 32 kHz and DAC = 24 kHz or vice-versa is invalid for right justified mode.
D7–D6		R	00	Reserved
D5–D3	DACFS	R/W	000	DAC Sampling Rate 000 => DAC FS = Fsref/1 001 => DAC FS = Fsref/(1.5) 010 => DAC FS = Fsref/2 011 => DAC FS = Fsref/3 100 => DAC FS = Fsref/4 101 => DAC FS = Fsref/5 110 => DAC FS = Fsref/5.5 111 => DAC FS = Fsref/6 Note: Fsref is set between 39 kHz or 53kHz
D2–D0	ADCFS	R/W	000	ADC Sampling Rate 000 => ADC FS = Fsref/1 001 => ADC FS = Fsref/(1.5) 010 => ADC FS = Fsref/2 011 => ADC FS = Fsref/3 100 => ADC FS = Fsref/4 101 => ADC FS = Fsref/5 110 => ADC FS = Fsref/5.5 111 => ADC FS = Fsref/6 Note: Fsref is set between 39 kHz or 53kHz

REGISTER 01H: CODEC ADC Gain Control

BIT	NAME	READ/ WRITE	RESET VALUE	FUNCTION
D15	ADMUT	R/W	1	ADC Channel Mute 1 => ADC channel mute 0 => ADC channel not muted Note: If AGC is enabled then D15–D8 reflects gain being applied by AGC. If AGC is on the decoding for read values is as follows 01110111 => +59.5 dB 01110110 => +59.0 dB ––––– 00000000 => 0 dB ––––– 11101001 => –11.5 dB 11101000 => –12 dB
D14–D8	ADPGA	R/W	0000000	ADC PGA Settings 0000000 => ADC PGA = 0 dB 0000001 => ADC PGA = 0.5 dB 0000010 => ADC PGA = 1.0 dB ––––– 1110110 => ADC PGA = 59.0 dB 1110111 => ADC PGA = 59.5 dB 1111000 => ADC PGA = 59.5 dB ––––– 1111110 => ADC PGA = 59.5 dB 1111111 => ADC PGA = 59.5 dB Note: If AGC is enabled then D15–D8 reflects gain being applied by AGC. If AGC is on, the decoding for read values is as follows 01110111 => +59.5 dB 01110110 => +59.0 dB ––––– 00000000 => 0 dB ––––– 11101001 => –11.5 dB 11101000 => –12 dB
D7–D5	AGCTG	R/W	000	AGC Target Level. These three bits set the AGC's targeted ADC output level. 000 => –5.5 dB 001 => –8.0 dB 010 => –10 dB 011 => –12 dB 100 => –14 dB 101 => –17 dB 110 => –20 dB 111 => –24 dB

BIT	NAME	READ/ WRITE	RESET VALUE	FUNCTION
D4–D1	AGCTC	R/W	0000	AGC Time Constant. These four bits set the AGC attack and decay time constants. Time constants remain the same irrespective of any sampling frequency. **Attack time (ms) Decay time (ms)** 0000 8 100 0001 11 100 0010 16 100 0011 20 100 0100 8 200 0101 11 200 0110 16 200 0111 20 200 1000 8 400 1001 11 400 1010 16 400 1011 20 400 1100 8 500 1101 11 500 1110 16 500 1111 20 500
D0	AGCEN	R/W	0	AGC Enable 0 => AGC is off (ADC PGA is controlled by D15–D8 ADC PGA Control) 1 => AGC is on (ADC PGA is controlled by AGC)

REGISTER 02H: CODEC DAC Gain Control

BIT	NAME	READ/ WRITE	RESET VALUE	FUNCTION
D15	DALMU	R/W	1	DAC Left Channel Mute 1 => DAC left channel muted 0 => DAC left channel not muted
D14–D8	DALVL	R/W	1111111	DAC Left Channel Volume Control 0000000 => DAC left channel volume control = 0 dB 0000001 => DAC left channel volume control = –0.5 dB 0000010 => DAC left channel volume control = –1.0 dB ––––– 1111110 => DAC left channel volume control = –63.0 dB 1111111 => DAC left channel volume control = –63.5 dB
D7	DARMU	R/W	1	DAC Right Channel Mute 1 => DAC right channel muted 0 => DAC right channel not muted
D6–D0	DARVL	R/W	1111111	DAC Right Channel Volume Control 0000000 => DAC right channel volume control = 0 dB 0000001 => DAC right channel volume control = –0.5 dB 0000010 => DAC right channel volume control = –1.0 dB ––––– 1111110 => DAC right channel volume control = –63.0 dB 1111111 => DAC right channel volume control = –63.5 dB

REGISTER 03H: CODEC Sidetone Control

BIT	NAME	READ/ WRITE	RESET VALUE	FUNCTION
D15	ASTMU	R/W	1	Analog Sidetone Mute Control 1 => Analog sidetone mute 0 => Analog sidetone not muted
D14–D8	ASTG	R/W	1000101	Analog Sidetone Gain Setting 0000000 => Analog sidetone gain setting = –34.5dB 0000001 => Analog sidetone gain setting = –34dB 0000010 => Analog sidetone gain setting = –33.5dB ––––– 1000101 => Analog sidetone gain setting = 0dB 1000110 => Analog sidetone gain setting = 0.5dB ––––– 1011100 => Analog sidetone gain setting = 11.5dB 1011101 => Analog sidetone gain setting = 12dB 1011110 => Analog sidetone gain setting = 12dB 1011111 => Analog sidetone gain setting = 12dB ––––– 11xxxxx => Analog sidetone gain setting = 12dB
D7	DSTMU	R/W	1	Digital Sidetone Mute Control 1 => Digital sidetone muted 0 => Digital sidetone not muted
D6–D1	DSTG	R/W	000000	Digital Sidetone Setting 000000 => Digital sidetone gain = 0dB 000001 => Digital sidetone gain = –1.5dB 000010 => Digital sidetone gain = –3.0dB ––––– 1xxxxx => Digital sidetone gain = –48dB Note: Digital sidetone setting applied at zero cross over
D0	ASTGF	R	0	Analog Sidetone PGA Flag (Read Only) 0 => Gain applied /= PGA register setting 1 => PGA applied = PGA register setting. Note: Analog sidetone gain is implemented at zero crossings of the signal.

REGISTER 04H: Audio Control 2

BIT	NAME	READ/ WRITE	RESET VALUE	FUNCTION
D15	KCLEN	R/W	0	Keyclick Enable 0 => Keyclick disabled 1 => Keyclick enabled Note: This bit is automatically cleared after giving out the keyclick signal length equal to the programmed value.
D14–D12	KCLAC	R/W	100	Keyclick Amplitude Control 000 => Lowest amplitude 100 => Medium amplitude 111 => Highest amplitude
D11	APGASS	R/W	0	ADC Channel PGA Soft-stepping control 0 => 0.5dB change every ADWS 1 => 0.5dB change every 2 ADWS Note: When AGC is enabled, this bit is read only. The read values indicate the following 0 => signal power greater than noise threshold 1 => signal power is less than noise threshold
D10–D8	KCLFRQ	R/W	100	Keyclick Frequency 000 => 62.5Hz 001 => 125Hz 010 => 250Hz 011 => 500Hz 100 => 1kHz 101 => 2kHz 110 => 4kHz 111 => 8kHz
D7–D4	KCLLN	R/W	0001	Keyclick Length 0000 => 2 periods key click 0001 => 4 periods key click 0010 => 6 periods key click ––––– 1110 => 30 periods key click 1111 => 32 periods key click
D3	DLGAF	R	0	DAC Left Channel PGA Flag (Read Only) 0 => Gain applied /= PGA register setting 1 => Gain applied = PGA register setting. Note: This flag indicates when the soft-stepping for DAC left channel is completed
D2	DRGAF	R	0	DAC Right Channel PGA Flag (Read Only) 0 => Gain applied /= PGA register setting 1 => Gain applied = PGA register setting. Note: This flag indicates when the soft-stepping for DAC right channel is completed
D1	DASTC	R/W	0	DAC Channel PGA Soft-stepping control 0 => 0.5dB change every LRCK 1 => 0.5dB change every 2 LRCK
D0	ADGAF	R	0	ADC Channel PGA Flag (Read Only) 1 => Gain applied = PGA register setting. 0 => Gain applied /= PGA register setting Note: This flag indicates when the soft-stepping for ADC channel is completed. When AGC is enabled the read value of this bit indicates the following 0 => AGC is not saturated. 1 => AGC is saturated.

REGISTER 05H: CODEC Power Control

BIT	NAME	READ/ WRITE	RESET VALUE	FUNCTION
D15	PWDNC	R/W	1	Codec Power-Down Control 0 => Codec powered up 1 => Codec powered down
D14		R	0	Reserved (During read the value of this bit is 0. Write only 0 into this location.)
D13	ASTPWD	R/W	1	Analog Sidetone Power-down Control 0 => Analog sidetone powered up 1 => Analog sidetone powered down
D12	DAODRC	R/W	0	Audio Output Driver Control 0 => Output driver in low power mode. 1 => Output driver in high power mode.
D11	ASTPWF	R	1	Analog Sidetone Power-Down Flag 0 => Analog sidetone powered down is not complete. 1 => Analog sidetone powered down is complete.
D10	DAPWDN	R/W	1	DAC Power-Down Control 0 => Power up the DAC 1 => Power down the DAC
D9	ADPWDN	R/W	1	ADC Power-Down Control 0 => Power up the ADC 1 => Power down the ADC
D8	VGPWDN	R/W	1	Driver Virtual Ground Power Down 0 => Power up the VGND amp 1 => Power down the VGND amp
D7	ADPWDF	R	1	ADC Power-Down Flag 0 => ADC power down is not complete 1 => ADC power down is complete
D6	DAPWDF	R	1	DAC Power-Down Flag (See DAC Powerdown section of this data sheet) 0 => DAC power down is not complete 1 => DAC power down is complete
D5	ADWSF	R/W	0	ADWS Pin Function 0 => ADWS pin acts as hardware power down. 1 => ADWS pin acts as ADC Word–Select. Note: ADWS pin should be programmed as hardware power down only if the ADC channel is powered down or both the ADC and DAC channels have the same sampling rate. If both the ADC and DAC channels have the same sampling rates then LRCK can act as a common word select signal for the ADC and DAC.
D4	VBIAS	R/W	0	VBIAS voltage 0 => VBIAS output = 2.5 V 1 => VBIAS output = 2.0 V
D3–D2		R	00	Reserved Write only 00 into this location.
D1	EFFCTL	R/W	0	Digital Audio Effects Filter Control 0 => Disable digital audio effects filter 1 => Enable digital audio effects filter
D0	DEEMPF	R/W	0	De–Emphasis Filter Enable 0 => Disable de-emphasis filter 1 => Enable de-emphasis filter

REGISTER 06H: Audio Control 3

BIT	NAME	READ/ WRITE	RESET VALUE	FUNCTION
D15–D14	DMSVOL	R/W	00	DAC Channel Master Volume Control 00 => Left channel and right channel have independent volume controls 01 => Left channel volume control is the programmed value of the right channel volume control. 10 => Right channel volume control is the programmed value of the left channel volume control. 11 => same as 00
D13	REFFS	R/W	0	Reference Sampling Rate. This setting controls the coefficients in the de-emphasis filter, the time-constants in AGC, and internal divider values that generate a clock for the touch screen/measurement ADC. If an Fsref above 48 kHz is being used, then it is recommended to set this to the 48-kHz setting, otherwise either setting can be used. 0 => Fsref = 48.0 kHz 1 => Fsref = 44.1 kHz
D12	DAXFM	R/W	0	Master Transfer Mode 0 => Continuous data transfer mode 1 => 256–s data transfer mode
D11	SLVMS	R/W	0	CODEC Master Slave Selection 0 => TSC2100 is slave codec 1 => TSC2100 is master codec
D10–D9	DAPK2PK	R/W	00	DAC Max Output Signal Swing and Common Mode Voltage 00 => DAC max output signal swing = 2.0 V, V_{CM} = 1.35 V 01 => DAC max output signal swing = 2.192 V (only recommended for analog supply of 3.0 V and digital supply of 1.65 V and above), V_{CM} = 1.48 V 10 => DAC max output signal swing = 2.402 V (only recommended for analog supply of 3.3 V and digital supply of 1.8 V and above), V_{CM} = 1.62 V 11 => DAC max output signal swing = 2.633 V (only recommended for analog supply of 3.6 V and digital supply of 1.95 V), V_{CM} = 1.78 V
D8	ADCOVF	R	0	ADC Channel Overflow Flag (Read Only) 0 => ADC channel data is within saturation limits 1 => ADC channel data has exceeded saturation limits. Note : This flag is reset only on register read.
D7	DALOVF	R	0	DAC Left Channel Overflow Flag (Read Only) 0 => DAC left channel data is within saturation limits 1 => DAC left channel data has exceeded saturation limits Note : This flag is reset only on register read.
D6	DAROVF	R	0	DAC Right Channel Overflow Flag (Read Only) 0 => DAC right channel data is within saturation limits 1 => DAC right channel data has exceeded saturation limits Note : This flag is reset only on register read.
D5–D4	AGCNL	R/W	00	AGC Noise Threshold. 00 => –60 dB 01 => –70 dB 10 => –80 dB 11 => –90 dB Note: AGC does not try to achieve the programmed ADC output levels if the input signal is below the programmed noise thresholds. This feature helps to avoid gaining up noise during silence periods.
D3	CLPST	R/W	0	AGC Clip Stepping Enable 0 => Not enabled 1 => Enabled
D2–D0	REVID	R	XXX	Reserved

REGISTER 07H: Digital Audio Effects Filter Coefficients

BIT	NAME	READ/ WRITE	RESET VALUE (IN DECIMAL)	FUNCTION
D15–D0	L_N0	R/W	27619	Left channel digital audio effects filter coefficient N0.

REGISTER 08H: Digital Audio Effects Filter Coefficients

BIT	NAME	READ/ WRITE	RESET VALUE (IN DECIMAL)	FUNCTION
D15–D0	L_N1	R/W	–27034	Left channel digital audio effects filter coefficient N1.

REGISTER 09H: Digital Audio Effects Filter Coefficients

BIT	NAME	READ/ WRITE	RESET VALUE (IN DECIMAL)	FUNCTION
D15–D0	L_N2	R/W	26461	Left channel digital audio effects filter coefficient N2.

REGISTER 0AH: Digital Audio Effects Filter Coefficients

BIT	NAME	READ/ WRITE	RESET VALUE (IN DECIMAL)	FUNCTION
D15–D0	L_N3	R/W	27619	Left channel digital audio effects filter-coefficient N3.

REGISTER 0BH: Digital Audio Effects Filter Coefficients

BIT	NAME	READ/ WRITE	RESET VALUE (IN DECIMAL)	FUNCTION
D15–D0	L_N4	R/W	–27034	Left channel digital audio effects filter-coefficient N4.

REGISTER 0CH: Digital Audio Effects Filter Coefficients

BIT	NAME	READ/ WRITE	RESET VALUE (IN DECIMAL)	FUNCTION
D15–D0	L_N5	R/W	26461	Left channel digital audio effects filter-coefficient N5.

REGISTER 0DH: Digital Audio Effects Filter Coefficients

BIT	NAME	READ/ WRITE	RESET VALUE (IN DECIMAL)	FUNCTION
D15–D0	L_D1	R/W	32131	Left channel digital audio effects filter-coefficient D1.

REGISTER 0EH: Digital Audio Effects Filter Coefficients

BIT	NAME	READ/ WRITE	RESET VALUE (IN DECIMAL)	FUNCTION
D15–D0	L_D2	R/W	–31506	Left channel digital audio effects filter-coefficient D2.

REGISTER 0FH: Digital Audio Effects Filter Coefficients

BIT	NAME	READ/ WRITE	RESET VALUE (IN DECIMAL)	FUNCTION
D15–D0	L_D4	R/W	32131	Left channel digital audio effects filter-coefficient D4.

REGISTER 10H: Digital Audio Effects Filter Coefficients

BIT	NAME	READ/ WRITE	RESET VALUE (IN DECIMAL)	FUNCTION
D15–D0	L_D5	R/W	–31506	Left channel digital audio effects filter-coefficient D5.

REGISTER 11H: Digital Audio Effects Filter Coefficients

BIT	NAME	READ/ WRITE	RESET VALUE (IN DECIMAL)	FUNCTION
D15–D0	R_N0	R/W	27619	Right channel digital audio effects filter-coefficient N0.

REGISTER 12H: Digital Audio Effects Filter Coefficients

BIT	NAME	READ/ WRITE	RESET VALUE (IN DECIMAL)	FUNCTION
D15–D0	R_N1	R/W	–27034	Right channel digital audio effects filter-coefficient N1.

REGISTER 13H: Digital Audio Effects Filter Coefficients

BIT	NAME	READ/ WRITE	RESET VALUE (IN DECIMAL)	FUNCTION
D15–D0	R_N2	R/W	26461	Right channel digital audio effects filter-coefficient N2.

REGISTER 14H: Digital Audio Effects Filter Coefficients

BIT	NAME	READ/ WRITE	RESET VALUE (IN DECIMAL)	FUNCTION
D15–D0	R_N3	R/W	27619	Right channel digital audio effects filter-coefficient N3.

REGISTER 15H: Digital Audio Effects Filter Coefficients

BIT	NAME	READ/ WRITE	RESET VALUE (IN DECIMAL)	FUNCTION
D15–D0	R_N4	R/W	–27034	Right channel digital audio effects filter-coefficient N4.

REGISTER 16H: Digital Audio Effects Filter Coefficients

BIT	NAME	READ/ WRITE	RESET VALUE (IN DECIMAL)	FUNCTION
D15–D0	R_N5	R/W	26461	Right channel digital audio effects filter-coefficient N5.

REGISTER 17H: Digital Audio Effects Filter Coefficients

BIT	NAME	READ/ WRITE	RESET VALUE (IN DECIMAL)	FUNCTION
D15–D0	R_D1	R/W	32131	Right channel digital audio effects filter-coefficient D1.

REGISTER 18H: Digital Audio Effects Filter Coefficients

BIT	NAME	READ/ WRITE	RESET VALUE (IN DECIMAL)	FUNCTION
D15–D0	R_D2	R/W	–31506	Right channel digital audio effects filter-coefficient D2.

REGISTER 19H: Digital Audio Effects Filter Coefficients

BIT	NAME	READ/ WRITE	RESET VALUE (IN DECIMAL)	FUNCTION
D15–D0	R_D4	R/W	32131	Right channel digital audio effects filter coefficient D4.

REGISTER 1AH: Digital Audio Effects Filter Coefficients

BIT	NAME	READ/ WRITE	RESET VALUE (IN DECIMAL)	FUNCTION
D15–D0	R_D5	R/W	–31506	Right channel digital audio effects filter coefficient D5.

REGISTER 1BH: PLL Programmability

BIT	NAME	READ/ WRITE	RESET VALUE	FUNCTION
D15	PLLSEL	R/W	0	PLL Enable 0 => Disable PLL 1 => Enable PLL
D14–D11	QVAL	R/W	0010	Q value. Valid only if PLL is disabled. 0000 => 16 0001 => 17 0010 => 2 0011 => 3 ––––– 1100 => 12 1101 => 13 1110 => 14 1111 => 15
D10–D8	PVAL	R/W	000	P value. Valid when PLL is enabled 000 => 8 001 => 1 010 => 2 011 => 3 100 => 4 101 => 5 110 => 6 111 => 7
D7–D2	JVAL	R/W	000001	J value. Valid only if PLL is enabled. 000000 => Not valid 000001 => 1 000010 => 2 ––––– 111110 => 62 111111 => 63
D1–D0	Reserved	R	00	Reserved (write only 00)

REGISTER 1CH: PLL Programmability

BIT	NAME	READ/ WRITE	RESET VALUE	FUNCTION
D15–D2	DVAL	R/W	0 (in decimal)	D value. Used when PLL is enabled. D value is valid from 0000 to 9999 in decimal. Programmed value greater than 9999 is treated as 9999 00000000000000 => 0 decimal 00000000000001 => 1 decimal
D1–D0	Reserved	R	00	Reserved (write only 00)

REGISTER 1DH: Audio Control 4

BIT	NAME	READ/ WRITE	RESET VALUE	FUNCTION
D15	ASTPD	R/W	0	ADC PGA Soft-Stepping Control 0 => Soft-stepping enabled 1 => Soft-stepping disabled
D14	DASTPD	R/W	0	DAC PGA Soft-Stepping Control 0 => Soft-stepping enabled 1 => Soft-stepping disabled
D13	ASSTPD	R/W	0	Analog Sidetone Soft-Stepping Control 0 => Soft-stepping enabled 1 => Soft-stepping disabled
D12	DSTPD	R/W	0	Digital Sidetone Zero Cross Control 0 => Zero cross enabled 1 => Zero cross disabled
D11	Reserved	R	0	Reserved
D10–D9	AGC_HYST	R/W	00	AGC Hysteresis Control 00 =>1 dB hysteresis 01 => 2 dB hysteresis 10 => 4 dB hysteresis 11 => No hysteresis
D8	SHCKT_DIS	R/W	0	Disable Short Circuit Detection 0 => Short circuit detection enabled 1 => Short circuit detection disabled
D7	SHCKT_PD	R/W	0	Power down drivers if Short Circuit Detected 0 => No auto power down of drivers on short circuit. 1 => Auto power down drivers on short circuit.
D6	SHCKT_FLAG	R	0	Short Circuit Detected Flag 0 => Short circuit not detected 1 => Short circuit detected
D5	DAC_POP_RED	R	0	DAC POP Reduction Enable 0 => Disable POP reduction 1 => Enable POP reduction
D4	DAC_POP_RED_ SET1	R/W	0	DAC POP reduction setting 1 0 => Fast setting 1 => Slow setting
D3–D2	DAC_POP_RED_ SET2	R/W	00	DAC POP reduction setting 2 00 => Long setting 11 => Short setting
D1–D0	PGID	R	XX	

REGISTER 1EH: Audio Control 5

BIT	NAME	READ/ WRITE	RESET VALUE	FUNCTION
D15–D9	MAX_AGC_PGA	R/W	1111111	MAX ADC PGA applicable for AGC 0000000 => 0 dB 0000001 => 0.5 dB 0000010 => 1.0 dB ––––– 1110110 => 59.0 dB 1110111 => 59.5 dB 1111000 => 59.5 dB ––––– 1111111 => 59.5 dB
D8–D6	AGC_NOI_DEB	R/W	000	AGC Debounce time for speech mode to silence mode transition 000 => 0 ms 001 => 0.5 ms 010 => 1.0 ms ––––– 110 => 16.0 ms 111 => 32.0 ms
D5–D3	AGC_SIG_DEB	R/W	000	AGC Debounce time for silence mode to speech mode transition 000 => 0 ms 001 => 0.5 ms 010 => 1.0 ms ––––– 110 => 16.0 ms 111 => 32.0 ms
D2	DRV_POP_DIS	R/W	0	Audio Output Driver POP reduction enable 0 => Enabled 1 => Disabled
D1	DRV_POP_LEN	R/W	0	Audio Output Driver POP reduction duration 0 => Output driver ramps to final voltage in approximately 1 msec, if VGND is powered (0.8 sec otherwise) 1 => Output driver ramps to final voltage in approximately 5 msec, if VGND is powered (4 sec otherwise)
D0	Reserved	R	0	Reserved. Do not write 1 to this location.

LAYOUT

The following layout suggestions should provide optimum performance from the TSC2100. However, many portable applications have conflicting requirements concerning power, cost, size, and weight. In general, most portable devices have fairly *clean* power and grounds because most of the internal components are very low power. This situation means less bypassing for the converter power and less concern regarding grounding. Still, each situation is unique and the following suggestions should be reviewed carefully.

For optimum performance, care must be taken with the physical layout of the TSC2100 circuitry. The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to latching the output of the analog comparator. Therefore, during any single conversion for an *n-bit* SAR converter, there are *n windows* in which large external transient voltages can easily affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, and high power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. The error can change if the external event changes in time with respect to the timing of the critical *n windows*.

With this in mind, power to the TSC2100 must be clean and well bypassed. A 0.1-μF ceramic bypass capacitor must be placed as close to the device as possible. A 1-μF to 10-μF capacitor may also be needed if the impedance between the TSC2100 supply pins and the system power supply is high.

A bypass capacitor on the VREF pin is generally not needed because the reference is buffered by an internal op-amp, although it can be useful to reduce reference noise level. If an external reference voltage originates from an op-amp, make sure that it can drive any bypass capacitor that is used without oscillation.

The TSC2100 architecture offers no inherent rejection of noise or voltage variation in regards to using an external reference input. This is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply appears directly in the digital results. While high frequency noise can be filtered out, voltage variation due to line frequency (50 Hz or 60 Hz) can be difficult to remove.

The ground pins must be connected to a clean ground point. In many cases, this is the *analog* ground. Avoid connections which are too near the grounding point of a microcontroller or digital signal processor. If needed, run a ground trace directly from the converter to the power supply entry or battery connection point. The ideal layout includes an analog ground plane dedicated to the converter and associated analog circuitry.

In the specific case of use with a resistive touch screen, care must be taken with the connection between the converter and the touch screen. Since resistive touch screens have fairly low resistance, the interconnection must be as short and robust as possible. Loose connections can be a source of error when the contact resistance changes with flexing or vibrations.

As indicated previously, noise can be a major source of error in touch-screen applications (e.g., applications that require a back-lit LCD panel). This EMI noise can be coupled through the LCD panel to the touch screen and cause *flickering* of the converted ADC data. Several things can be done to reduce this error, such as utilizing a touch screen with a bottom-side metal layer connected to ground. This couples the majority of noise to ground. Additionally, filtering capacitors, from Y+, Y–, X+, and X– to ground, can also help. Note, however, that the use of these capacitors increases screen settling time and requires longer panel voltage stabilization times, as well as increased precharge and sense times for the $\overline{\text{PINTDAV}}$ circuitry of the TSC2100.

CONVERSION TIME CALAULATIONS FOR THE TSC2100

Touch Screen Conversion Initiated At Touch Detect

The time needed to get a converted X/Y coordinate for reading can be calculated by (not including the time needed to send the command over the SPI bus):

$$t_{coordinate} = 2 \times \left[\frac{\left(t_{PRE} + t_{SNS} + t_{PVS}\right)}{125\ ns}\right] \times t_{OSC} + 2 \times \left\{N_{AVG}\left[\left(N_{BITS} + 1\right) \times \frac{8\ MHz}{f_{conv}} + n_1 + 12\right] + 1\right\}$$

$$\times t_{OSC} + 18 \times t_{OSC} + n_2 \times t_{OSC} + n_3 \times t_{OSC}$$

where:

$t_{coordinate}$ = time to convert X/Y coordinate

t_{PVS} = Panel voltage stabilization time

t_{PRE} = precharge time

t_{SNS} = sense time

N_{AVG} = number of averages; for no averaging, $N_{AVG} = 1$

N_{BITS} = number of bits of resolution

f_{conv} = A/D converter clock frequency

t_{OSC} = Oscillator clock period

n_1 = 6 ; if $f_{conv} = 8$ MHz

7 ; if $f_{conv} \neq 8$ MHz

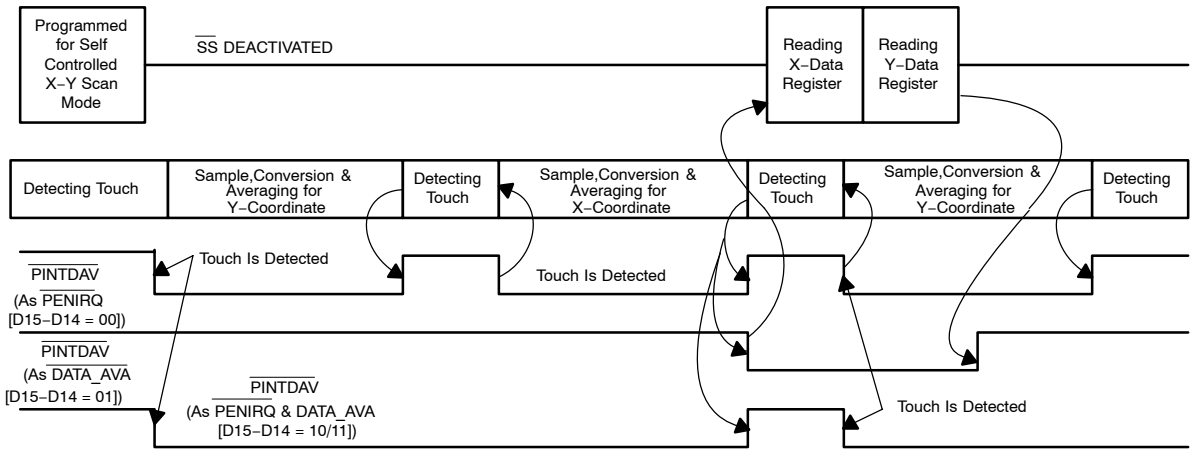
n_2 = 4 ; if $t_{PVS} = 0\ \mu s$

0 ; if $t_{PVS} \neq 0\ \mu s$

n_3 = 0 ; if $t_{SNS} = 32\ \mu s$

2 ; if $t_{SNS} \neq 32\ \mu s$

NOTE: The above formula is exactly valid only when the codec is powered down. Also, after touch detect, the formula holds true from second conversion onwards.



The time for a complete X/Y/Z1/Z2 coordinate conversion is given by(not including the time needed to send the command over the SPI bus):

$$t_{coordinate} = 3 \times \left[\frac{\left(t_{PRE} + t_{SNS} + t_{PVS}\right)}{125\ ns}\right] \times t_{OSC} + 4 \times \left\{N_{AVG}\left[\left(N_{BITS} + 1\right) \times \frac{8\ MHz}{f_{conv}} + n_1 + 12\right] + 1\right\}$$

$$\times t_{OSC} + 33 \times t_{OSC} + n_2 \times t_{OSC} + n_3 \times t_{OSC}$$

n_1 = 6 ; if f_{conv} = 8 MHz

7 ; if $f_{conv} \neq$ 8 MHz

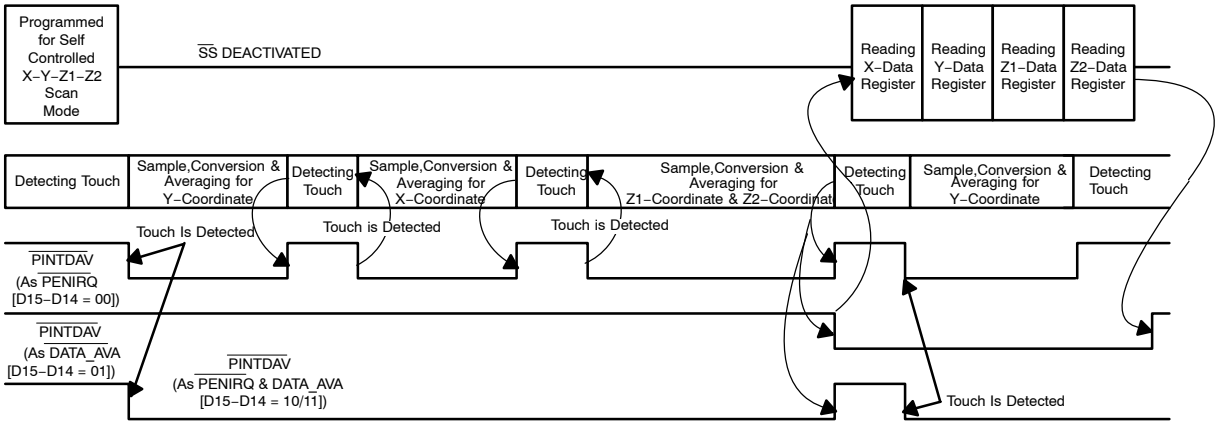
n_2 = 4 ; if t_{PVS} = 0 µs

0 ; if $t_{PVS} \neq$ 0 µs

n_3 = 0 ; if t_{SNS} = 32 µs

3 ; if $t_{SNS} \neq$ 32 µs

NOTE: The above formula is exactly valid only when the codec is powered down. Also after touch detect the formula holds true from second conversion onwards.



NOTE: If the $\overline{PINTDAV}$ signal is programmed to be used for pen-interrupt by setting bits D15–D14 of REG01H/Page–2 to either *00*, *01*, or *11*, then the high duration of $\overline{PINTDAV}$ is given by:

$$\frac{\left(t_{PRE} + t_{SNS}\right) \times t_{OSC}}{125\ ns}$$

Touch Screen Conversion Initiated by the Host

The time needed to convert any single coordinate either X or Y under host control (not including the time needed to send the command over the SPI bus) is given by:

$$t_{coordinate} = \left[\frac{\left(t_{PVS}\right)}{125\ ns}\right] \times t_{OSC} + \left\{N_{AVG}\left[\left(N_{BITS} + 1\right) \times \frac{8\ MHz}{f_{conv}} + n_1 + 12\right] + 1\right\}$$

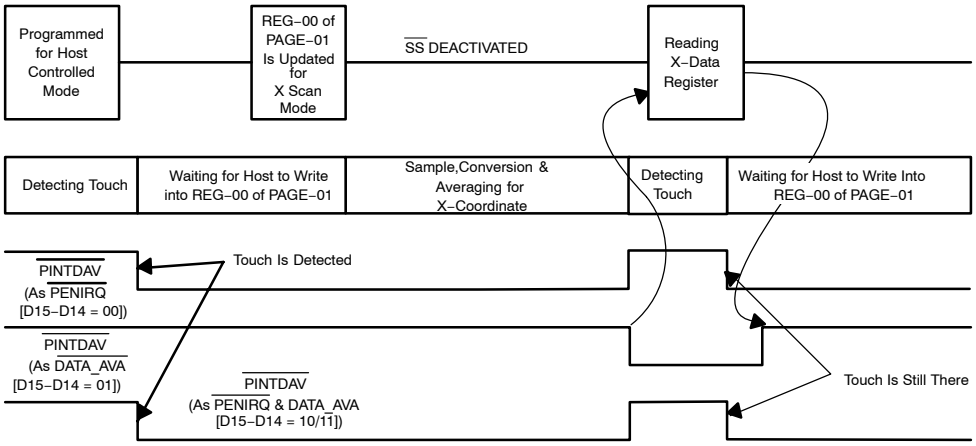
$$\times t_{OSC} + 14 \times t_{OSC} + n_2 \times t_{OSC}$$

n_1 = 6 ; if f_{conv} = 8 MHz

7 ; if $f_{conv} \neq$ 8 MHz

n_2 = 2 ; if t_{PVS} = 0 µs

0 ; if $t_{PVS \neq}$ 0 µs



The time needed to convert the Z coordinate under host control (not including the time needed to send the command over the SPI bus) is given by:

$$t_{coordinate} = \left[\frac{\left(t_{PVS}\right)}{125\ ns}\right] \times t_{OSC} + 2 \times \left\{N_{AVG}\left[\left(N_{BITS} + 1\right) \times \frac{8\ MHz}{f_{conv}} + n_1 + 12\right] + 1\right\}$$

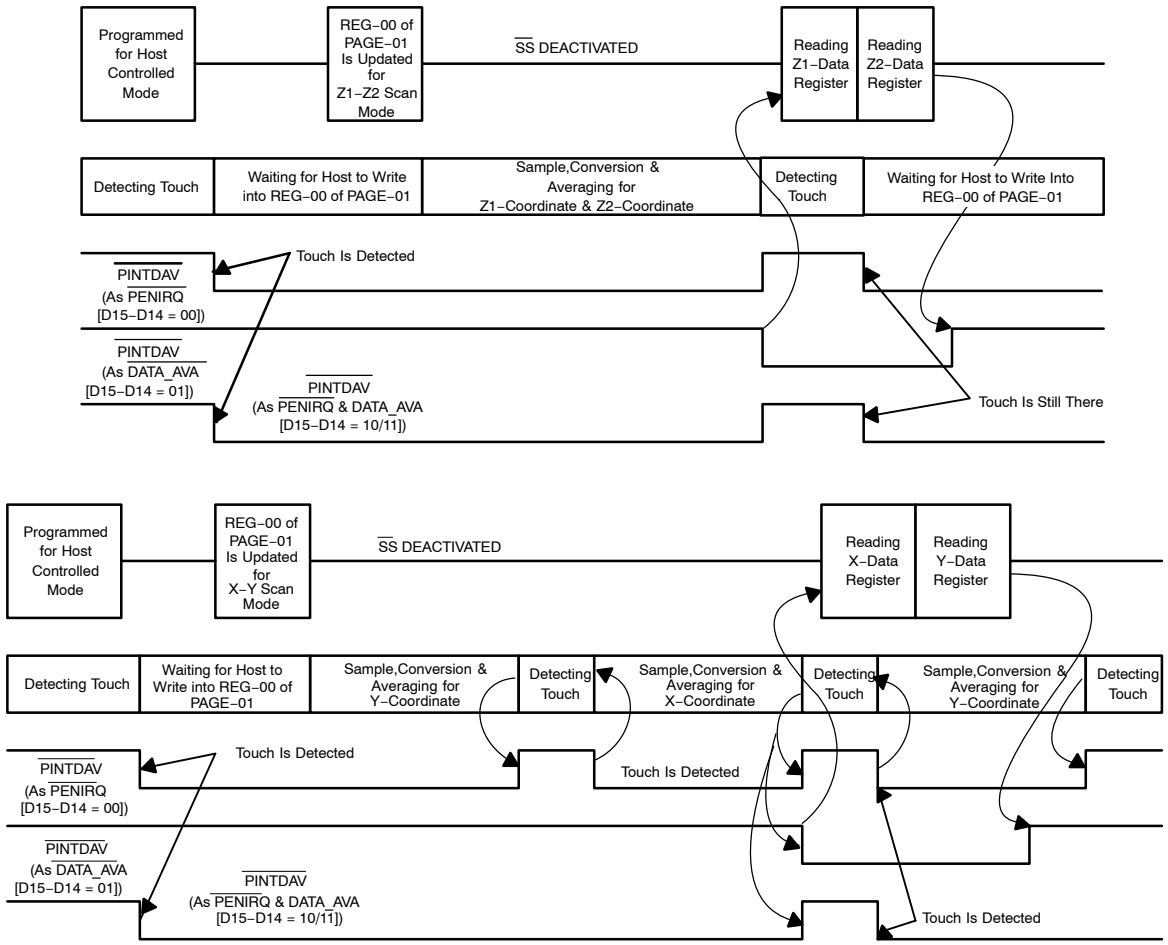
$$\times t_{OSC} + 20 \times t_{OSC} + n_2 \times t_{OSC}$$

n_1 = 6 ; if f_{conv} = 8 MHz

7 ; if $f_{conv} \neq$ 8 MHz

n_2 = 2 ; if t_{PVS} = 0 µs

0 ; if $t_{PVS \neq}$ 0 µs



NOTE: If the $\overline{\text{PINTDAV}}$ signal is programmed to be used for pen-interrupt by setting bits D15–D14 of REG01H/Page–2 to either *00*, *01*, or *11*, then the high duration of $\overline{\text{PINTDAV}}$ is given by:

$$\frac{\left(t_{PRE} + t_{SNS}\right) \times t_{OSC}}{125\ ns}$$

Non-Touch Screen Measurement Operation

The time needed to make temperature, auxiliary, or battery measurements is given by:

$$t = \left\{ N_{AVG}\left[\left(N_{BITS} + 1\right) \times \frac{8\ MHz}{f_{conv}} + n_1 + n_2 \right] + 1 \right\} \times t_{OSC} + 15 \times t_{OSC} + n_3 \times t_{OSC}$$

where:

n_1 = 6 ; if f_{conv} = 8 MHz

7 ; if $f_{conv} \neq$ 8 MHz

n_2 = 24 ; if measurement is for TEMP1 case

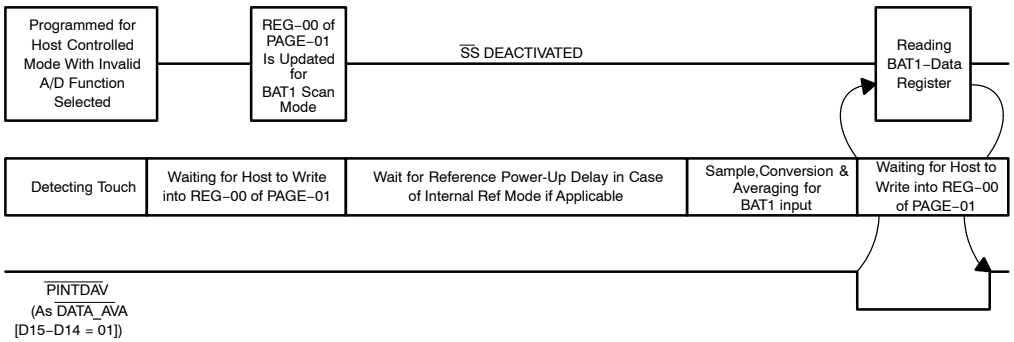
12 ; if measurement is for other than TEMP1 case

n_3 = 0 ; if external reference mode is selected

3 ; if t_{REF} = 0 μs or reference is programmed for power up all the time.

1 + t_{REF} /125 ns; if $t_{REF} \neq$ 0 μs and reference needs to power down between conversions.

t_{REF} is the reference power up delay time.



The time needed for continuous AUX conversion in scan mode is given by:

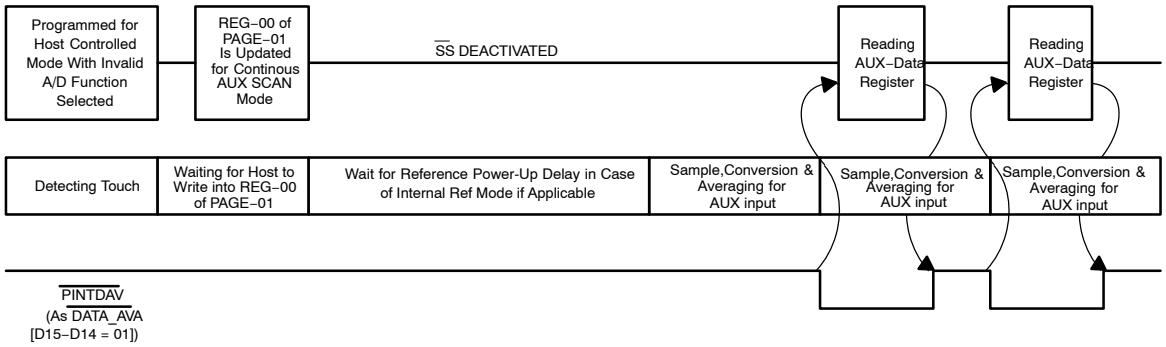
$$t = \left\{ N_{AVG} \left[\left(N_{BITS} + 1 \right) \times \frac{8\ MHz}{f_{conv}} + n_1 + 12 \right] + 1 \right\} \times t_{OSC} + 8 \times t_{OSC}$$

where:

n_1 = 6 ; if f_{conv} = 8 MHz

7 ; if $f_{conv} \neq$ 8 MHz

NOTE: The above equation is valid only from second conversion onwards.



Port Scan Operation

The time needed to complete one set of port scan conversions is given by:

$$t = 3 \times \left\{ N_{AVG} \left[\left(N_{BITS} + 1 \right) \times \frac{8\ MHz}{f_{conv}} + n_1 + 12 \right] + 1 \right\} \times t_{OSC} + 31 \times t_{OSC} + n_2 \times t_{OSC}$$

where:

n_1 = 6 ; if f_{conv} = 8 MHz

7 ; if $f_{conv} \neq$ 8 MHz

n_2 = 0 ; if external reference mode is selected

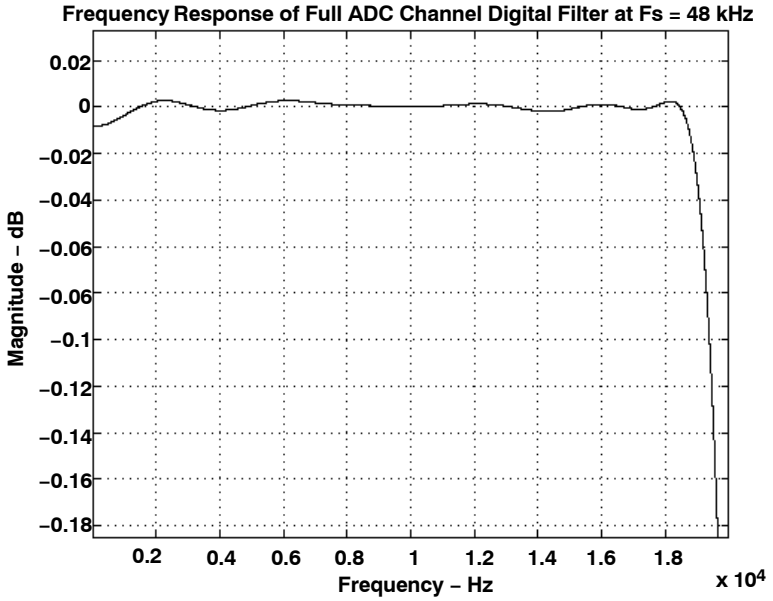
3 ; if t_{REF} = 0 μs or reference is programmed for power up all the times.

1 + t_{REF} /125 ns; if $t_{REF} \neq$ 0 μs and reference needs to power down between conversions.

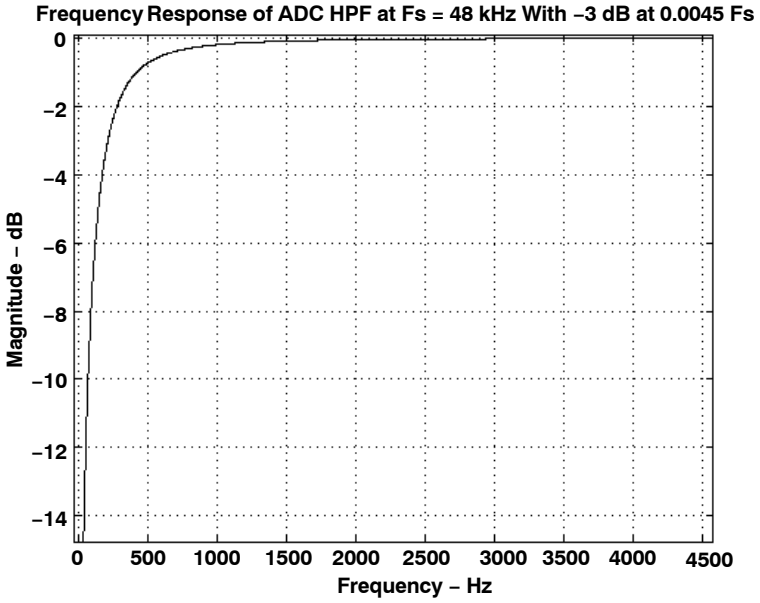
t_{REF} is the reference power up delay time.

AUDIO CODEC FILTER FREQUENCY RESPONSES

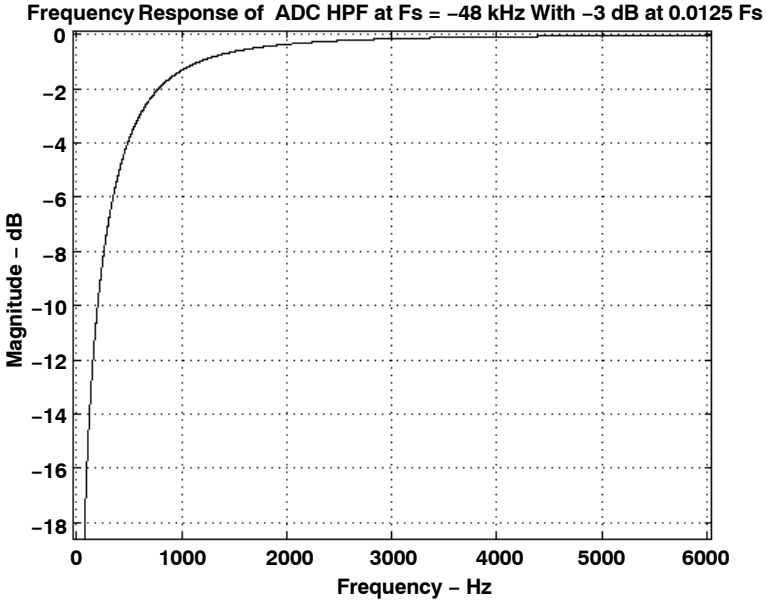
Pass-Band Frequency Response of ADC Digital Filter



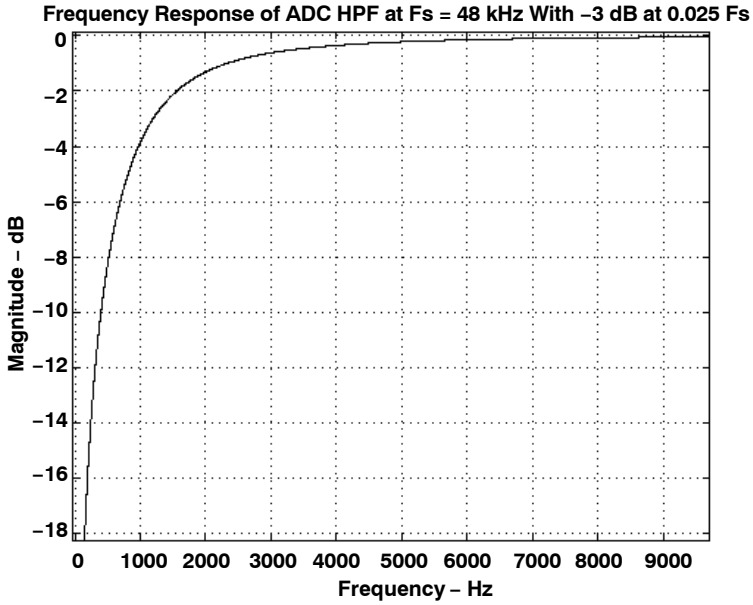
Frequency Response of ADC High-Pass Filter (Fcut-off = 0.0045 Fs)



Frequency Response of ADC High-Pass Filter (Fcut-off = 0.0125 Fs)

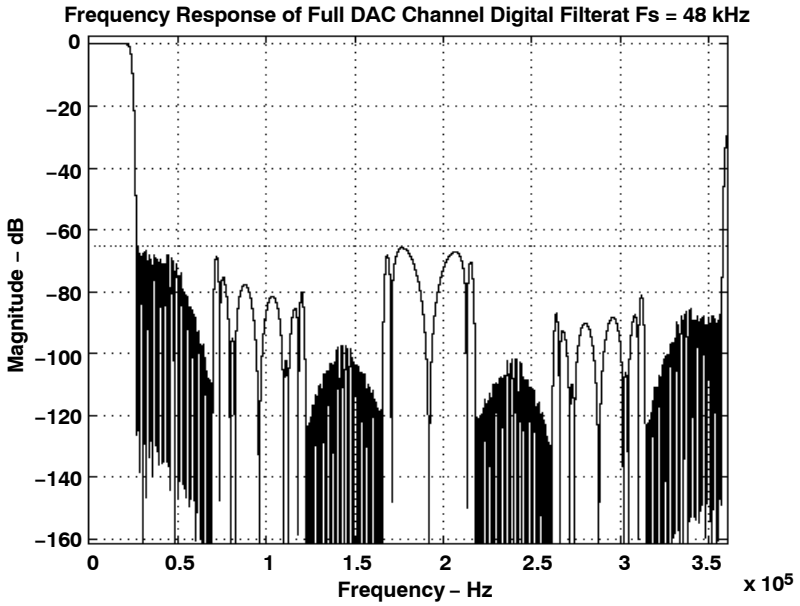


Frequency Response of ADC High-Pass Filter (Fcut-off = 0.025 Fs)

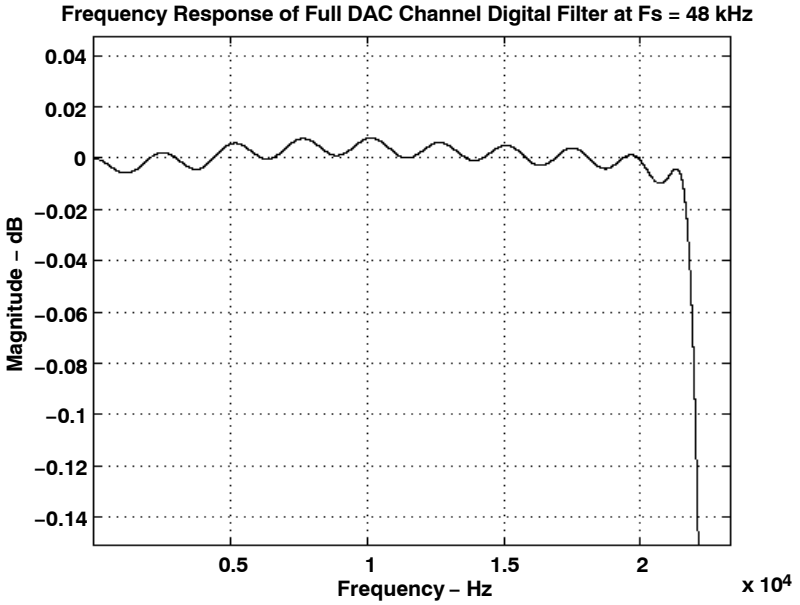


DAC CHANNEL DIGITAL FILTER

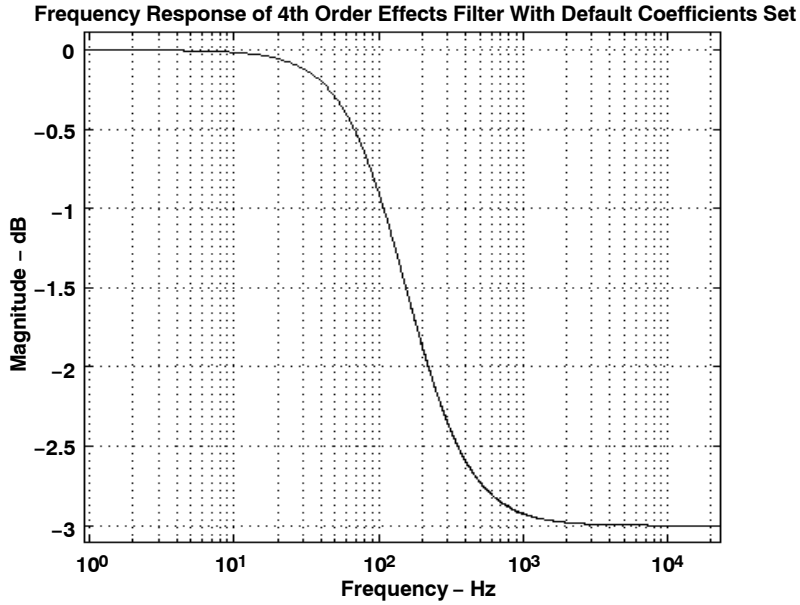
DAC Channel Digital Filter Frequency Response



DAC Channel Digital Filter Pass-Band Frequency Response

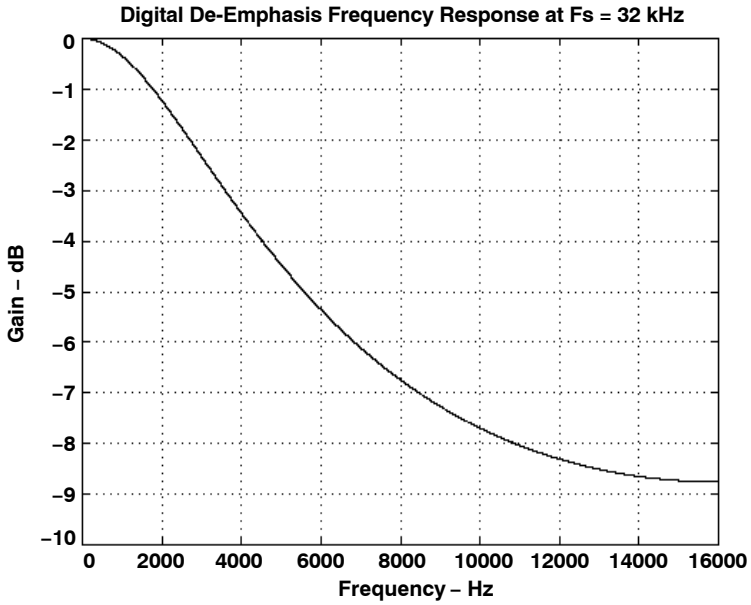


DEFAULT DIGITAL AUDIO EFFECTS FILTER RESPONSE AT 48 ksps

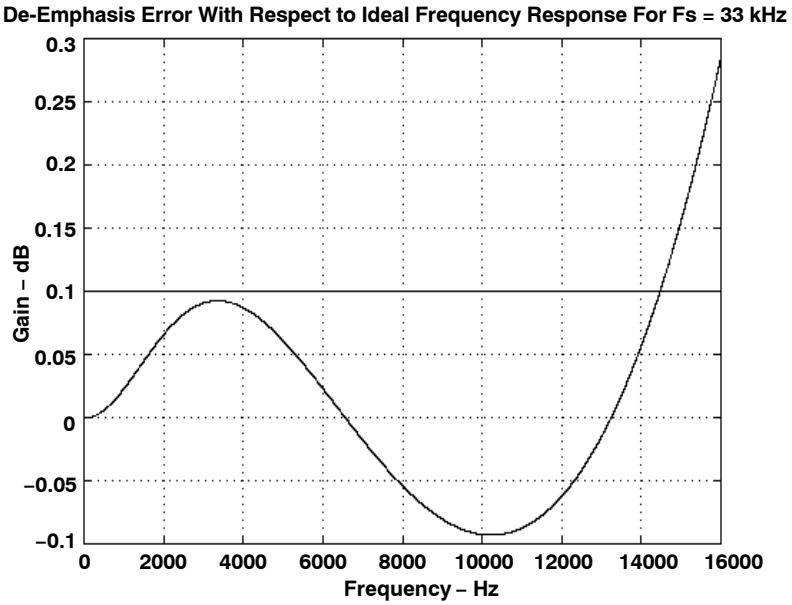


DE-EMPHASIS FILTER FREQUENCY RESPONSE

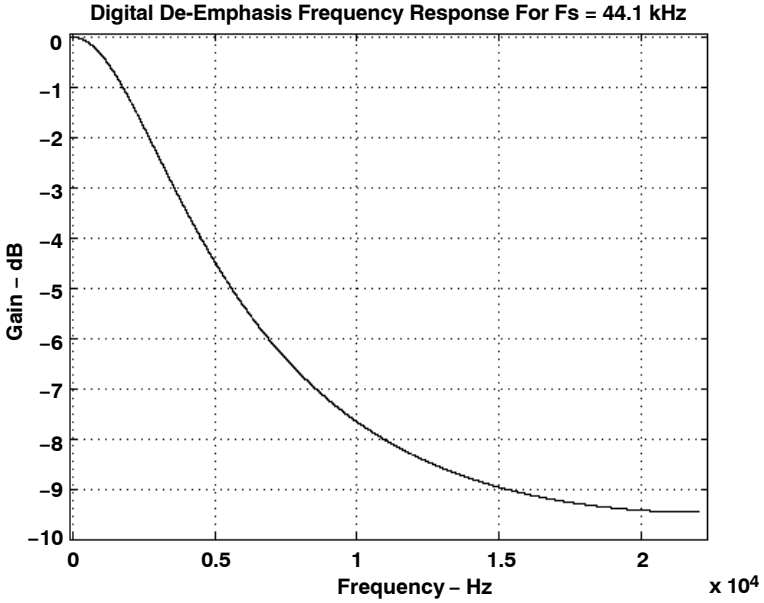
De-Emphasis Filter Response at 32 ksps



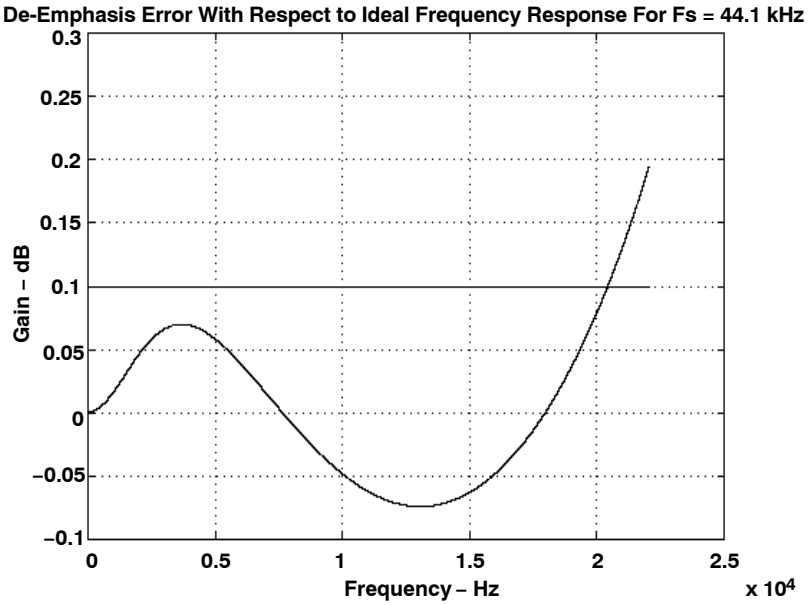
De-Emphasis Error at 32 ksps



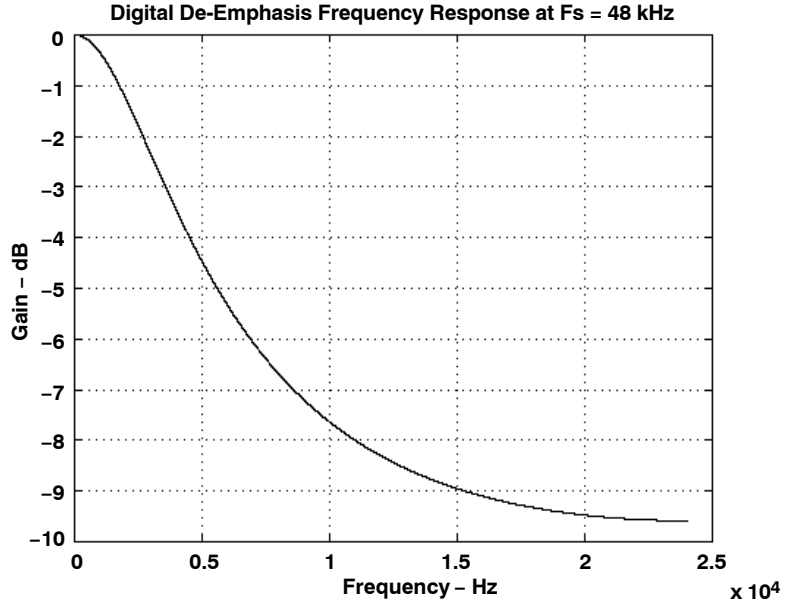
De-Emphasis Filter Frequency Response at 44.1 ksps



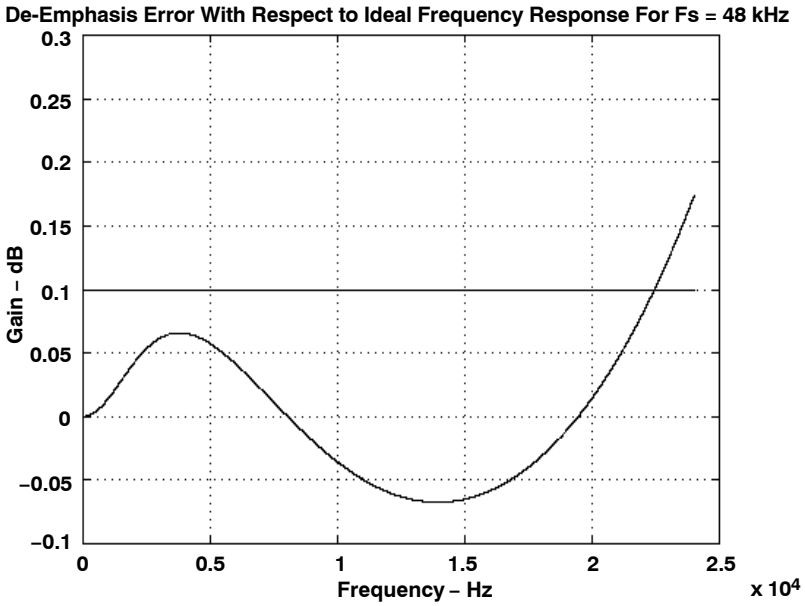
De-Emphasis Error at 44.1 ksps



De-Emphasis Frequency Response at 48 ksps



De-Emphasis Error at 48 ksps



PLL PROGRAMMING

The on-chip PLL in the TSC2100 can be used to generate sampling clocks from a wide range of MCLK's available in a system. The PLL works by generating oversampled clocks with respect to Fsref (44.1 kHz or 48 kHz). Frequency division generates all other internal clocks. The table below gives a sample programming for PLL registers for some standard MCLK's when PLL is required. Whenever the MCLK is of the form of N*128*Fsref (N=2,3…), PLL is not required.

Fsref = 44.1 kHz

MCLK (MHz)	P	J	D	ACHIEVED FSREF	% ERROR
2.8224	1	32	0	44100.00	0.0000
5.6448	1	16	0	44100.00	0.0000
12	1	7	5264	44100.00	0.0000
13	1	6	9474	44099.71	0.0007
16	1	5	6448	44100.00	0.0000
19.2	1	4	7040	44100.00	0.0000
19.68	1	4	5893	44100.30	–0.0007
48	4	7	5264	44100.00	0.0000

Fsref = 48 kHz

MCLK (MHz)	P	J	D	ACHIEVED FSREF	% ERROR
2.048	1	48	0	48000.00	0.0000
3.072	1	32	0	48000.00	0.0000
4.096	1	24	0	48000.00	0.0000
6.144	1	16	0	48000.00	0.0000
8.192	1	12	0	48000.00	0.0000
12	1	8	1920	48000.00	0.0000
13	1	7	5618	47999.71	0.0006
16	1	6	1440	48000.00	0.0000
19.2	1	5	1200	48000.00	0.0000
19.68	1	4	9951	47999.79	0.0004
48	4	8	1920	48000.00	0.0000

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TSC2100IDA	ACTIVE	TSSOP	DA	32	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TSC2100I	Samples
TSC2100IDAG4	ACTIVE	TSSOP	DA	32	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TSC2100I	Samples
TSC2100IRHB	ACTIVE	VQFN	RHB	32	73	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TSC 2100I	Samples
TSC2100IRHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TSC 2100I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

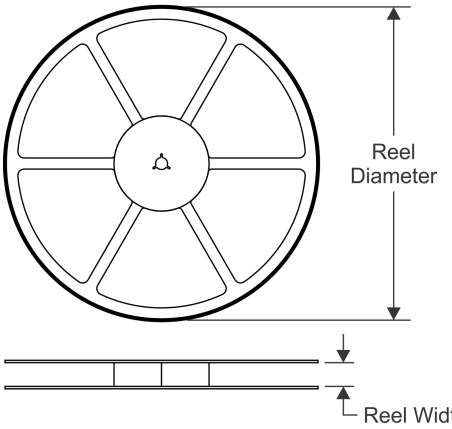
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

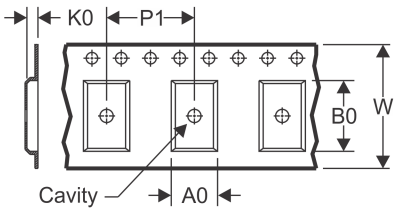
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

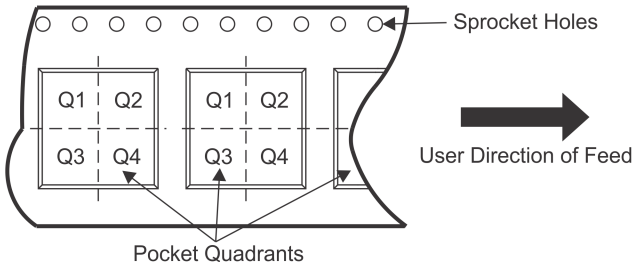


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

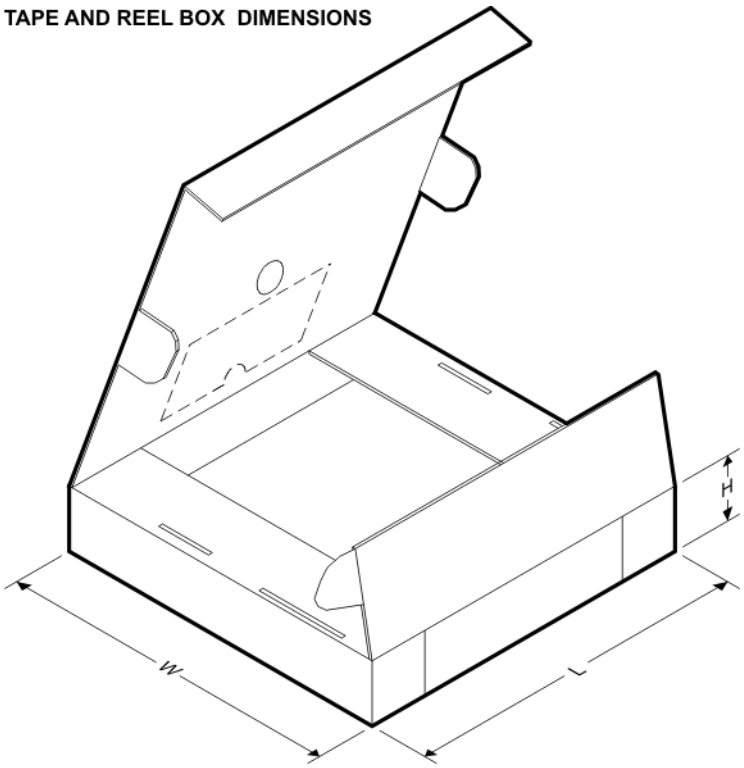
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TSC2100IRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

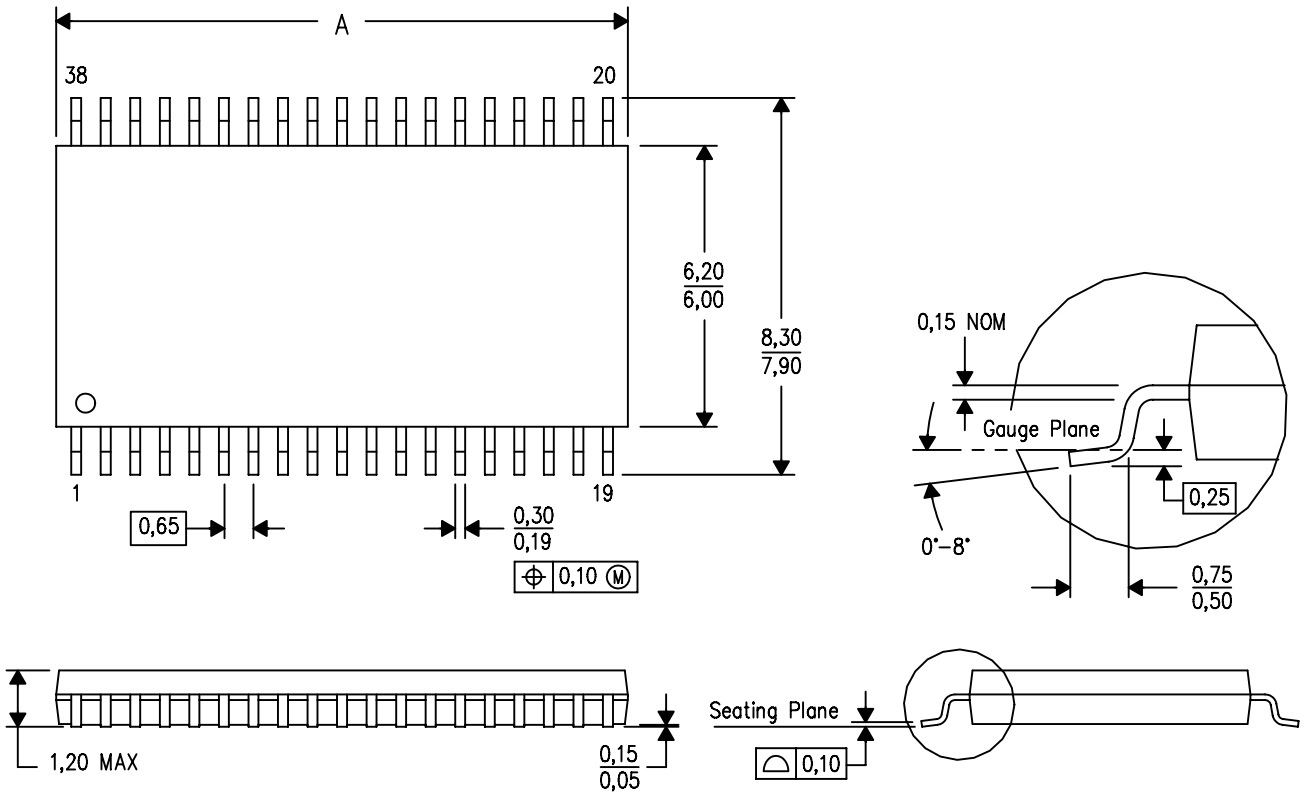


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TSC2100IRHBR	VQFN	RHB	32	3000	336.6	336.6	28.6

DA (R–PDSO–G**) PLASTIC SMALL–OUTLINE PACKAGE

38 PIN SHOWN

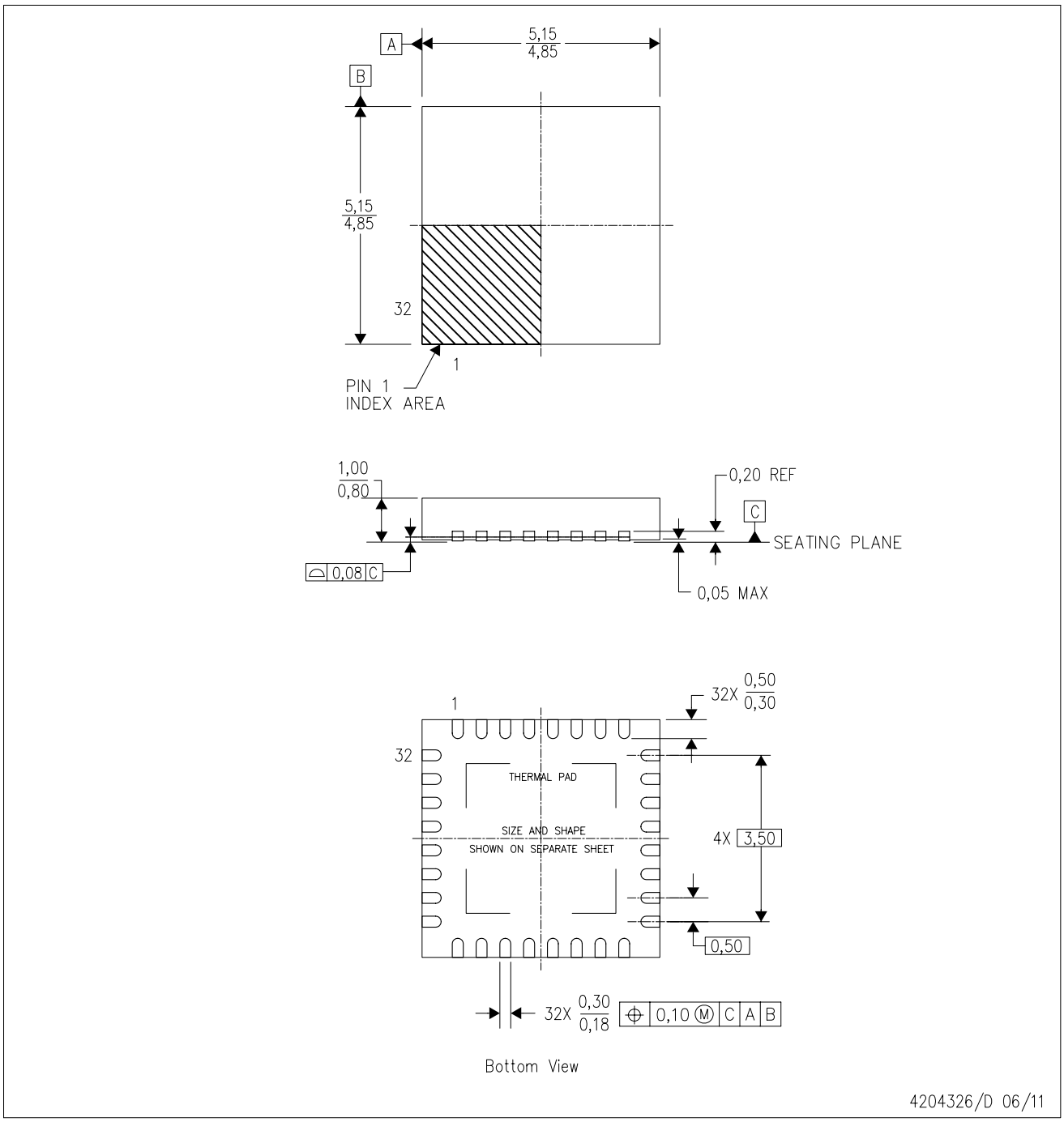


DIM \ PINS **	30	32	38
A MAX	11,10	11,10	12,60
A MIN	10,90	10,90	12,40
△D MO–153 Variation	DB–1	DC	DD–1

4040066/F 01/2009

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
△D Falls within JEDEC MO–153, except 30 pin body length.

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

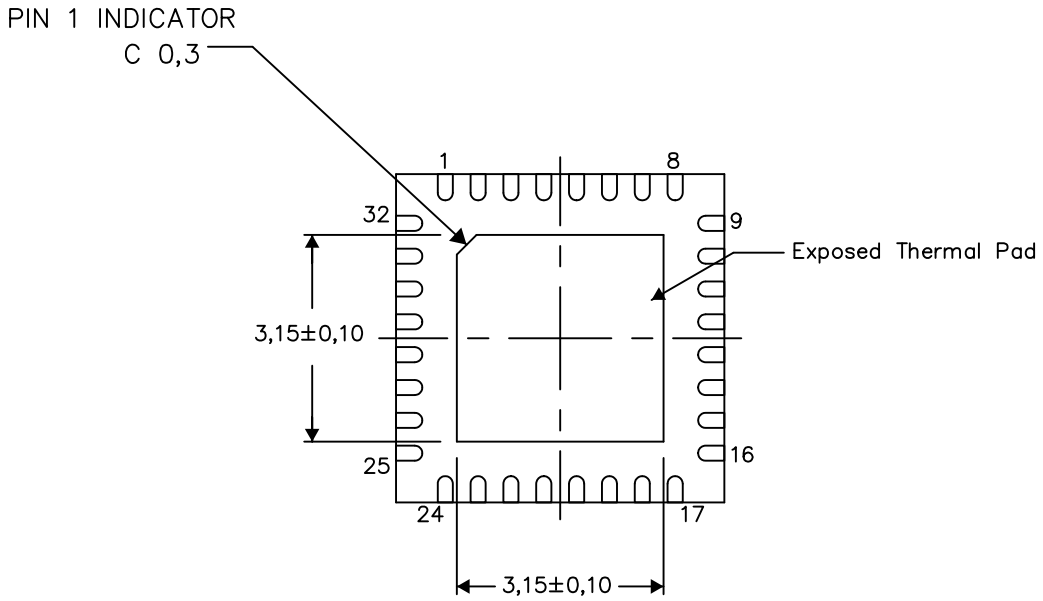
RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



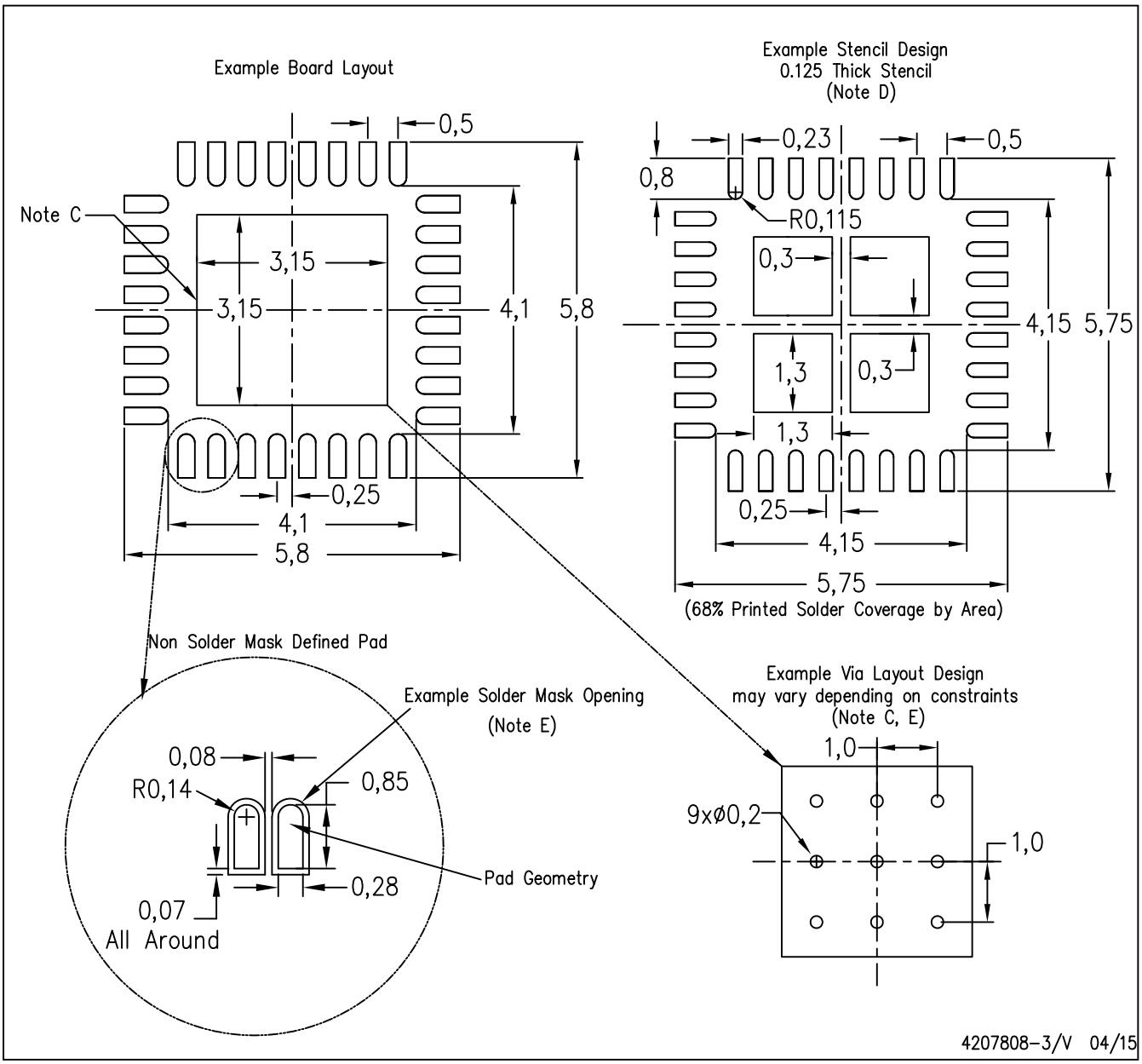
Bottom View

Exposed Thermal Pad Dimensions

4206356–3/AC 05/15

NOTE: A. All linear dimensions are in millimeters

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265