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TXS0206A

SCES833B-NOVEMBER 2011-REVISED APRIL 2016

TXS0206A SD Card Voltage-Translation Transceiver

Technical

Documents

1 Features

- Level Translator
 - $\,$ V_{CCA} and V_{CCB} Range of 1.1 V to 3.6 V
 - Fast Propagation Delay (4.4 ns Maximum When Translating Between 1.8 V and 3 V)
- ESD Protection Exceeds JESD 22
 - 2500-V Human-Body Model (A114-B)
 - 250-V Machine Model (A115-A)
 - 1500-V Charged-Device Model (C101)

2 Applications

- Mobile Phones
- Tablet PCs
- Notebooks
- Ultrabook Computers

3 Description

Tools &

Software

The TXS0206A is a level shifter for interfacing microprocessors with MultiMediaCards (MMCs), secure digital (SD) cards, and Memory Stick[™] cards.

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The voltage-level translator has two supply voltage pins. V_{CCA} as well as V_{CCB} can be operated over the full range of 1.1 V to 3.6 V. The TXS0206A enables system designers to easily interface applications processors or digital basebands to memory cards and SDIO peripherals operating at a different I/O voltage level.

The TXS0206A is offered in a 20-bump wafer chip scale package (WCSP). This package has dimensions of 1.96 mm \times 1.56 mm, with a 0.4-mm ball pitch for effective board-space savings. Memory cards are widely used in mobile phones, PDAs, digital cameras, personal media players, camcorders, settop boxes, etc. Low static power consumption and small package size make the TXS0206A an ideal choice for these applications.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE
TXS0206A	DSBGA (20)	1.96 mm × 1.56 mm

 For all available packages, see the orderable addendum at the end of the data sheet.

Application Example



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2012) to Revision B

•	Added Device Information table, ESD Ratings table, Feature Description section, Device Functional Modes,	
	Application and Implementation section, Power Supply Recommendations section, Layout section, Device and	
	Documentation Support section, and Mechanical, Packaging, and Orderable Information section.	1
•	Deleted the ordering information. See POA at the end of the datasheet	1



5 Pin Configuration and Functions

YFP Package 20–Pin DSBGA Top View							
	1	2	3	4			
Α	\bigcirc	\bigcirc	\bigcirc	\bigcirc			
В	\bigcirc	()	()	\bigcirc			
С	\bigcirc	()	()	\bigcirc			
D	\bigcirc	()	()	\bigcirc			
E	()	\bigcirc	\bigcirc	\bigcirc			

Pin Assignments

	1	2	3	4
Α	DAT2A	V _{CCA}	WP	DAT2B
В	DAT3A	CD	V _{CCB}	DAT3B
С	CMDA	GND	GND	CMDB
D	DAT0A	CLKA	CLKB	DAT0B
E	DAT1A	CLK-f	EN	DAT1B

Pin Functions

PIN .		TYPE	DESCRIPTION		
NO.	NAME	TYPE	DESCRIPTION		
A1	DAT2A	I/O	Data bit 2 connected to host. Referenced to V_{CCA} . Includes a 40-k Ω pullup resistor to V_{CCA} .		
A2	V _{CCA}	Pwr	A-port supply voltage. V _{CCA} powers all A-port I/Os and control inputs.		
A3	WP	0	Connected to write protect on the mechanical connector. The WP pin has an internal 100-k Ω (± 30%) pullup resistor to V _{CCA} . Leave unconnected if not used.		
A4	DAT2B	I/O	Data bit 2 connected to memory card. Referenced to V_{CCB} . Includes a 40-k Ω pullup resistor to V_{CCB} .		
B1	DAT3A	I/O	Data bit 3 connected to host. Referenced to V_{CCA} . Includes a 40-k Ω pullup resistor to V_{CCA} .		
B2	CD	0	Connected to card detect on the mechanical connector. The CD pin has an internal 100-k Ω (± 30%) pullup resistor to V _{CCA} . Leave unconnected if not used.		
B3	V _{CCB}	Pwr	B-port supply voltage. V _{CCB} powers all B-port I/Os.		
B4	DAT3B	I/O	Data bit 3 connected to memory card. Referenced to V_{CCB} . Includes a 40-k Ω pullup resistor to V_{CCB} .		
C1	CMDA	I/O	Command bit connected to host. Referenced to V_{CCA} . Includes a 40-k Ω pullup resistor to V_{CCA} .		
C2	GND	_	Ground		
C3	GND	_	Ground		
C4	CMDB	I/O	Command bit connected to memory card. Referenced to V_{CCB} . Includes a 40-k Ω pullup resistor to V_{CCB} .		
D1	DAT0A	I/O	Data bit 0 connected to host. Referenced to V _{CCA} . Includes a 40-k Ω pullup resistor to V _{CCA} .		
D2	CLKA	I	Clock signal connected to host. Referenced to V _{CCA} .		
D3	CLKB	0	Clock signal connected to memory card. Referenced to V _{CCB} .		
D4	DAT0B	I/O	Data bit 0 connected to memory card. Referenced to V_{CCB} . Includes a 40-k Ω pullup resistor to V_{CCB} .		
E1	DAT1A	I/O	Data bit 1 connected to host. Referenced to V_{CCA} . Includes a 40-k Ω pullup resistor to V_{CCA} .		
E2	CLK-f	0	Clock feedback to host for resynchronizing data to a processor. Leave unconnected if not used.		
E3	EN	Ι	Enable/disable control. Pull EN low to place all outputs in Hi-Z state. Referenced to V _{CCA} .		
E4	DAT1B	I/O	Data bit 1 connected to memory card. Referenced to V _{CCB} . Includes a 40-k Ω pullup resistor to V _{CCB} .		

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CCA}	Supply voltage, A-Port	-0.5	4.6	V	
V _{CCB}	Supply voltage, B-Port		-0.5	4.6	V
VI		I/O ports (A port)	-0.5	4.6	
	Input voltage	I/O ports (B port)	-0.5	4.6	V
		Control inputs	-0.5	4.6	
.,	Voltage range applied to any output in the high-impedance or power-off state	A port	-0.5	4.6	V
Vo		B port	-0.5	4.6	
	Voltage range applied to any output in the high or low state	A port	-0.5	4.6	V
Vo		B port	-0.5	4.6	
I _{IK}	Input clamp current	V ₁ < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
I _O	Continuous output current			±50	mA
	Continuous current through V _{CCA} or GND			±100	mA
T _{stg}	Storage temperature		-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
		Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2500	
V _(ESD) Electros	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 $^{(2)}$	±1500	V
		Machine model (MM)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



6.3 Recommended Operating Conditions

See	(1)	
See	` '	

			V _{CCA}	V _{CCB}	MIN	MAX	UNIT	
V _{CCA}	Supply voltage				1.1	3.6	V	
V _{CCB}	Supply voltage				1.1	3.6	V	
		A-Port CMD and	1.1 V to 1.95 V	1.1 V to 1.95 V				
V _{IH}	High-level input voltage	DATA I/Os B-Port CMD and DATA I/Os	1.95 V to 3.6 V	1.95 V to 3.6 V	V _{CCI} – 0.2	V _{CCI}	V	
		EN and CLKA	1.1 V to 3.6 V	1.1 V to 3.6 V	$V_{CCI} \times 0.65$	V _{CCI}		
		A-Port CMD and	1.1 V to 1.95 V	1.1 V to 1.95 V				
V _{IL}	Low-level input voltage	DATA I/Os B-Port CMD and DATA I/Os	1.95 V to 3.6 V	1.95 V to 3.6 V	0	0.15	V	
		EN and CLKA	1.1 V to 3.6 V	1.1 V to 3.6 V	0	$V_{CCI} \times 0.35$		
V	Output voltage	Active state			0	V _{CCO}	V	
Vo	Oulput voltage	3-state			0	3.6	v	
			1.1 V to 3.6 V			-100	μA	
			1.1 V to 1.3 V			-0.5	i	
	High-level output current (CLK-f output)	urrent (CLK fourtout)	1.4 V to 1.6 V	1.1 V to 3.6 V		-1		
I _{ОН}		1.65 V to 1.95 V	1.1 V 10 3.6 V		-2	mA		
	-		2.3 V to 2.7 V				-4	
			3 V to 3.6 V			-8		
			1.1 V to 3.6 V		100		μA	
	Low-level output current (CLK-f output)		1.1 V to 1.3 V			0.5		
			1.4 V to 1.6 V	1.1 V to 3.6 V		1		
I _{OL}			1.65 V to 1.95 V			2	mA	
			2.3 V to 2.7 V		4			
			3 V to 3.6 V			8		
				1.1 V to 3.6 V		-100	μA	
				1.1 V to 1.3 V		-0.5		
lau	High-level output current (CLK output)		1.1 V to 3.6 V	1.4 V to 1.6 V		-1		
I _{OH}			1.1 V to 5.0 V	1.65 V to 1.95 V		-2	mA	
				2.3 V to 2.7 V		-4		
				3 V to 3.6 V		-8		
				1.1 V to 3.6 V		100	μA	
				1.1 V to 1.3 V		0.5		
le.		rrent (CLK output)	1.1 V to 3.6 V	1.4 V to 1.6 V		1		
I _{OL}	Low-level output current (CLK output)		1.1 V 10 3.0 V	1.65 V to 1.95 V		2	mA	
				2.3 V to 2.7 V		4		
				3 V to 3.6 V		8		
Δt/Δv	Input transition rise	or fall rate				5	ns/V	
T _A	Operating free-air te	emperature			-40	85	°C	

 All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, SCBA004.

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6.4 Thermal Information

		TXS0206A	
	THERMAL METRIC ⁽¹⁾	YFP (DSBGA)	UNIT
		20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	71.1	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	0.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	10.4	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

F	ARAMETER	TEST CONDITIONS	V _{CCA}	V _{CCB}	MIN	TYP ⁽¹⁾ MAX	UNIT	
		I _{OH} = -100 μA	1.1 V to 3.6 V	1.65 V to 3.6 V	$V_{CCA} \times 0.8$			
		I _{OH} = -0.5 mA	1.1 V	1.65 V to 3.6 V	0.8			
	A port	$I_{OH} = -1 \text{ mA}$	1.4 V	1.65 V to 3.6 V	1.05			
	(CLK-f output) V _{OH}	$I_{OH} = -2 \text{ mA}$	1.65 V	1.65 V to 3.6 V	1.2			
VOH		$I_{OH} = -4 \text{ mA}$	2.3 V	1.65 V to 3.6 V	1.75		V	
		$I_{OH} = -8 \text{ mA}$	3 V	1.65 V to 3.6 V	2.3			
A port (DAT and CMD outputs)	I _{OH} = -20 μA	1.1 V to 3.6 V	1.65 V to 3.6 V	V _{CCA} × 0.8				
		I _{OL} = 100 μA	1.1 V to 3.6 V	1.65 V to 3.6 V		$V_{CCA} \times 0.2$		
		I _{OL} = 0.5 mA	1.1 V	1.65 V to 3.6 V		0.35		
	A port	I _{OL} = 1 mA	1.4 V	1.65 V to 3.6 V		0.35	v	
	(CLK-f output)	$I_{OL} = 2 \text{ mA}$	1.65 V	1.65 V to 3.6 V		0.45	v	
		I _{OL} = 4 mA	2.3 V	1.65 V to 3.6 V		0.55		
V _{OL}		I _{OL} = 8 mA	3 V	1.65 V to 3.6 V		0.7		
		I _{OL} = 135 μA	1.1 V	1.65 V to 3.6 V		0.4		
	A port	I _{OL} = 180 μA	1.4 V	1.65 V to 3.6 V		0.4		
	(DAT and CMD	I _{OL} = 220 μA	1.65 V	1.65 V to 3.6 V		0.4	V	
	outputs)	I _{OL} = 300 μA	2.3 V	1.65 V to 3.6 V		0.4		
		I _{OL} = 400 μA	3 V	1.65 V to 3.6 V		0.55		
		I _{OH} = -100 μA	1.1 V to 3.6 V	1.65 V to 3.6 V	$V_{CCB} \times 0.8$			
	B port	$I_{OH} = -2 \text{ mA}$	1.1 V to 3.6 V	1.65 V	1.2			
V _{OH}	(CLK output)	$I_{OH} = -4 \text{ mA}$	1.1 V to 3.6 V	2.3 V	1.75		V	
· ОП		I _{OH} = -8 mA	1.1 V to 3.6 V	3 V	2.3		·	
	B port (DAT output)	I _{OH} = -20 μA	1.1 V to 3.6 V	1.65 V to 3.6 V	$V_{CCB} \times 0.8$			

(1) All typical values are at $T_A = 25^{\circ}C$.

Electrical Characteristics (continued)

F	PARAMETER	TEST CONDITIONS	V _{CCA}	V _{CCB}	MIN TYP ⁽¹⁾ MAX	UNIT
		I _{OL} = 100 μA	1.1 V to 3.6 V	1.65 V to 3.6 V	$V_{CCB} \times 0.2$	
	B port	$I_{OL} = 2 \text{ mA}$	1.1 V to 3.6 V	1.65 V	0.45	V
	B port	$I_{OL} = 4 \text{ mA}$	1.1 V to 3.6 V	2.3 V	0.55	
V		I _{OL} = 8 mA	1.1 V to 3.6 V	3 V	0.7	
V _{OL}		I _{OL} = 135 μA	1.1 V to 3.6 V	1.65 V to 3.6 V	0.4	
	B port (DAT output)	I _{OL} = 220 μA	1.1 V to 3.6 V	1.65 V	0.4	V
		I _{OL} = 300 μA	1.1 V to 3.6 V	2.3 V	0.4	
		I _{OL} = 300 μA	1.1 V to 3.6 V	3 V	0.55	
I _I	Control inputs	$V_I = V_{CCA}$ or GND	1.1 V to 3.6 V	1.65 V to 3.6 V	±1	μA
I _{CCA}	A port	$V_{I} = V_{CCI}, I_{O} = 0$	1.1 V to 3.6 V	1.65 V to 3.6 V	7	μA
I _{CCB}	B port	$V_{I} = V_{CCI}, I_{O} = 0$	1.1 V to 3.6 V	1.65 V to 3.6 V	11	μA
~	A port				5.5 6.5	- 5
C _{io}	B port				7 9.5	pF
~	Control inputs	$V_I = V_{CCA}$ or GND			3.5 4.5	- 5
Ci	Clock input	$V_I = V_{CCA}$ or GND			3 4	pF

over recommended operating free-air temperature range (unless otherwise noted)

6.6 Timing Requirements— $V_{CCA} = 1.2 \text{ V} \pm 0.1 \text{ V}$

over recommended operating free-air temperature range (unless otherwise noted)

				V _{cc}	MIN	MAX	UNIT	
			Push-pull	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		40		
		Command	driving	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		40	Mhna	
			Open-drain	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		1	Mbps	
Data rate			driving	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		1		
Dala Tale		Cleak	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		40	MHz		
		Clock	Push-pull	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		40	IVITIZ	
		Data	driving	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		40	Mhna	
		Dala		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		40	Mbps	
			Push-pull driving	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	25		20	
		Command		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	25		ns	
		Command	Open-drain	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	1			
	Pulse		driving	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1		μs	
t _W	duration	Clock		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	10		20	
		CIUCK	Push-pull	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	8.3		ns	
		Dete	driving	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	25		20	
		Data		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	25		ns	

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6.7 Timing Requirements— $V_{CCA} = 1.8 \text{ V} \pm 0.15 \text{ V}$

over recommended operating free-air temperature range (unless otherwise noted)

				V _{cc}	MIN MAX	UNIT	
			Push-pull	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	60		
		Command	driving	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	60	Mbps	
			Open-drain	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	1	Mobs	
Data rata			driving	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1		
Data rate		Clash		V _{CCB} = 1.8 V ± 0.15 V	60	N411-	
		Clock	Push-pull	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	60	MHz	
		Dete	driving	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	60	Mhno	
		Data		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	60	Mbps	
			Push-pull driving	V _{CCB} = 1.8 V ± 0.15 V	17		
				$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	17	ns	
		Command	Open-drain	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	1		
	Pulse		driving	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1	μs	
t _W	duration	Clash		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	8.3		
		Clock	Push-pull	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	8.3	ns	
			driving	V _{CCB} = 1.8 V ± 0.15 V	17		
		Data		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	17	ns	

6.8 Timing Requirements— $V_{CCA} = 3.3 V \pm 0.3 V$

over recommended operating free-air temperature range (unless otherwise noted)

				V _{cc}	MIN MA	X UNIT
			Push-pull	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	(60
		Command	driving	V_{CCB} = 3.3 V ± 0.3 V	(0 Mbps
		Commanu	Open-drain	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		1 INIDPS
Doto roto			driving	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		1
Data rate		Clock Push-pull		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$!	5 MHz
			Push-pull	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	ł	55
		Data	driving Data	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	(0 Mbps
		Dala		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	(in the second se
			Push-pull driving	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	17	ns
		Command		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	17	115
		Command	Open-drain	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	1	μs
+	Pulse		driving	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1	μs
t _W	duration	Clock		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	9	ns
		CIUCK	Push-pull	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	9	115
		Data	driving	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	17	ns
				$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	17	115



6.9 Switching Characteristics— $V_{CCA} = 1.2 \text{ V} \pm 0.1 \text{ V}$

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{cc}	MIN	МАХ	UNIT
	CMDA	CMDD	V _{CCB} = 1.8 V ± 0.15 V		5.7	
	CMDA	CMDB	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		4.4	
	ONDD	CMPA	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		6.7	
	CMDB	CMDA	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		5.8	
		OL KD	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		6.2	
	CLKA	CLKB	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		4.5	
bd	DATA	DATUD	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		7.6	ns
	DATxA	DATxB	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		7.5	
		DATXA	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		6.3	
	DATxB	DATxA	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		4.6	
		01// 6	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		12	
	CLKA	CLK-f	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		7.9	
		D 1	V _{CCB} = 1.8 V ± 0.15 V		1	
	EN	B-port	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		1	
en		A	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		1	μs
	EN	A-port	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		1	
		D 1	V _{CCB} = 1.8 V ± 0.15 V		412	ns
	EN	B-port	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		363	
lis		A port	V _{CCB} = 1.8 V ± 0.15 V		423	
	EN	A-port	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		422	
	0.454		V _{CCB} = 1.8 V ± 0.15 V	3.5	8.4	
	CMDA	rise time	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	3.4	8.1	
	0.144	CLK f rise time		1	4.7	
A	CLK-f rise time		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1	4.1	ns
				3.5	8.4	
	DATxA rise time		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	3.4	8.1	
	01122			1.4	6.5	
	CMDB	CMDB rise time		0.6	3.1	
	01.1/2		V _{CCB} = 1.8 V ± 0.15 V	0.6	5.9	
В	CLKB	ise time	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	0.5	4.3	ns
			V _{CCB} = 1.8 V ± 0.15 V	1.4	10.9	
	DATXB	rise time	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	0.6	5	
	0.15.1	6 H A	V _{CCB} = 1.8 V ± 0.15 V	2.4	5.7	
	CMDA	fall time	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	2	5.1	
	0.177		V _{CCB} = 1.8 V ± 0.15 V	0.8	2.5	
A	CLK-f	fall time	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	0.8	3	ns
		6 H C	V _{CCB} = 1.8 V ± 0.15 V	2.4	5.7	
	DATxA	fall time	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1.9	5.1	
		Z 11	V _{CCB} = 1.8 V ± 0.15 V	1.2	5.4	
	CMDB	fall time	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	0.6	3.6	
	01.17	6. H. C	V _{CCB} = 1.8 V ± 0.15 V	0.6	6.3	
В	CLKB	fall time	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	0.5	4	ns
		6 H 2	V _{CCB} = 1.8 V ± 0.15 V	0.6	6.3	
	DATxB fall time		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	0.5	3.6	
	Channel-	to-channel	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		1	
SK(O)		ew	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		1	ns

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Switching Characteristics— $V_{CCA} = 1.2 V \pm 0.1 V$ (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{cc}	MIN MAX	UNIT	
		Duch null driving	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	40		
		Push-pull driving	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	40	Mbpo	
	Command	Open-drain driving	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	1	Mbps	
Max data rate			$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1		
	Clock		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	40		
			$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	60	MHz	
	D		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	40	h dhara	
	Data		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	40	Mbps	

6.10 Switching Characteristics— $V_{CCA} = 1.8 \text{ V} \pm 0.15 \text{ V}$

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{cc}	MIN	МАХ	UNIT
	01/04	01400	V _{CCB} = 1.8 V ± 0.15 V		4.9	
	CMDA	CMDB	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		3.3	
	OMDD	OMDA	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		5.6	
	CMDB	CMDA	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		3.6	
	01.144		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		5.4	
	CLKA	CLKB	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		3.4	
t _{pd}	DATxA	DATUD	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		5	ns
	DATXA	DATxB	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		4.4	
		DATVA	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		5.4	
	DATxB	DATxA	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		3.5	
	CLKA		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		10.2	
	CLKA	CLK-f	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		5.7	
	EN	D nort	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		1	μs
	EN	B-port	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		1	
t _{en}		Anort	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		1	
	EN	A-port	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		1	
	EN	B-port	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		411	ns
	EN		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		411	
t _{dis}	EN	A	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		413	
	EN	A-port	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		361	
	CMDA		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	2.1	4.5	
	CMDA	rise time	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	2.1	4.1	
	01/(6	i	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	0.6	2.5	
t _{rA}	CLK-II	ise time	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	0.6	2.3	ns
	DATKA	ria a tima	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	1.8	4.5	
	DATXA	rise time	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1.8	4.2	
	CMDD	rise time	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	1.4	6.6	
	CMDB		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	0.7	3.8	
		iao timo	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	0.5	5.8	ns
t _{rB}	ULKB r	ise time	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	0.5	4.4	
		rico timo	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	1.4	10.8	
	DATXB	rise time	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	0.7	8	



Switching Characteristics— $V_{CCA} = 1.8 V \pm 0.15 V$ (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{cc}	MIN	МАХ	UNIT	
	CMDA fall time		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	0.4	3.4		
			$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	0.3	2.9		
t _{fA}		fall time	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	0.3	2.8	ns	
	CER-I		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	0.3	2.8	115	
		fall time	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	0.4	3.4		
	DATXA		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	0.3	2.9		
•	CMDR	fall time	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	1.1	6.3		
	CMDB fall time		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	0.6	3.7		
	CLKB fall time		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	0.6	8.7	ns	
t _{fB}			$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	0.5	4.1		
	DATxB fall time		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	1.2	7		
			$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	0.2	4		
	Channel-to-channel		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		1	20	
t _{SK(O)}	sk	ew	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		1	ns	
		Push-pull driving	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		60		
	Command	P ush-pull unving	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		60	Mbps	
	Command	Open-drain driving	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		1	Mbps	
Max data rate		Open-drain driving	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		1		
ויומג טמומ ומוכ	CL	ock	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		60	MHz	
	Clock		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		60		
	Data		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		60	Mbps	
			$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		60	edana.	

6.11 Switching Characteristics—V_{CCA} = 3.3 V \pm 0.3 V

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{cc}	MIN MAX	UNIT
	CMDA	CMDB	V _{CCB} = 1.8 V ± 0.15 V	5.3	
	CMDA	CIVIDB	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	3.2	
	CMDB	ONDA	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	5.1	
		CMDA	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	3	
	CLKA		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	4.8	
		CLKB	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	3.1	
t _{pd}	DATxA	DATxB	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	5.1	ns
		DATXB	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	3.2	
	DATxB	DATxA	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	9.6	
	DATXB	DATXA	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	5.1	
	CLKA	CLK-f	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	6.8	
	CLKA		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	4.2	
	EN	B-port	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	1	
	EIN	в-роп	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1	
t _{en}	EN	Aport	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	1	μs
	EIN	A-port	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1	
	EN	P port	$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	410	
	EN	B-port	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	364	
t _{dis}	EN A-		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	396	-
		A-port	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	398	

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Switching Characteristics— V_{CCA} = 3.3 V ± 0.3 V (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{cc}	MIN	МАХ	UNIT	
	01454		V _{CCB} = 1.8 V ± 0.15 V	1.4	4.2		
	CMDA	rise time	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1.4	4.2		
	01// 4	i	V _{CCB} = 1.8 V ± 0.15 V	0.5	1.5		
rA	CLK-f rise time		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	0.5	1.4	ns	
	DATUA		V _{CCB} = 1.8 V ± 0.15 V	1.4	3.4		
	DATXA	DATxA rise time		1.3	3		
	ONDD		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$	1.4	6.4		
[‡] rв	CMDB	rise time	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	0.9	4		
	01.1/D	1	V _{CCB} = 1.8 V ± 0.15 V	0.6	5.9		
	CLKB rise time		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	0.5	4.4	ns	
	DATxB rise time		V _{CCB} = 1.8 V ± 0.15 V	1.4	14		
	DATXB	rise time	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	0.9	14	l	
	CMDA fall time		V _{CCB} = 1.8 V ± 0.15 V	0.8	2.3		
	CMDA	tali time	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	0.8	2.3		
fA	01// (6 H C	V _{CCB} = 1.8 V ± 0.15 V	0.4	1.3		
	CLK-T	fall time	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	0.4	1.3	ns	
		6.0.0	V _{CCB} = 1.8 V ± 0.15 V	0.8	2.2		
	DATxA fall time		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	0.7	2		
	CMDB fall time		V _{CCB} = 1.8 V ± 0.15 V	0.8	6.2		
			$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	0.8	5		
	01.1/5			0.6	7.8		
В	CLKB	fall time	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	0.5	4.3	ns	
	547.5	6 H C	V _{CCB} = 1.8 V ± 0.15 V	0.7	6.8		
	DATXB	fall time	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	0.6	5		
	Channel-	to-channel	V _{CCB} = 1.8 V ± 0.15 V		1		
SK(O)		æw	V _{CCB} = 3.3 V ± 0.3 V		1	ns	
			V _{CCB} = 1.8 V ± 0.15 V		60		
		Push-pull driving	V _{CCB} = 3.3 V ± 0.3 V		60		
	Command		V _{CCB} = 1.8 V ± 0.15 V		1	Mbps	
		Open-drain driving			1		
Max data rate			V _{CCB} = 1.8 V ± 0.15 V		55		
	Cl	Clock			55	MHz	
	_				60		
	Data		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$ $V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		60	Mbps	

6.12 Operating Characteristics $-V_{CCA} = 1.2 V$

 $T_A = 25^{\circ}C$

	PARAMETER		TEST	V _{CCB}	UNIT		
FARAWETER			CONDITIONS	1.8 V	3.3 V	UNIT	
	A-port input,	CLK Enabled		15.1	15		
	B-port output	DATA Enabled		9.26	9.19		
C (1)	B-port input, A-port output	DATA Enabled	$C_L = 0,$	12.4	11.9	pF	
C _{pdA} ⁽¹⁾	A-port input,	CLK Disabled	f = 10 MHz, $t_r = t_f = 1 \text{ ns}$	0.1	0.1		
	B-port output	DATA Disabled		1.3	1.3		
	B-port input, A-port output	DATA Disabled		0.1	0.1		

(1) Power dissipation capacitance per transceiver.



Operating Characteristics $-V_{CCA} = 1.2 V$ (continued)

 $T_A = 25^{\circ}C$

PARAMETER			TEST	V _{CCB}	UNIT	
PARAMETER		CONDITIONS	1.8 V	3.3 V	UNIT	
	A-port input, B-port output	DATA Enabled		26.7	30.3	
	B-port input, A-port output	CLK Enabled	$C_L = 0,$	25.6	27	
C (1)		DATA Enabled		16.38	19.91	۶Ē
C _{pdB} ⁽¹⁾ A-port input, B-port output B-port input,	DATA Disabled	f = 10 MHz, $t_r = t_f = 1 \text{ ns}$	0.1	0.1	pF	
	B-port input,	CLK Disabled		0.1	0.1	
	A-port output	DATA Disabled		1.1	0.8	

6.13 Operating Characteristics $-V_{CCA} = 1.8 V$

 $T_A = 25^{\circ}C$

PARAMETER		TEST	V _{CCE}	LINUT		
		CONDITIONS	1.8 V	3.3 V	UNIT	
	A-port input,	CLK Enabled		17.5	17.1	
	B-port output	DATA Enabled		9.96	9.82	
C _{pdA} ⁽¹⁾ B-port input, A-port output A-port input, B-port output		DATA Enabled	$C_{L} = 0,$	15.6	14	- 5
	A-port input,	CLK Disabled	f = 10 MHz, $t_r = t_f = 1 \text{ ns}$	0.1	0.1	pF
	B-port output	DATA Disabled		1.3	1.3	
	B-port input, A-port output	DATA Disabled		0.1	0.1	
	A-port input, B-port output	DATA Enabled		26	28.5	
	B-port input,	CLK Enabled		25.8	27	
c (1)	A-port output	DATA Enabled	$C_L = 0,$	16.69	19.6	
C _{pdB} ⁽¹⁾	A-port input, B-port output	DATA Disabled	f = 10 MHz, $t_r = t_f = 1 \text{ ns}$	0.1	0.1	– pF
	B-port input,	CLK Disabled		0.1	0.1	
	A-port output	DATA Disabled		1.1	0.8	

(1) Power dissipation capacitance per transceiver.

6.14 Operating Characteristics — V_{CCA} = 3.3 V

 $T_A = 25^{\circ}C$

	DADAMETE	D	TEST	V _{CCB}	UNIT	
PARAMETER			CONDITIONS	1.8 V	3.3 V	UNIT
	A-port input,	CLK Enabled		17.5	17.1	
	B-port output	DATA Enabled		12.50	13.29	
C (1)	B-port input, A-port output	DATA Enabled	$C_{L} = 0,$	15.6	14	~ F
C _{pdA} ⁽¹⁾	A-port input, B-port output	CLK Disabled	f = 10 MHz, $t_r = t_f = 1 \text{ ns}$	0.1	0.1	pF
		DATA Disabled		1.3	1.3	
	B-port input, A-port output	DATA Disabled		0.1	0.1	

(1) Power dissipation capacitance per transceiver.

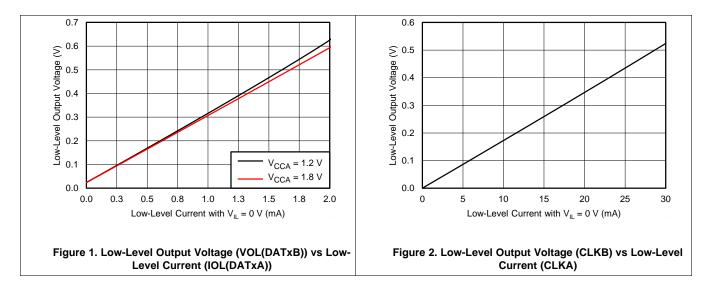
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Operating Characteristics — $V_{CCA} = 3.3 V$ (continued)

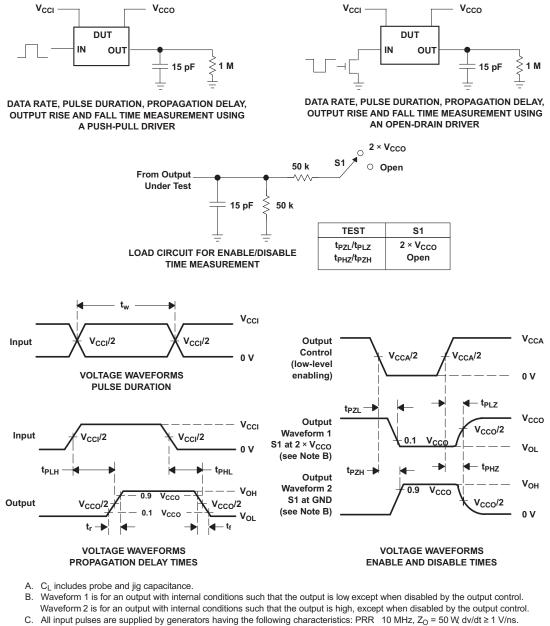
T _A = 25°C			TEST	V _{CCE}	3 TYP	
PARAMETER			CONDITIONS	1.8 V	3.3 V	UNIT
	A-port input, B-port output DATA Enabled			26	28.5	
	B-port input, A-port output	CLK Enabled		25.8	27	pF
c (1)		DATA Enabled	$C_{L} = 0,$	16.67	19.92	
C _{pdB} ⁽¹⁾	A-port input, B-port output	DATA Disabled	f = 10 MHz, $t_r = t_f = 1 \text{ ns}$	0.1	0.1	
	B-port input,	CLK Disabled		0.1	0.1	1
	A-port output	DATA Disabled		1.1	0.8	

6.15 Typical Characteristics





7 Parameter Measurement Information



- D. The outputs are measured one at a time, with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis} . E.
- t_{PZL} and t_{PZH} are the same as t_{en} . F.
- t_{PLH} and t_{PHL} are the same as t_{pd} . G.
- Η. V_{CCI} is the V_{CC} associated with the input port.
- V_{CCO} is the V_{CC} associated with the output port. 1.
- J. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

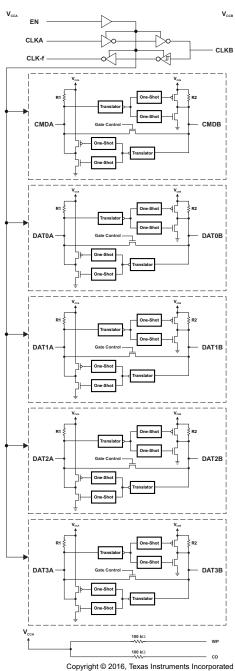


8 Detailed Description

8.1 Overview

The TXS0206A is a complete application-specific voltage-translator designed to bridge the digital switching compatibility gap and interface logic threshold levels between a micrprocessor with MMC, SD, and Memory Stick[™] cards. It is intended to be used in a point-to-point topology when interfacing these devices that may or may not be operating at different interface voltages.

8.2 Functional Block Diagram





8.3 Feature Description

8.3.1 Architecture

The CLKA, CLKB, and CLK-f subsystem interfaces consist of a fully-buffered voltage translator design that has its output transistors to source and sink current optimized for drive strength. CLKA is a CMOS input and therefore must not be left floating.

The SDIO lines comprise a semi-buffered auto-direction-sensing based translator architecture (see Figure 4) that does not require a direction-control signal to control the direction of data flow of the A to B ports (or from B to A ports).

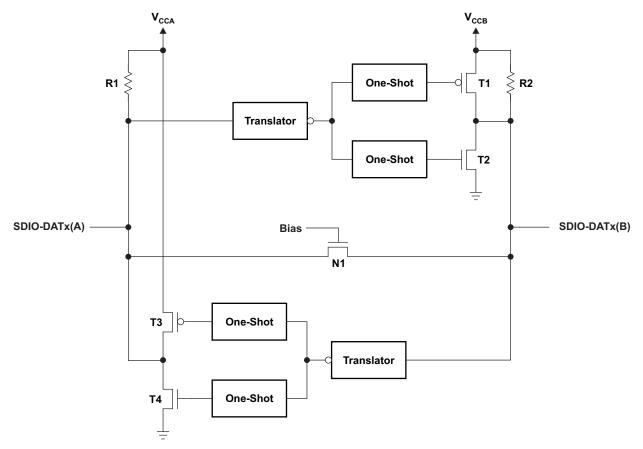


Figure 4. Architecture of an SDIO Switch-Type Cell

Each of these bidirectional SDIO channels independently determines the direction of data flow without a direction-control signal. Each I/O pin can be automatically reconfigured as either an input or an output, which is how this auto-direction feature is realized.

The following two key circuits are employed to facilitate the "switch-type" voltage translation function:

- 1. Integrated pullup resistors to provide dc-bias and drive capabilities
- 2. An N-channel pass-gate transistor topology (with a high R_{ON} of approximately 300 Ω) that ties the A-port to the B-port
- 3. Output one-shot (O.S.) edge-rate accelerator circuitry to detect and accelerate rising edges on the A or B ports

For bidirectional voltage translation, pullup resistors are included on the device for dc current sourcing capability. The V_{GATE} gate bias of the N-channel pass transistor is set at a level that optimizes the switch characteristics for maximum data rate as well as minimal static supply leakage. Data can flow in either direction without guidance from a control signal.

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Feature Description (continued)

The edge-rate acceleration circuitry speeds up the output slew rate by monitoring the input edge for transitions, helping maintain the data rate through the device.

During a low-to-high signal rising-edge, the O.S. circuits turn on the PMOS transistors (T_1 , T_3) and its associated driver output resistance of the driver is decreased to approximately 50 Ω to 70 Ω during this acceleration phase to increase the current drive capability of the driver for approximately 30 ns or 95% of the input edge, whichever occurs first. This edge-rate acceleration provides high ac drive by bypassing the internal pullup resistors during the low-to-high transition to speed up the rising-edge signal.

During a high-to-low signal falling-edge, the O.S. circuits turn on the NMOS transistors (T_2 , T_4) and its associated driver output resistance of the driver is decreased to approximately 50 Ω to 70 Ω during this acceleration phase to increase the current drive capability of the driver for approximately 30 ns or 95% of the input edge, whichever occurs first.

To minimize dynamic I_{CC} and the possibility of signal contention, the user should wait for the O.S. circuit to turnoff before applying a signal in the opposite direction. The worst-case duration is equal to the minimum pulsewidth number provided in the *Timing Requirements*— $V_{CCA} = 1.2 V \pm 0.1 V$ section of this data sheet.

Once the O.S. is triggered and switched off, both the A and B ports must go to the same state (i.e. both High or both Low) for the one-shot to trigger again. In a DC state, the output drivers maintain a Low state through the pass transistor. The output drivers maintain a High through the "smart pullup resistors" that dynamically change value based on whether a Low or a High is being passed through the SDIO lines, as follows:

- R_1 and R_2 values are a nominal 40 k Ω when the output is driving a low
- R_1 and R_2 values are a nominal 4 k Ω when the output is driving a high
- R_1 and R_2 values are a nominal 40 k Ω when the device is disabled via the EN pin or by pulling the either V_{CCA} or V_{CCB} to 0 V.
- The threshold at which the resistance changes is approximately V_{CCx}/2

The reason for using these "smart" pullup resistors is to allow the TXS0206 to realize a lower static power consumption (when the I/Os are low), support lower V_{OL} values for the same size pass-gate transistor, and improved simultaneous switching performance.

8.4 Device Functional Modes

Table 1 lists the functional modes of the TXS0206A.

EN	TRANSLATOR I/Os
L	Disabled, pulled to V_CCA, V_CCB through 40 k $\!\Omega$
Н	Active

Table 1. Function Table



9 Application and Implementation

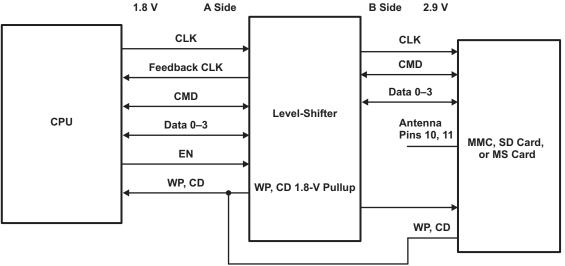
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Systems engineers working with SD and MMC memory cards face a dilemma. These cards operate at a higher voltage node than the latest multimedia application processors, which have moved to smaller process technology nodes that support a maximum I/O interface voltage of 1.2 V. The problem is bridging the gap between these two voltage nodes while maintaining digital switching compatibility. The TXS0206A was designed specifically to address this. It is an auto direction sensing voltage level shifter that can interface with high speed SD and MMC cards because it supports a clock frequency of up to 60 MHz and each data channel supports up to 60 Mbps.

9.2 Typical Application



Integrated Pullup/Pulldown Resistors

Figure 5. Typical Application Circuit

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 2

Table 2	2. Desi	gn Para	meters
---------	---------	---------	--------

PARAMETERS	VALUES
Input voltage	1.1 V to 3.6 V
Output voltage	1.1 V to 3.6 V

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
 - Use the supply voltage of the microprocessor that is driving the TXS0206A to determine the input voltage range. For a valid logic high, the value must exceed the V_{IH} of the input port. For a valid logic low, the value must be less than the V_{IL} of the input port.
- Output voltage range

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 Use the supply voltage of the memory card that the TXS0206A is driving to determine the output voltage range.

9.2.2.1 External Pulldown Resistors

When using the TXS0206A device with MMCs, SD, and Memory StickTM to ensure that a valid receiver input voltage high (V_{IH}) is achieved, the value of any pulldown resistors (external or internal to a memory card) must not be smaller than a 10-k Ω value. The impact of adding too heavy (less than 10-k Ω value) a pulldown resistor to the data and command lines of the TXS0206A device and the resulting 4-k Ω pullup / 10-k Ω pulldown voltage divider network has a direct impact on the V_{IH} of the signal being sent into the memory card and its associated logic.

The resulting V_{IH} voltage for the 10-k Ω pulldown resistor value would be:

 $V_{CC} \times 10 \ k\Omega / (10 \ k\Omega + 4 \ k\Omega) = 0.714 \times V_{CC}$

This is marginally above a valid input high voltage for a 1.8-V signal (i.e., 0.65 × V_{CC}).

The resulting V_{IH} voltage for 20-k Ω pulldown resistor value would be:

 $V_{CC} \times 20 \text{ k}\Omega / (20 \text{ k}\Omega + 4 \text{ k}\Omega) = 0.833 \times V_{CC}$

Which is above the valid input high voltage for a 1.8-V signal of 0.65 \times V_{CC}.

9.2.3 Application Curves

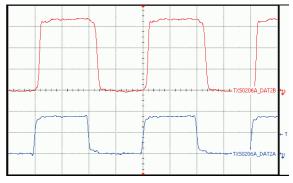
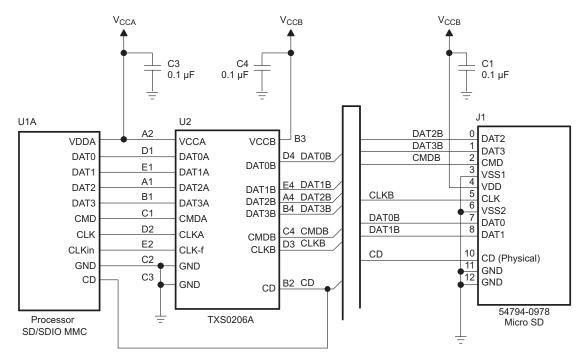


Figure 6. 1.8 V to 3.3 V Translation at 25 MHz



9.3 System Examples





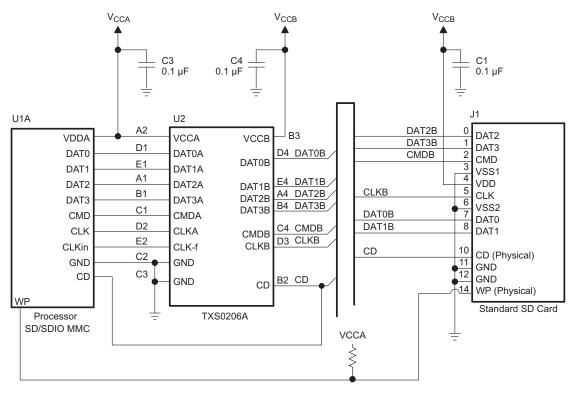


Figure 8. Interfacing With Seperate WP and CD Pin

System Examples (continued)

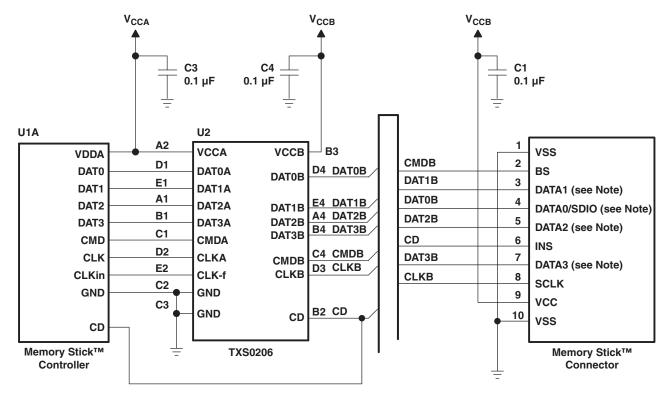


Figure 9. Interfacing With Memory Stick[™] Card

10 Power Supply Recommendations

The TXS0206A does not require power sequencing between V_{CCA} and V_{CCB} during power-up so the power-supply rails can be ramped in any order.

The EN pin is referenced to V_{CCA} and when configured to low, will place all outputs into a high-impedance state. To ensure the high-impedance state of the outputs during power up or power down, the EN pin must be tied to GND through a pulldown resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pulldown resistor to ground is determined by the current-sourcing capability of the driver controlling the EN pin.

Finally, the EN pin may be shorted to V_{CCA} if the application does not require use of the high-impedance state at any time.

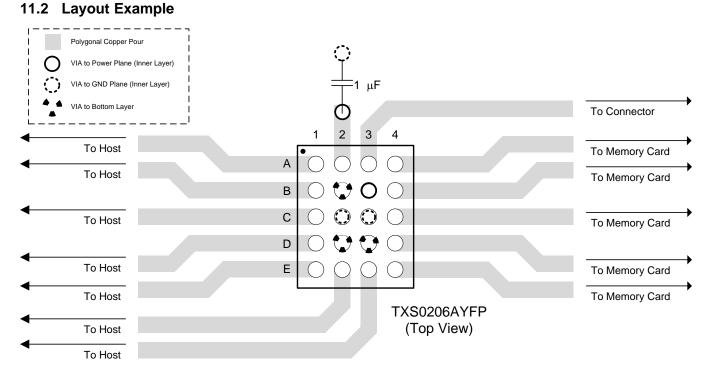
11 Layout

11.1 Layout Guidelines

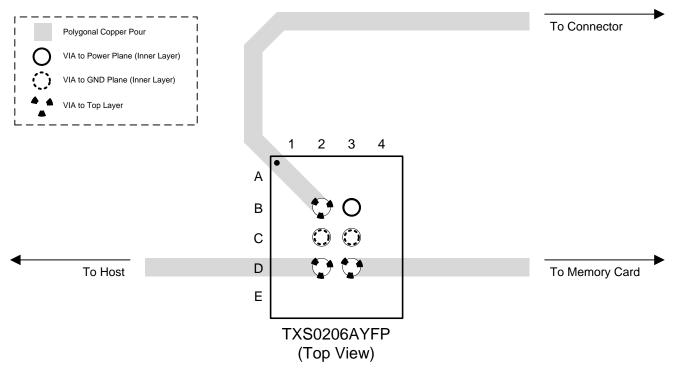
To ensure reliability of the device, TI recommends following common printed-circuit board layout guidelines.

- Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading
- PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one shot duration, approximately 30 ns, ensuring that any reflection encounters low impedance at the source driver
- With very heavy capacitive loads, the one-shot can time-out before the signal is driven fully to the positive rail, so it is recommended that this lumped-load capacitance be considered and kept below 50 pF to avoid O.S. retriggering, bus contention, output signal oscillations, or other adverse system-level affects.













12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Introduction to Logic, SLVA700.
- TXS0206A Evaluation Module, SCEU008.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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12.3 Trademarks

E2E is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



20-Jan-2016

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
TXS0206AYFPR	ACTIVE	DSBGA	YFP	20	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TXS0206A	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE OPTION ADDENDUM

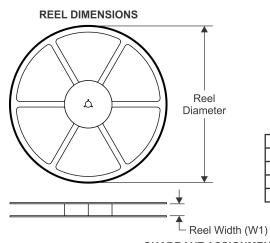
20-Jan-2016

PACKAGE MATERIALS INFORMATION

www.ti.com

Texas Instruments

TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal	
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Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXS0206AYFPR	DSBGA	YFP	20	3000	180.0	8.4	1.66	2.06	0.56	4.0	8.0	Q1

TEXAS INSTRUMENTS

www.ti.com

PACKAGE MATERIALS INFORMATION

20-Jan-2016



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXS0206AYFPR	DSBGA	YFP	20	3000	182.0	182.0	20.0

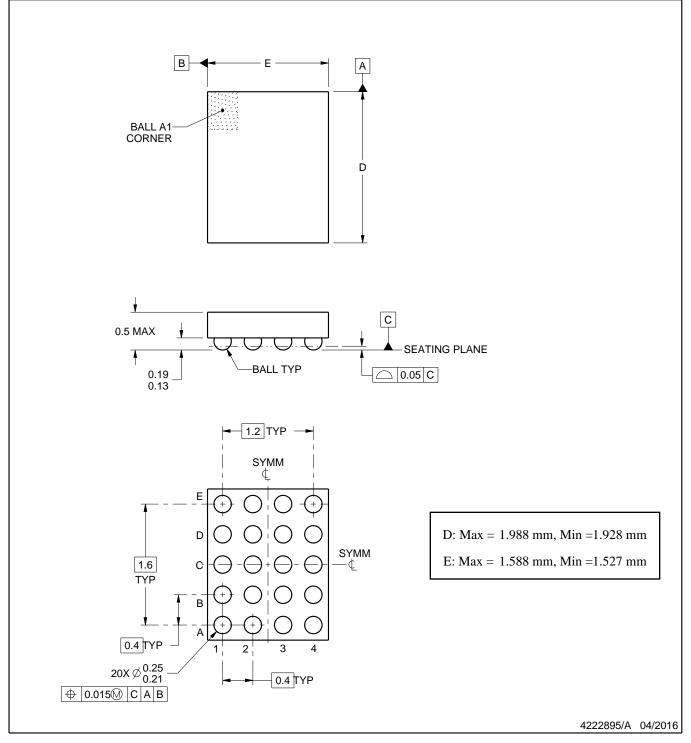
YFP0020



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M. 2. This drawing is subject to change without notice.

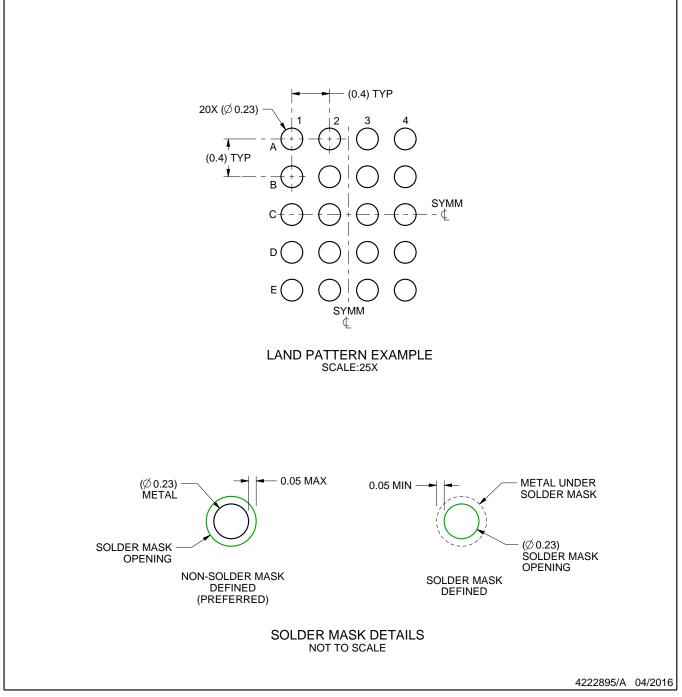


YFP0020

EXAMPLE BOARD LAYOUT

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

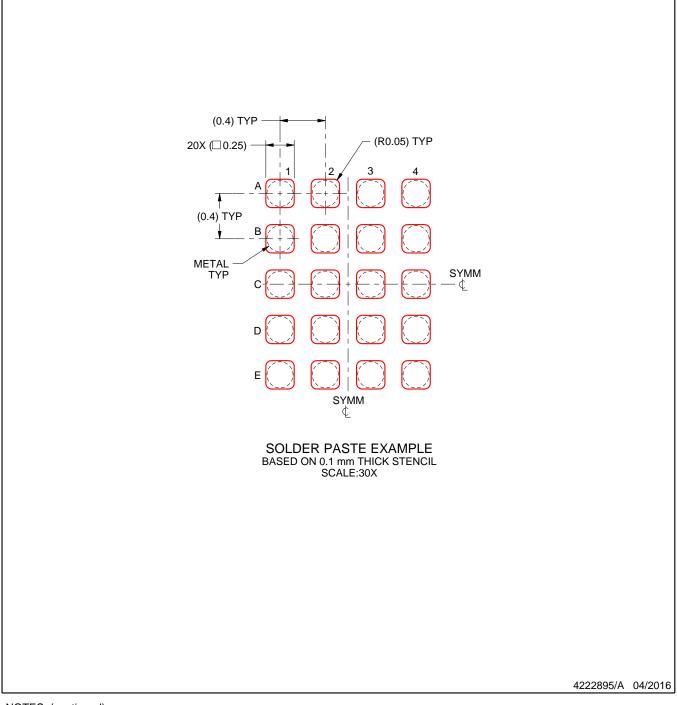


YFP0020

EXAMPLE STENCIL DESIGN

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



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