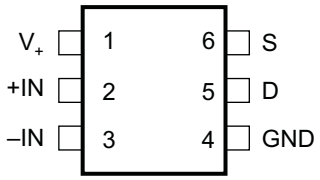
COMPARATOR WITH OUTPUT VOLTAGE-LEVEL TRANSLATION

FEATURES

- **Low Supply Current: 8 μA (Max)**
- **Supply Voltage: 2.5 V to 5.5 V**
- **Output FET Provides Down Translation**
- **Small Package: SOT-563**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance**
  - **2500-V Human-Body Model (JESD-A114E)**
  - **250-V Machine Model (EIA/JESD A115-A)**
  - **1500-V Charged-Device Model (JESD22-C101-A Level III)**

DRL PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

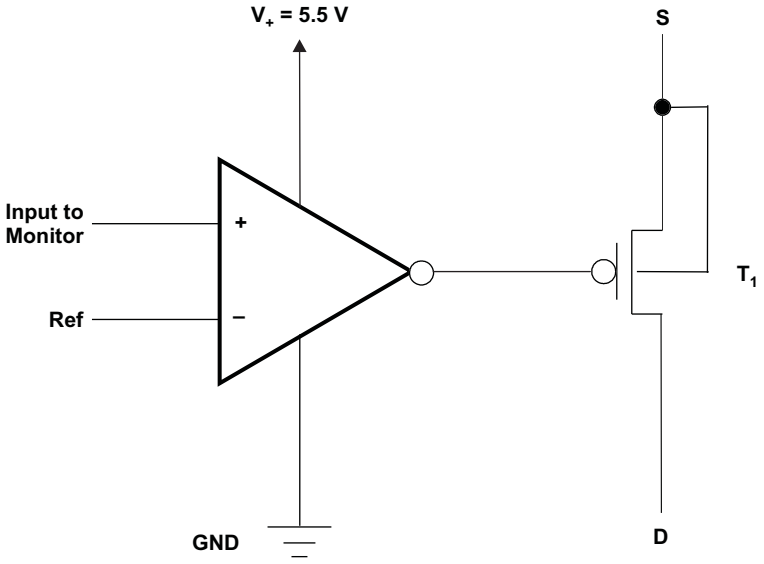
The TXS03121 is a comparator designed for battery monitoring applications. It can be operated with a voltage of 2.5 V to 5.5 V. The reference voltage is applied to the –IN terminal, whereas the voltage to be monitored is connected to +IN. When the voltage at +IN is greater than the voltage at –IN, the output FET is turned On. When the voltage at +IN is less than the voltage at –IN, the output FET is turned Off. The source (S) of the output FET can be connected to 1.1 V to 3.6 V, which allows the output signal to be level translated to another voltage value. The voltage at V_+ must be greater than or equal to the voltage at S. The voltage at S must be greater than or equal to the voltage at D ($V_+ \geq V_S \geq V_D$).

ORDERING INFORMATION

T_A	PACKAGE(1)(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOT-563 – DRL	Tape and reel	TXS03121DRLR	2FR

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

APPLICATION BLOCK DIAGRAM



PIN ASSIGNMENTS

NO.	NAME	DESCRIPTION
1	V_+	Comparator supply voltage
2	+IN	Comparator positive input
3	–IN	Comparator negative input
4	GND	Ground
5	D	Drain of output FET
6	S	Source of output FET

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_+	Supply voltage range(2)		–0.5	6.5	V
+IN, –IN	Input voltage range		–0.5	6.5	V
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current (On-state switch current)			–50	mA
	Continuous current through V_+ or GND			±100	mA
θ_{JA}	Package thermal impedance(3)	DRL package		171.6	°C/W
T_{stg}	Storage temperature range			150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_+	Comparator supply voltage	2.5	5.5	V
V_S, V_D(1)	Output FET source or drain voltage	1.1	3.6	V
T_A	Operating free-air temperature	–40	85	°C

(1) V_+ must be greater than or equal to V_S, and V_S must be greater than or equal to V_D ($V_+ \geq V_S \geq V_D$).

COMPARATOR ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

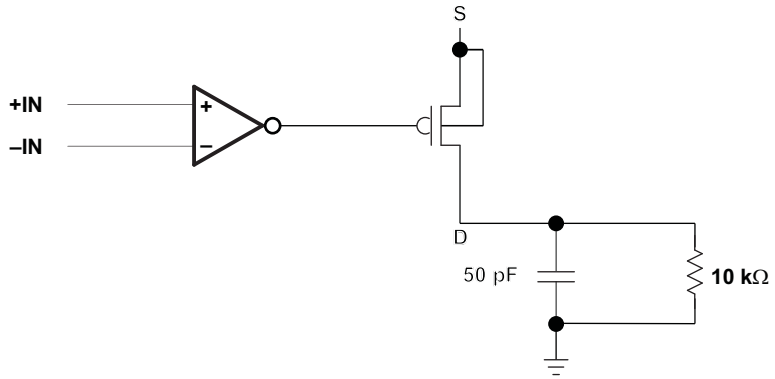
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage	V_+ = 2.5 V to 5.5 V	V_{CM} = 0.8 V, I_O = 0	–10	0.5	10	mV
			V_{CM} = V_+, I_O = 0				
V_{CM}	Common-mode voltage range	V_+ = 2.5 V to 5.5 V		0.8		V_+	V
I_{+IN}	Input leakage current	V_+ = 2.5 V to 5.5 V	V_{+IN} = 0 V to V_+			0.5	µA
$I_{–IN}$			$V_{–IN}$ = 0 V to V_+				
I_+	Supply current	V_+ = 2.5 V to 5.5 V				8	µA
C_{IN}	Capacitance of +IN, –IN pins				2	2.5	pF

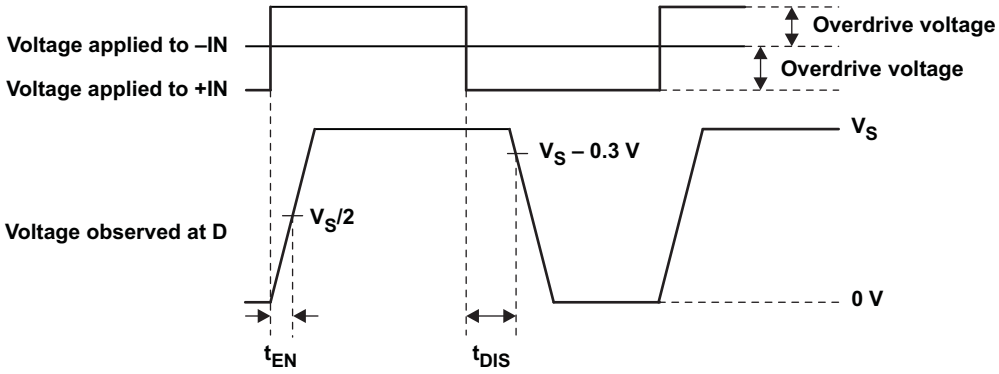
OUTPUT FET ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$I_{DS(ON)}$	On leakage current	V_S = 1.1 V to 3.6 V, Switch ON					0.5	µA
$I_{DS(OFF)}$	Off leakage current	V_S = 1.1 V to 3.6 V, V_D = Open, Switch OFF					0.5	µA
$C_{(ON)}$	On capacitance				4	5.1	6	pF
$C_{(OFF)}$	Off capacitance, S and D terminals				1.5	3.4	5	pF
r_{ON}	On resistance of output FET	$V_+ \geq V_S$, I_D = -100 µA		V_S = 1.1 V			150	Ω
				V_S = 1.4 V			65	
				V_S = 1.65 V			61	
				V_S = 2.3 V			50	
				V_S = 3 V			44	
t_{EN}	Enable time	20-mV overdrive	$V_{–IN}$ = 0.8 V, V_S = 1.65 V	V_+ = 4.5 V			1.7	µs
				V_+ = 3 V			3.9	
			$V_{–IN}$ = V_+, V_S = 1.65 V	V_+ = 4.5 V			1	
				V_+ = 3 V			3.9	
		50-mV overdrive	V_{-IN} = 0.8 V, V_S = 1.65 V	V_+ = 4.5 V			1.2	
				V_+ = 3 V			2.7	
				V_+ = 2.5 V			6.2	
			$V_{–IN}$ = V_+, V_S = 1.65 V	V_+ = 4.5 V			1	
				V_+ = 3 V			2.4	
				V_+ = 2.5 V			5.3	
		100-mV overdrive	$V_{–IN}$ = 0.8 V, V_S = 1.65 V	V_+ = 4.5 V			0.8	
				V_+ = 3 V			1.4	
				V_+ = 2.5 V			5	
			$V_{–IN}$ = V_+, V_S = 1.65 V	V_+ = 4.5 V			0.7	
				V_+ = 3 V			1.3	
				V_+ = 2.5 V			4.7	
t_{DIS}	Disable time	20-mV overdrive	$V_{–IN}$ = 0.8 V, V_S = 1.65 V	V_+ = 4.5 V			4.4	µs
				V_+ = 3 V			12	
			$V_{–IN}$ = V_+, V_S = 1.65 V	V_+ = 4.5 V			3.5	
				V_+ = 3 V			6.1	
		50-mV overdrive	$V_{–IN}$ = 0.8 V, V_S = 1.65 V	V_+ = 4.5 V			4.1	
				V_+ = 3 V			9.6	
				V_+ = 2.5 V			5.3	
			$V_{–IN}$ = V_+, V_S = 1.65 V	V_+ = 4.5 V			2.5	
				V_+ = 3 V			3.2	
				V_+ = 2.5 V			5.2	
		100-mV overdrive	$V_{–IN}$ = 0.8 V, V_S = 1.65 V	V_+ = 4.5 V			4.6	
				V_+ = 3 V			6.7	
				V_+ = 2.5 V			5.2	
			$V_{–IN}$ = V_+, V_S = 1.65 V	V_+ = 4.5 V			1.9	
				V_+ = 3 V			2.8	
				V_+ = 2.3 V			4.9	

PARAMETER MEASUREMENT INFORMATION





PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TXS03121DRLR	ACTIVE	SOT-5X3	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2FR	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

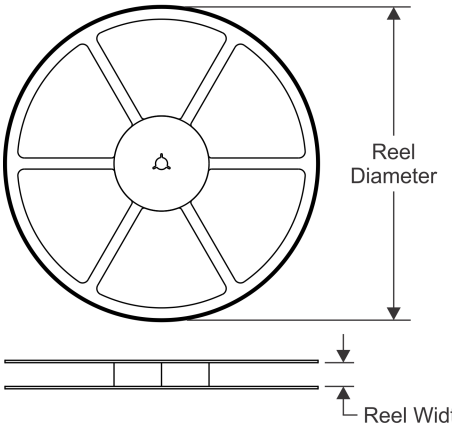
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

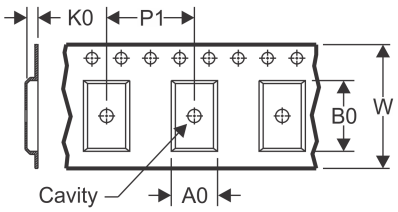
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

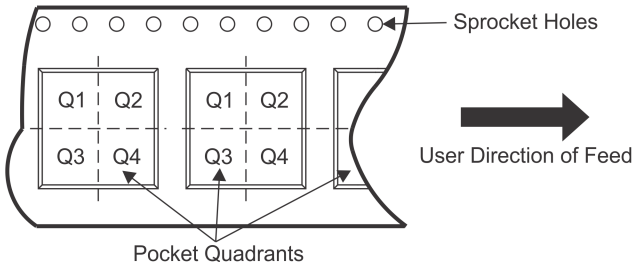


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

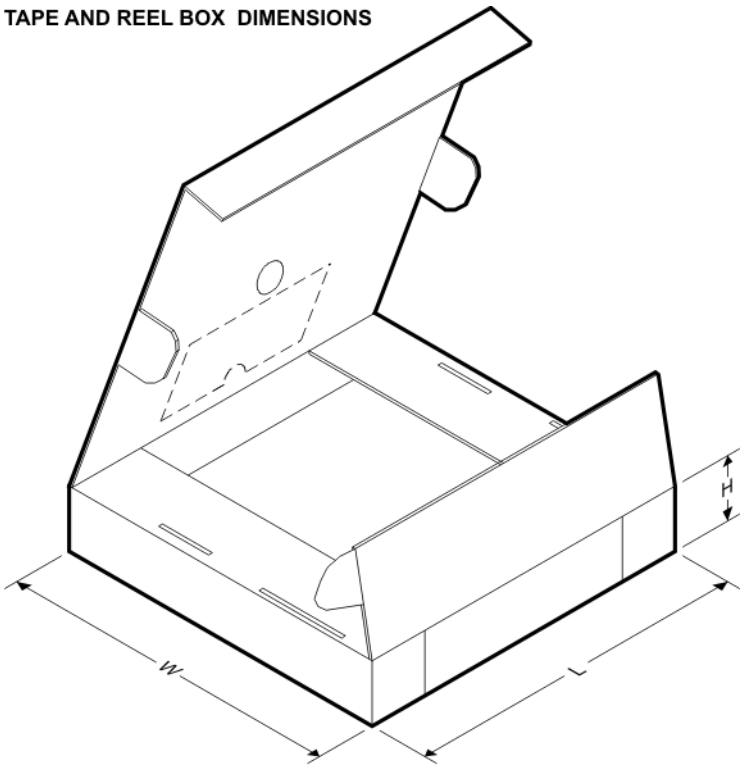
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

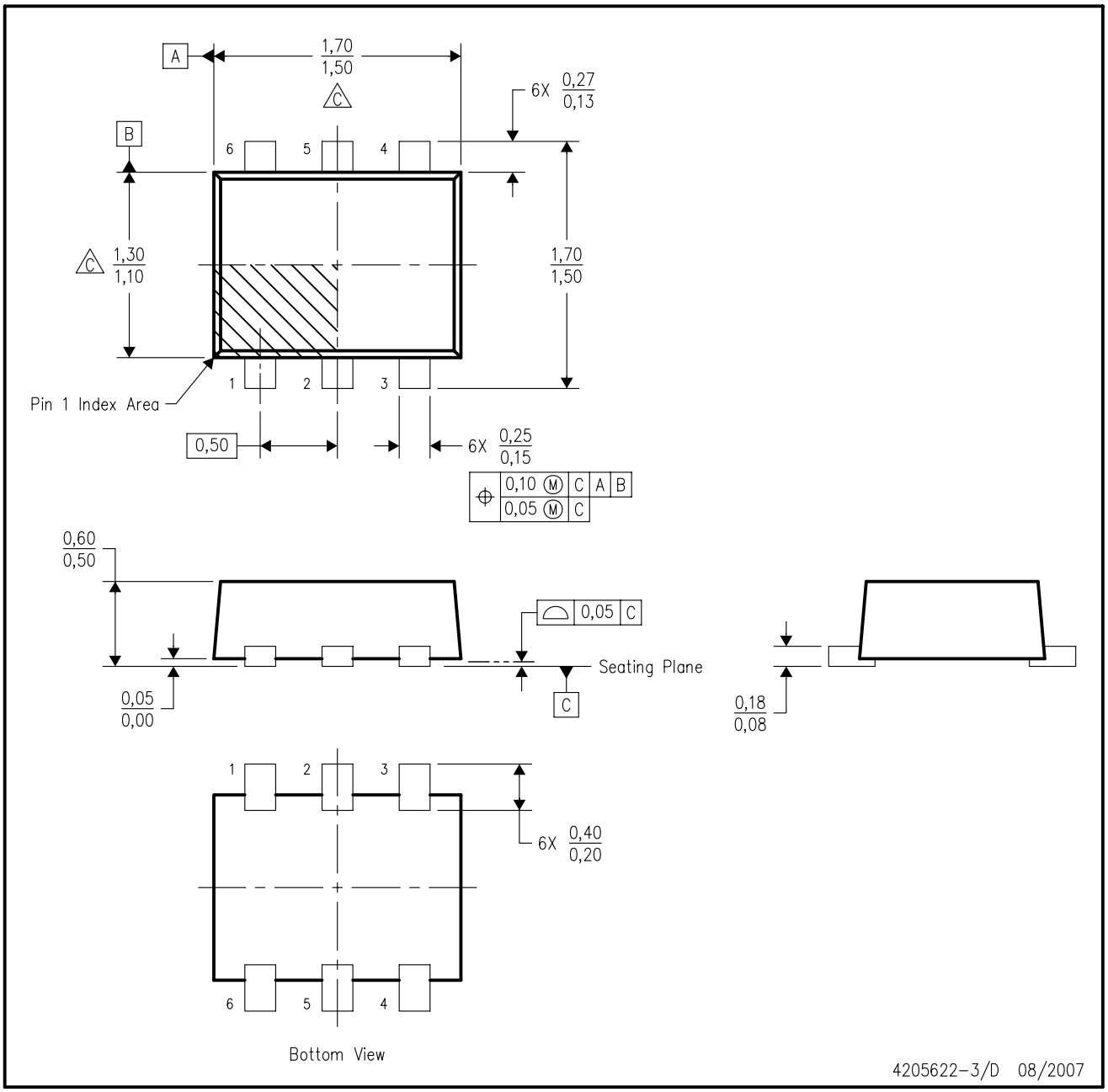
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXS03121DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



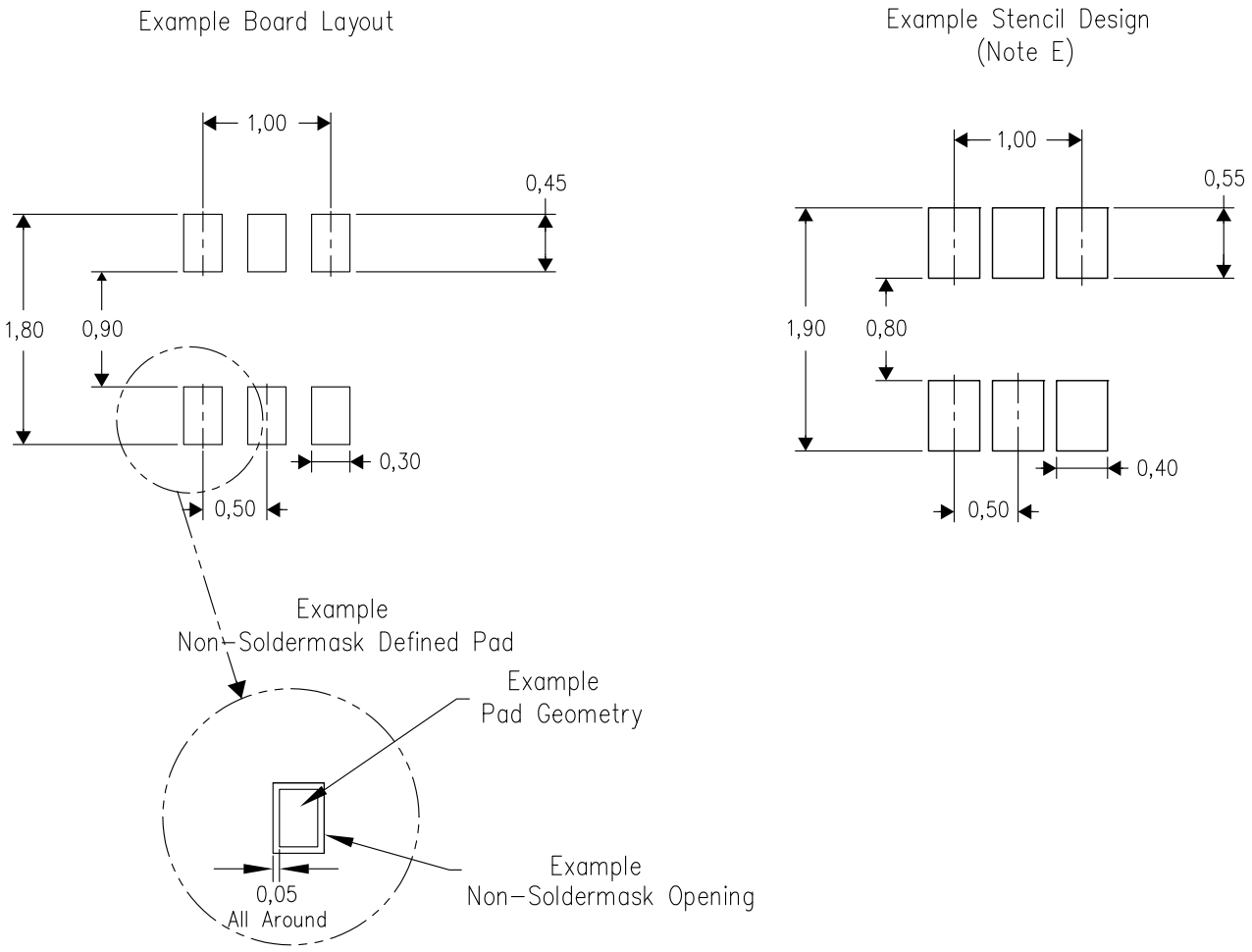
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXS03121DRLR	SOT-5X3	DRL	6	4000	202.0	201.0	28.0



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
D. JEDEC package registration is pending.

DRL (R–PDSO–N6) PLASTIC SMALL OUTLINE



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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