

PHASE SHIFT RESONANT CONTROLLER

FEATURES

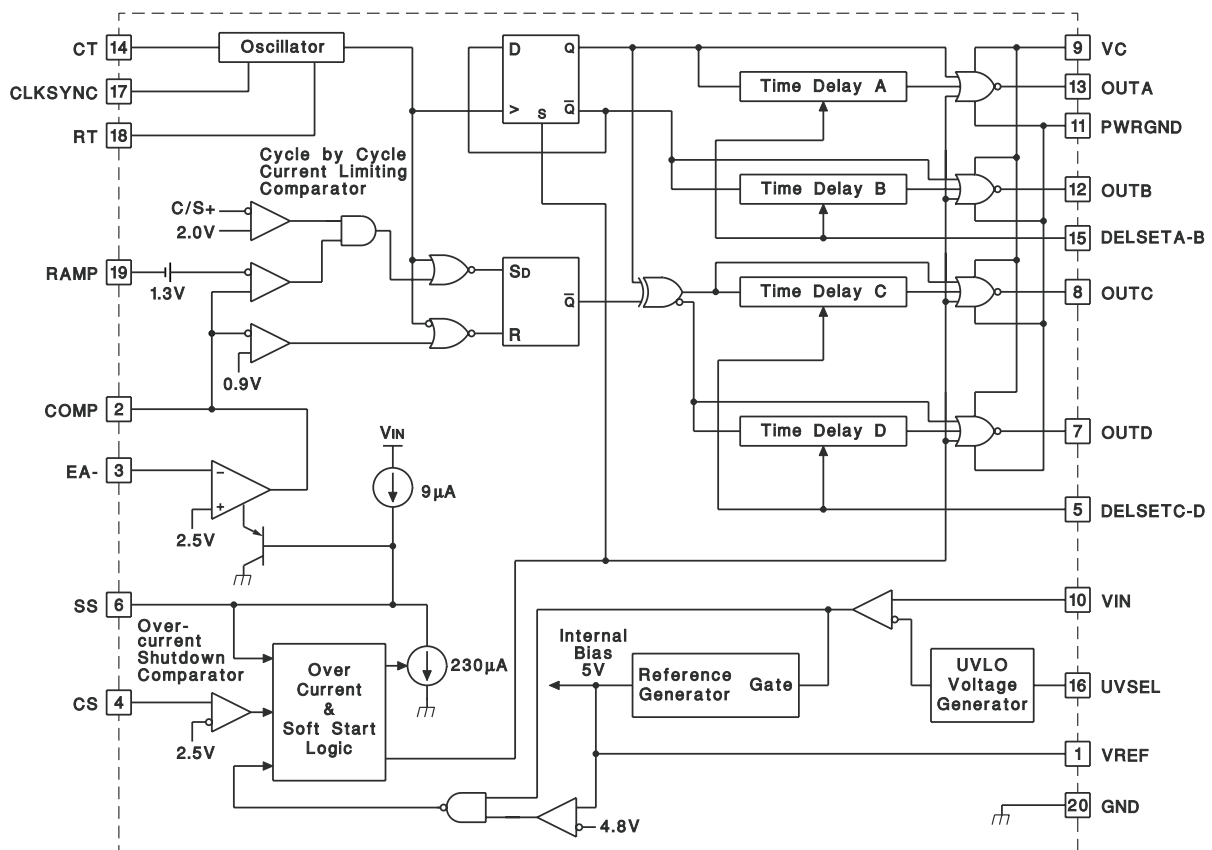
- Programmable Output Turn On Delay; Zero Delay Available
- Compatible with Voltage Mode or Current Mode Topologies
- Practical Operation at Switching Frequencies to 300 kHz
- 10-MHz Error Amplifier
- Pin Programmable Undervoltage Lockout
- Low Startup Current – 150 μ A
- Soft Start Control
- Outputs Active Low During UVLO

DESCRIPTION

The UC3879 controls a bridge power stage by phase shifting the switching of one half-bridge with respect to the other. This allows constant frequency pulse width modulation in combination with resonant, zero-voltage switching for high efficiency performance. The UC3879 can be configured to provide control in either voltage mode or current mode operation, with overcurrent shutdown for fast fault protection.

Independently programmable time delays provide dead-time at the turn-on of each output stage, allowing time for each resonant switching interval.

BLOCK DIAGRAM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

DESCRIPTION (CONTINUED)

With the oscillator capable of operating in excess of 600 kHz, overall output switching frequencies to 300 kHz are practical. In addition to the standard free running mode, with the CLKS_{SYNC} pin, the user may configure the UC3879 to accept an external clock synchronization signal. Alternatively, up to three units can be locked together with the operational frequency determined by the fastest device.

Protective features include an undervoltage lockout and overcurrent protection. Additional features include a 10-MHz error amplifier, a 5-V precision reference, and soft start. The UC3879 is available in 20 pin N, J, DW, and Q and 28 pin L packages.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

PARAMETER	VALUE	UNIT
Supply voltage (V _C , V _{IN})	20	V
Output current, source or sink, dc	20	mA
Output current, source, sink peak for 0.1 μs at max frequency of 300 kHz	100	
Analog inputs		
(Pins 1, 2, 3, 4, 5, 6, 14, 15, 17, 18, 19)	–0.3 to 5.3	V
(Pin 16)	–0.03 to V _{IN}	
Analog outputs		
(Pins 7, 8, 12, 13)	–0.3 to V _C to 0.3	V
Storage temperature range	–65°C to 150°C	°C
Junction temperature	–55°C to 150°C	
Lead temperature (soldering, 10 sec)	300°C	

(1) Pin references are to 20-pin DIL and SOIC packages. All voltages are with respect to ground unless otherwise stated. Currents are positive into, negative out of the specified terminal.

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

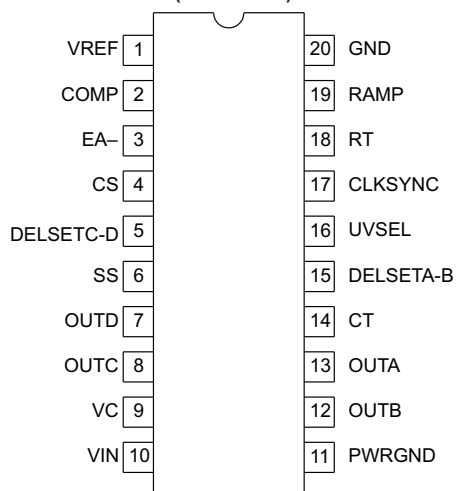
PACKAGE	θ _{JA}	θ _{JC}
J-20	70-85	28 ⁽¹⁾
N-20	80 ⁽²⁾	35
DW-20 SOIC	45-95 ⁽²⁾	25
PLCC-20	43-75 ⁽²⁾	34
CLCC-20	N/A	5-8 ⁽²⁾⁽³⁾

- (1) θ_{JC} data values stated were derived from MIL-STD-1835B. MIL-STD-1835B states "The baseline values shown are worst case (mean +2s) for a 60 x 60 mil microcircuit device silicon die and applicable for devices with die sizes up to 14400 square mils. For devices die sizes greater than 14400 square mils use the following values; dual-in-line, 11°C/W; flat pack 10°C/W; pin grid array, 10°C/W".
- (2) Specified θ_{JA} (junction-to-ambient) is for devices mounted to 5-in² FR4 PC board with one ounce copper wire where noted. When resistance range is given, lower values are for 5-in² aluminum PC board. Test PWB was 0.062 in thick and typically used 0.635-mm trace widths for power packages and 1.3-mm trace widths for non-power packages with a 100 x 100 mil probe land area at the end of each trace.
- (3) θ_{JC} estimated for backside of device, through the metalized thermal conduction pads.

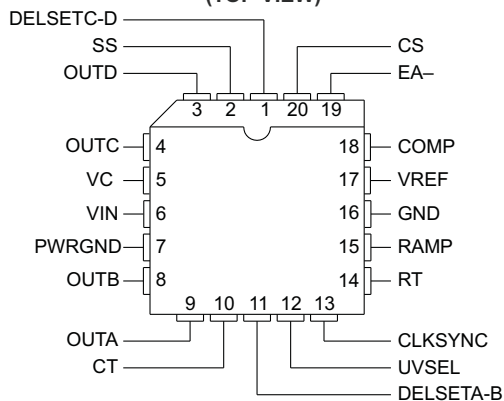
Product Selection Guide

	TEMPERATURE RANGE	AVAILABLE PACKAGES
UCC1879	-55°C to 125°C	J, L
UCC2879	-40°C to 85°C	N, DW, Q, J, L
UCC3879	0°C to 70°C	N, DW, Q

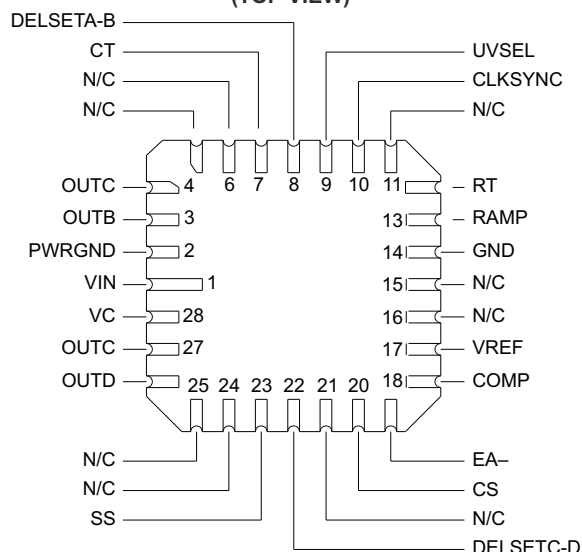
**DIL-20, SOIC-2
J OR N PACKAGE, DW PACKAGE
(TOP VIEW)**



**PLCC-20
Q PACKAGE
(TOP VIEW)**



**CLCC-28
L PACKAGE
(TOP VIEW)**



ELECTRICAL CHARACTERISTICS

Unless specified; $V_C = V_{IN} = V_{UVSEL} = 12\text{ V}$, $C_T = 470\text{ pF}$, $R_T = 9.53\text{ k}$, $R_{DELSETA-B} = R_{DELSEC-D} = 4.8\text{ k}$, $C_{DELSETA-B} = C_{DELSETC-D} = 0.01\text{ }\mu\text{F}$, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Undervoltage Lockout					
Start threshold	$V_{UVSEL} = V_{IN}$	9	10.75	12.5	V
	$V_{UVSEL} = \text{Open}$	12.5	15.25	16.5	
UVLO hysteresis	$V_{UVSEL} = V_{IN}$	1.15	1.75	2.15	
	$V_{UVSEL} = \text{Open}$	5.2	6	7.4	
Input bias, UVSEL pin	$V_{UVSEL} = V_{IN} = 8\text{ V}$		30		μA
Supply Current					
I_{VIN} startup	$V_{IN} = V_{UVSEL} = 8\text{ V}$, $V_C = 18\text{ V}$, $I_{DELSETA-B} = I_{DELSETC-D} = 0$		150	600	μA
I_{VC} startup	$V_{IN} = V_{UVSEL} = 8\text{ V}$, $V_C = 18\text{ V}$, $I_{DELSETA-B} = I_{DELSETC-D} = 0$		10	100	
I_{VIN} operating	UC3879, UC2879		23	35	mA
	UC1879		23	36	
I_{VC} operating			4	8	
Voltage Reference					
Output voltage	$T_J = 25^\circ\text{C}$	4.92	5	5.08	V
Line regulation	$11\text{ V} < V_{IN} < 18\text{ V}$		1	10	mV
Load regulation	$I_{VREF} = -10\text{ mA}$		5	20	
Total variation	Line, Load, Temperature	4.875		5.125	V
Short circuit current	$V_{REF} = 0\text{ V}$, $T_J = 25^\circ\text{C}$		-60	-15	mA
Error Amplifier					
Error amplifier input voltage		2.4	2.5	2.6	V
Input bias current			0.6	3	μA
AVOL	$1\text{ V} < V_{COMP} < 4\text{ V}$	60	90		dB
PSRR	$11\text{ V} < V_{IN} < 18\text{ V}$	85	100		
Output sink current	$V_{COMP} = 1\text{ V}$	1	2.5		mA
Output source current	$V_{COMP} = 4\text{ V}$		-1.3	-0.5	
Output voltage high	$I_{COMP} = -0.5\text{ mA}$	4	4.7	5	V
Output voltage low	$I_{COMP} = 1\text{ mA}$	0	0.5	1	
Slew rate	$T_A = 25^\circ\text{C}$	6	11		V/ μs

ELECTRICAL CHARACTERISTICS (continued)

Unless specified; $V_C = V_{IN} = V_{UVSEL} = 12\text{ V}$, $C_T = 470\text{ pF}$, $R_T = 9.53\text{ k}$, $R_{DELSETA-B} = R_{DELSEC-D} = 4.8\text{ k}$, $C_{DELSETA-B} = C_{DELSETC-D} = 0.01\text{ }\mu\text{F}$, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWM Comparator					
RAMP offset voltage	$T_J = 25^\circ\text{C}^{(1)}$	1.1	1.25	1.4	V
PWM phase shift, $T_{DELSETA-B}, T_{DELSETC-D} = 0^{(2)}$	$V_{COMP} > V_{RAMPpeak} + V_{RAMPoffset}$	98%	99.7%	102%	
	$V_{COMP} < \text{Zero Phase Shift Voltage}$	0%	0.3%	2%	
Output skew, $T_{DELSETA-B}, T_{DELSETC-D} = 0^{(2)}$	$V_{COMP} > V_{RAMPpeak} + V_{RAMPoffset}$		10		ns
	$V_{COMP} < \text{Zero Phase Shift Voltage}$		10		
Ramp to output delay, $T_{DELSETA-B} = 0, T_{DELSETC-D} = 0$	UC3879, UC2879		115	250	
	UC1879		115	300	
Oscillator					
Initial accuracy	$T_A = 25^\circ\text{C}$	180	200	220	kHz
Voltage stability	$11\text{ V} < V_{IN} < 18\text{ V}$		1	2	%
Total variation	Line, Temperature	160	200	240	kHz
CLKSYNC threshold		2.3	2.5	2.7	V
Clock out high		2.8	4		
Clock out low		0.5	1	1.5	
Clock out pulse width			400	600	ns
Ramp valley voltage			0.2	0.4	V
Ramp peak voltage		2.8	2.9	3.2	
Current Limit					
Input bias	$V_{CS} = 3\text{ V}$		2	10	μA
Threshold voltage		2.35	2.5	2.65	V
Delay to OUTA, B, C, D			160	300	ns
Cycle-by-Cycle Current Limit					
Input bias	$V_{CS} = 2.2\text{ V}$		2	10	μA
Threshold voltage		1.85	2	2.15	V
Delay to output zero phase			110	300	ns

(1) Ramp offset voltage has a temperature coefficient of about $-4\text{ mV}/^\circ\text{C}$.

$$\theta = \frac{200}{T} \phi \%$$

(2) Phase shift percentage ($0\% = 0$, $100\% = 180$) is defined as where θ is the phase shift, and T are defined in Figure 1. At 0% phase shift, θ is the output skew.

ELECTRICAL CHARACTERISTICS (continued)

Unless specified; VC = VIN = V_{UVSEL} = 12 V, CT = 470 pF, RT = 9.53k, R_{DELSETA-B} = R_{DELSEC-D} = 4.8k, C_{DELSETA-B} = C_{DELSETC-D} = 0.01 μF, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Soft Start/Reset Delay					
Charge current	V _{SS} = 0.5 V	-20	-9	-3	μA
Discharge current	V _{SS} = 1 V	120	230		
Restart threshold		4.3	4.7		V
Discharge level			300		mV
Output Drivers					
Output Low level	I _{OUT} = 10 mA		0.3	0.4	V
Output High level	I _{OUT} = -10 mA, Referenced to VC		2.2	3	
Delay Set ⁽³⁾					
Delay time ⁽⁴⁾	R _{DELSETA-B} = R _{DELSETC-D} = 4.8k	250	370	520	ns
Delay time ⁽⁴⁾	R _{DELSETA-B} = R _{DELSETC-D} = 1.9k	100	155	220	
Zero delay ⁽⁵⁾	V _{DELSETA-B} = V _{DELSETC-D} = 5 V		5		

(3) Delay time can be programmed via resistors from the delay set pins to ground.

$$\text{Delay Time} = (0.89 \cdot 10^{-10} \cdot R_{\text{DELAY}}) \text{sec}$$

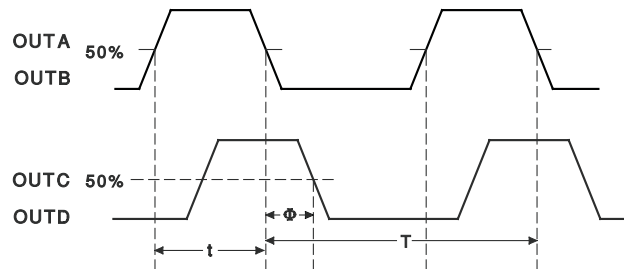
The recommended range for R_{DELAY} is 1.9 kΩ to 10 kΩ.

(4) Delay time is defined as:

$$\text{delay} = T \cdot \left(\frac{1}{2} - \text{duty cycle} \right)$$

where T is defined in Figure 1.

(5) The zero phase shift voltage is the voltage measured at COMP which forces zero phase shift. This condition corresponds to zero effective output power. Zero phase shift voltage has a temperature coefficient of about -2 mV/°C.



$$\text{DutyCycle} = \frac{t}{T}$$

$$\text{Period} = T$$

$$T_{\text{DHL}}(\text{A to C}) = T_{\text{DHL}}(\text{B to D}) =$$

Figure 1. Phase Shift, Output Skew and Delay Time Definitions

PIN DESCRIPTIONS

CLKSYNC (Bi-directional Clock and Synchronization): Used as an output, CLKSNC provides a clock signal. As an input, this pin provides a synchronization point. Multiple UC3879s, each with their own local oscillator frequency, may be connected together by the CLKSNC pin, and they will synchronize to the fastest oscillator. This pin may also be used to synchronize the UC3879 to an external clock, provided the frequency of the external signal is higher than the frequency of the local oscillator. CLKSNC is internally connected to an emitter follower pull-up and a current source pull-down (300 μ A typical). Therefore, an external resistor to GND can be used to improve the CLKSNC pin's ability to drive capacitive loads.

COMP (Error Amplifier Output): This pin is the output of the gain stage for overall feedback control. Error amplifier output voltage levels below 0.9 V forces zero phase shift. Since the error amplifier has a relatively low current drive capability, the output may be overridden by driving it with a sufficiently low impedance source.

CT (Oscillator Frequency Set): After choosing R_T to set the required upper end of the linear duty cycle range, the timing capacitor (CT) value is calculated to set the oscillator frequency as follows:

$$CT = \frac{D_{lin}}{1.08 \cdot R_T \cdot f}$$

Connect the timing capacitor directly between CT and GND. Use a high quality ceramic capacitor with low ESL and ESR for best results. A minimum CT value of 200 pF insures good accuracy and less susceptibility to circuit layout parasitics. The oscillator and PWM are designed to provide practical operation to 600 kHz.

CS (Current Sense): This pin is the non-inverting input to the two current fault comparators whose references are set internally to fixed values of 2 V and 2.5 V. When the voltage at this pin exceeds 2 V, and the error amplifier output voltage exceeds the voltage on the ramp input, the phase shift limiting overcurrent comparator will limit the phase shifting on a cycle-by-cycle basis. When the voltage at this pin exceeds 2.5 V, the current fault latch is set, the outputs are forced OFF, and a soft start cycle is initiated. If a constant voltage above 2.5 V is applied to this pin the outputs are disabled and held low. When CS is brought below 2.5 V, the outputs will begin switching at 0 degrees phase shift before the SS pin begins to rise. This condition will not prematurely deliver power to the load.

DELSETA-B, DELSETC-D (Output Delay Control): The user programmed currents from these pins to GND set the turn on delay for the corresponding output pair. This delay is introduced between the turn off of one switch and the turn on of another in the same leg of the bridge to allow resonant switching to take place. Separate delays are provided for the two half-bridges to accommodate differences in the resonant capacitor charging currents.

EA- (Error Amplifier Inverting Input): This is normally connected to the voltage divider resistors which sense the power supply output voltage level. The loop compensation components are connected between this pin and COMP.

GND (Signal Ground): All voltages are measured with respect to GND. The timing capacitor on CT, and bypass capacitors on VREF and VIN should be connected directly to the ground plane near GND.

OUTA – OUTD (Outputs A-D): The outputs are 100-mA totem pole output drivers optimized to drive FET driver devices. The outputs operate as pairs with a nominal 50% duty cycle. The A-B pair is intended to drive one half-bridge in the external power stage and is synchronized to the clock waveform. The C-D pair drives the other half-bridge with switching phase shifted with respect to the A-B outputs.

PWRGND (Power Ground): VC should be bypassed with a ceramic capacitor from VC to the section of the ground plane that is connected to PWRGND. Any required bulk reservoir capacitor should be connected in parallel. PWRGND and GND should be connected at a single point near the chip to optimize noise rejection and minimize DC voltage drops.

RAMP (Voltage Ramp): This pin is the input to the PWM comparator. Connect it to CT for voltage mode control. For current mode control, connect RAMP to CS and also to the output of the current sense transformer circuit. Slope compensation can be achieved by injecting a portion of the ramp voltage from CT to RAMP.

PIN DESCRIPTIONS (continued)

RT (Clock/Sync Duty Cycle Set Pin): The UC3879 oscillator produces a sawtooth waveform. The rising edge is generated by connecting a resistor from RT to GND and a capacitor from CT to GND (see CT pin description). During the rising edge, the modulator has linear control of the duty cycle. The duty cycle jumps to 100% when the voltage on COMP exceeds the oscillator peak voltage. Selection of RT should be done first, based on the required upper end of the linear duty cycle range (D_{in}) as follows:

$$RT = \frac{2.5}{10 \text{ mA} \cdot (1 - D_{in})}$$

Recommended values for RT range from 2.5 k Ω to 100 k Ω .

SS: Connect a capacitor between this pin and GND to set the soft start time. The voltage at SS will remain near zero volts as long as VIN is below the UVLO threshold. Soft start will be pulled up to about 4.8 V by an internal 9- μ A current source when VIN and VREF become valid (assuming a non-fault condition). In the event of a current fault (CS voltage exceeding 2.5 V), soft start will be pulled to GND and then ramp to 4.8 V. If a fault occurs during the soft start cycle, the outputs will be immediately disabled and soft start must fully charge prior to resetting the fault latch. For paralleled controllers, the soft start pins may be paralleled to a single capacitor, but the charge currents will be additive.

UVSEL: Connecting this pin to VIN sets a turn on voltage of 10.75 V with 1.5 V of UVLO hysteresis. Leaving the pin open-circuited programs a turn on voltage of 15.25 V with 6 V of hysteresis.

VC (Output Switch Supply Voltage): This pin supplies power to the output drivers and their associated bias circuitry. The difference between the output high drive and VC is typically 2.1 V. This supply should be bypassed directly to PWRGND with a low ESR/ESL capacitor.

VIN (Primary Chip Supply Voltage): This pin supplies power to the logic and analog circuitry on the integrated circuit that is not directly associated with driving the output stages. Connect VIN to a stable source above 12 V for normal operation. To ensure proper functionality, the UC3879 is inactive until VIN exceeds the upper undervoltage lockout threshold. This pin should be bypassed directly to GND with a low ESR/ESL capacitor.

NOTE:

When VIN exceeds the UVLO threshold the supply current (I_{IN}) jumps from about 100 A to greater than 20 mA. If the UC3879 is not connected to a well bypassed supply, it may immediately enter the UVLO state again. Therefore, sufficient bypass capacity must be added to ensure reliable startup.

VREF: This pin provides an accurate 5 V voltage reference. It is internally short circuit current limited. VREF is disabled while VIN is below the UVLO threshold. The circuit is also disabled until VREF reaches approximately 4.75 V. For best results bypass VREF with a 0.1 μ F, low ESR/ESL capacitor.

ADDITIONAL INFORMATION

Please refer to the following Unitrode publications for additional information. The following three topics are available in the Applications Handbook.

1. Application Note U-154, *The New UC3879 Phase- Shifted PWM Controller Simplifies the Design of Zero Voltage Transition Full-Bridge Converters*, by Laszlo Balogh.
2. Application Note U-136, *Phase Shifted, Zero Voltage Transition Design Considerations and the UC3875 PWM Controller*, by Bill Andreycak.
3. Design Note DN-63, *The Current-Doubler Rectifier: An Alternative Rectification Technique for Push-Pull and Bridge Converters*, by Laszlo Balogh.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC2879DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2879DW	Samples
UC2879DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2879DW	Samples
UC2879DWTR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2879DW	Samples
UC2879DWTRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2879DW	Samples
UC2879N	ACTIVE	PDIP	N	20	20	Green (RoHS & no Sb/Br)	CU NIPDAU Call TI	N / A for Pkg Type	-40 to 85	UC2879N	Samples
UC2879NG4	ACTIVE	PDIP	N	20	20	Green (RoHS & no Sb/Br)	Call TI	N / A for Pkg Type	-40 to 85	UC2879N	Samples
UC3879DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3879DW	Samples
UC3879DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3879DW	Samples
UC3879DWTR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3879DW	Samples
UC3879DWTRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3879DW	Samples
UC3879N	ACTIVE	PDIP	N	20	20	Green (RoHS & no Sb/Br)	CU NIPDAU Call TI	N / A for Pkg Type	0 to 70	UC3879N	Samples
UC3879NG4	ACTIVE	PDIP	N	20	20	Green (RoHS & no Sb/Br)	Call TI	N / A for Pkg Type	0 to 70	UC3879N	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2879DWTR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
UC3879DWTR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2879DWTR	SOIC	DW	20	2000	367.0	367.0	45.0
UC3879DWTR	SOIC	DW	20	2000	367.0	367.0	45.0

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.