SINGLE 9-A HIGH-SPEED LOW-SIDE MOSFET DRIVER WITH ENABLE

Check for Samples: UCC27322-EP

FEATURES

- **Industry-Standard Pinout With Addition of Enable Function**
- **High-Peak Current Drive Capability of ±9 A at the Miller Plateau Region Using TrueDrive™**
- **Efficient Constant Current Sourcing Using a Unique Bipolar and CMOS Output Stage**
- **TTL-/CMOS-Compatible Inputs Independent of Supply Voltage**
- **20-ns Typical Rise and 15-ns Typical Fall Times With 10-nF Load**
- **Typical Propagation Delay Times of 25 ns With Input Falling and 35 ns With Input Rising**
- **4-V to 15-V Supply Voltage**
- **Pb-Free Finish (NiPdAu)**

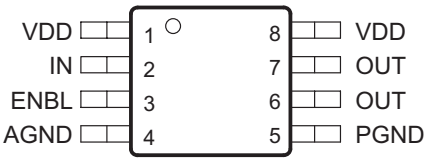
SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Rated From –55°C to 125°C**
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

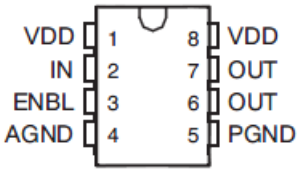
APPLICATIONS

- **Switch-Mode Power Supplies**
- **DC/DC Converters**
- **Motor Controllers**
- **Line Drivers**
- **Class D Switching Amplifiers**
- **Pulse Transformer Driver**

DGK PACKAGE
(TOP VIEW)

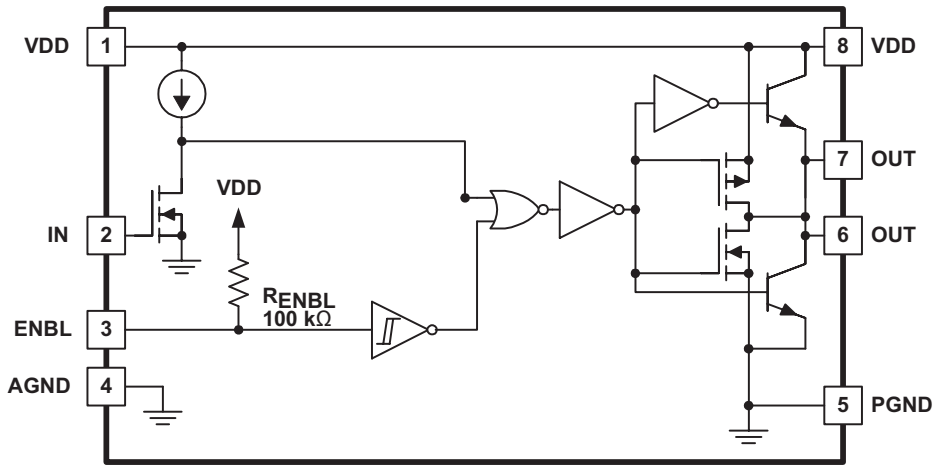


D PACKAGE
(TOP VIEW)



DESCRIPTION

The UCC27322 delivers 9 A of peak drive current in an industry standard pinout. These drivers can drive the largest of MOSFETs for systems requiring extreme Miller current due to high dV/dt transitions. This eliminates additional external circuits and can replace multiple components to reduce space, design complexity and assembly cost.



INPUT/OUTPUT TABLE

ENBL	IN	OUT
0	0	0
0	1	0
1	0	0
1	1	1

Using a design that inherently minimizes shoot-through current, the outputs of these can provide high gate drive current where it is most needed at the Miller plateau region during the MOSFET switching transition. A unique hybrid output stage paralleling bipolar and MOSFET transistors (TrueDrive) allows efficient current delivery at low supply voltages. With this drive architecture, UCC27322 can be used in industry standard 6-A, 9-A and many 12-A driver applications. Latch up and ESD protection circuits are also included. Finally, the UCC27322 provides an enable (ENBL) function to have better control of the operation of the driver applications. ENBL is implemented on pin 3 which was previously left unused in the industry standard pin-out. It is internally pulled up to V_{DD} for active high logic and can be left open for standard operation.

ORDERING INFORMATION(1)

T_A	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
–40°C to 105°C	DGK	Reel of 2500	UCC27322TDGKREP	QTK	V62/11601-01XE
–55°C to 125°C	D	Reel of 2500	UCC27322MDREP	27322M	V62/11601-02YE
		Tube of 75	UCC27322MDEP	27322M	V62/11601-02YE-T

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

Table 1. TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NO.	NAME		
4	AGND	—	Common ground for input stage. This ground should be connected very closely to the source of the power MOSFET which the driver is driving. Grounds are separated to minimize ringing affects due to output switching di/dt which can affect the input threshold.
3	ENBL	I	Enable input for the driver with logic compatible threshold and hysteresis. The driver output can be enabled and disabled with this pin. It is internally pulled up to VDD with 100-kΩ resistor for active high operation. The output state when the device is disabled will be low regardless of the input state.
2	IN	I	Input signal of the driver which has logic compatible threshold and hysteresis.
6, 7	OUT	O	Driver outputs that must be connected together externally. The output stage is capable of providing 9-A peak drive current to the gate of a power MOSFET.
5	PGND	—	Common ground for output stage. This ground should be connected very closely to the source of the power MOSFET which the driver is driving. Grounds are separated to minimize ringing affects due to output switching di/dt which can affect the input threshold.
1, 8	VDD	I	Supply voltage and the power input connections for this device. Three pins must be connected together externally.

ABSOLUTE MAXIMUM RATINGS(1) (2)

over operating free-air temperature range (unless otherwise noted)

V_{DD}	Supply voltage		–0.3 V to 16 V
I_O	Output current, OUT		0.6 A
V_I	Input voltage	IN	-0.3 V to 6 V or V_{DD} + 0.3 V (whichever is larger)
		ENBL	-0.3 V to 6 V or V_{DD} + 0.3 V (whichever is larger)
	Latch-up protection(3)	IN, OUT	500 mA
T_J	Junction operating temperature		–55°C to 150°C
T_{stg}	Storage temperature		–65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND. Currents are positive into and negative out of the specified terminal.
(3) Specified by design

THERMAL INFORMATION

THERMAL METRIC		UCC27322		UNITS
		DGK	D	
		8 PINS	8 PINS	
θ_{JA}	Junction-to-ambient thermal resistance(1)	161.8	116.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(2)	56.2	70.8	
θ_{JB}	Junction-to-board thermal resistance(3)	81.1	56.6	
ψ_{JT}	Junction-to-top characterization parameter(4)	5.7	22.8	
ψ_{JB}	Junction-to-board characterization parameter(5)	79.8	56.1	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(6)	N/A	N/A	

(1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(4) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(5) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

OVERALL ELECTRICAL CHARACTERISTICS

V_{DD} = 4.5 V to 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	DGK PACKAGE $T_J = T_A$ = -40°C to 105°C			D PACKAGE $T_J = T_A$ = -55°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
I_{DD}	Static operating current	IN = Low, ENBL = Low, V_{DD} = 15 V		150	225		225	µA
		IN = High, ENBL = Low, V_{DD} = 15 V		450	650		650	
		IN = Low, ENBL = High, V_{DD} = 15 V		75	125		125	
		IN = High, ENBL = High, V_{DD} = 15 V		675	1000		1000	

INPUT (IN) ELECTRICAL CHARACTERISTICS

V_{DD} = 4.5 V to 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	DGK PACKAGE $T_J = T_A$ = -40°C to 105°C			D PACKAGE $T_J = T_A$ = -55°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
V_{IH}	Logic 1 input threshold		2			2		V
V_{IL}	Logic 0 input threshold				1		1	V
	Input current	0 V ≤ V_{IN} ≤ V_{DD}	–10	0	10	–10	10	µA

OUTPUT (OUT) ELECTRICAL CHARACTERISTICS

V_{DD} = 4.5 V to 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	DGK PACKAGE $T_J = T_A$ = -40°C to 105°C			D PACKAGE $T_J = T_A$ = -55°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
	Peak output current(1) (2)	V_{DD} = 14 V		9				A
V_{OH}	High-level output voltage	$V_{OH} = V_{DD} – V_{OUT}$, I_{OUT} = –10 mA		150	300		300	mV
V_{OL}	Low-level output voltage	I_{OUT} = 10 mA		11	25		25	mV
	Output resistance high(3)	I_{OUT} = –10 mA, V_{DD} = 14 V		15	25		25	Ω
	Output resistance low(3)	I_{OUT} = 10 mA, V_{DD} = 14 V		1.1	2.5		2.5	Ω

(1) Specified by design
(2) The pullup/pulldown circuits of the driver are bipolar and MOSFET transistors in parallel. The pulsed output current rating is the combined current from the bipolar and MOSFET transistors.
(3) The pullup/pulldown circuits of the driver are bipolar and MOSFET transistors in parallel. The output resistance is the $R_{DS(ON)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor.

ENABLE (ENBL) ELECTRICAL CHARACTERISTICS

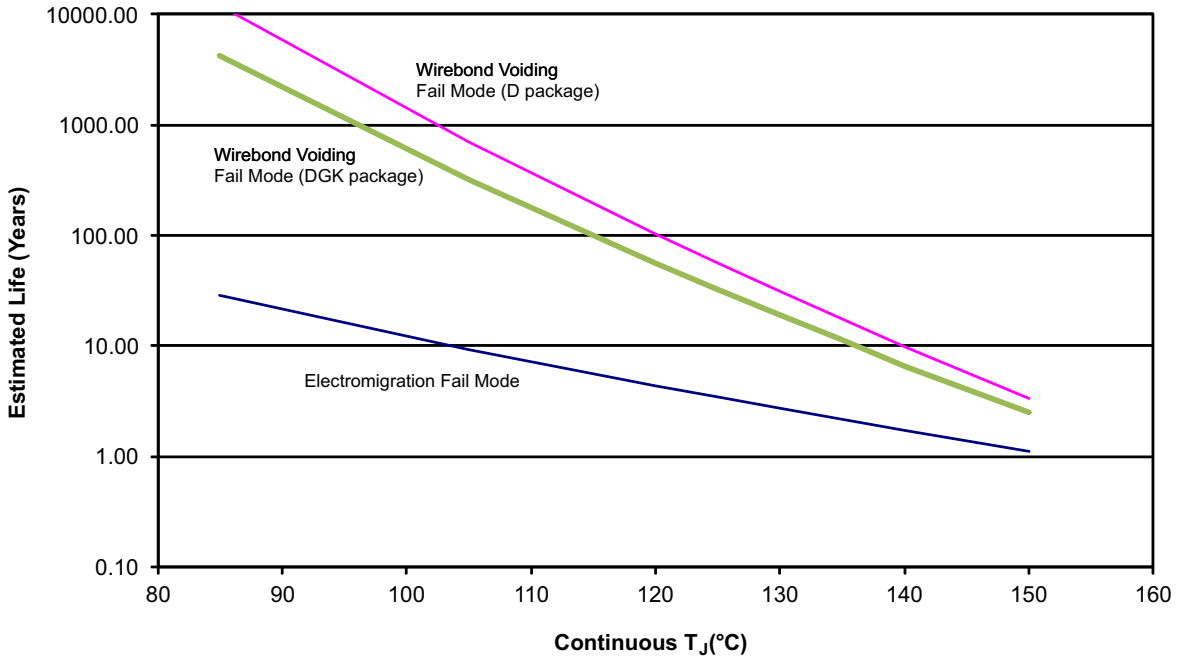
V_{DD} = 4.5 V to 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	DGK PACKAGE $T_J = T_A$ = -40°C to 105°C			D PACKAGE $T_J = T_A$ = -55°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
V_{EN_H}	Enable rising threshold voltage	Low to high transitions	1.7	2.2	2.7	1.5	3.4	V
V_{EN_L}	Enable falling threshold voltage	High to low transition	1.1	1.6	2	1.1	2.2	V
	Hysteresis		0.25	0.55	0.90	0.18	1.15	V
$R_{(ENBL)}$	Enable impedance	V_{DD} = 14 V, ENBL = Low	75	100	135	75	180	kΩ
t_{D3}	Propagation delay time	C_{LOAD} = 10 nF (see Figure 3)		60	90		95	ns
t_{D4}	Propagation delay time	C_{LOAD} = 10 nF (see Figure 3)		60	90		95	ns

SWITCHING CHARACTERISTICS

V_{DD} = 4.5 V to 15 V (unless otherwise noted) (see Figure 2)

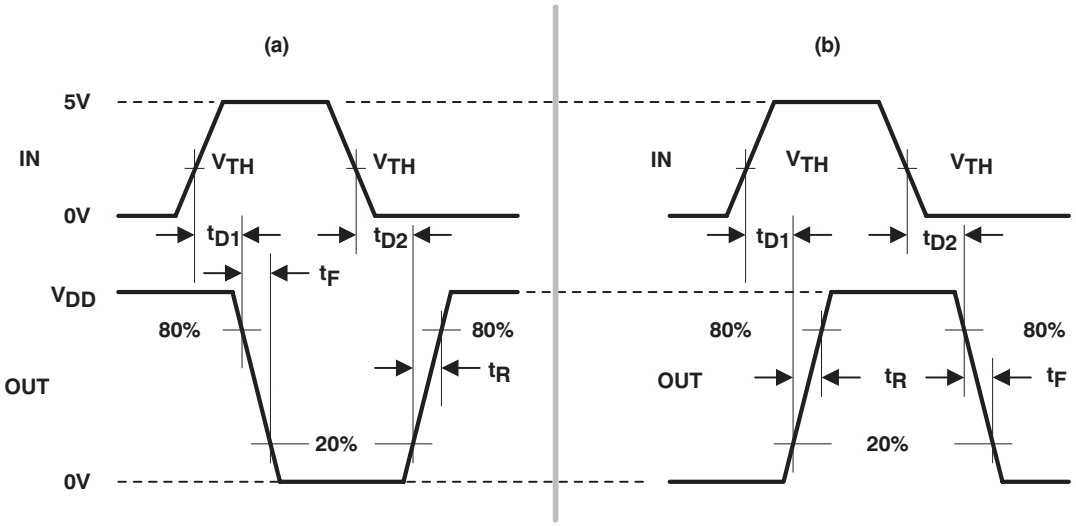
PARAMETER		TEST CONDITIONS	DGK PACKAGE $T_J = T_A$ = -40°C to 105°C			D PACKAGE $T_J = T_A$ = -55°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_R	Rise time (OUT)	C_{LOAD} = 10 nF		20	70		77	ns
t_F	Fall time (OUT)	C_{LOAD} = 10 nF		20	30		35	ns
t_{D1}	Delay time, IN rising (IN to OUT)	C_{LOAD} = 10 nF		25	70		75	ns
t_{D2}	Delay time, IN falling (IN to OUT)	C_{LOAD} = 10 nF		35	70		75	ns



Notes:

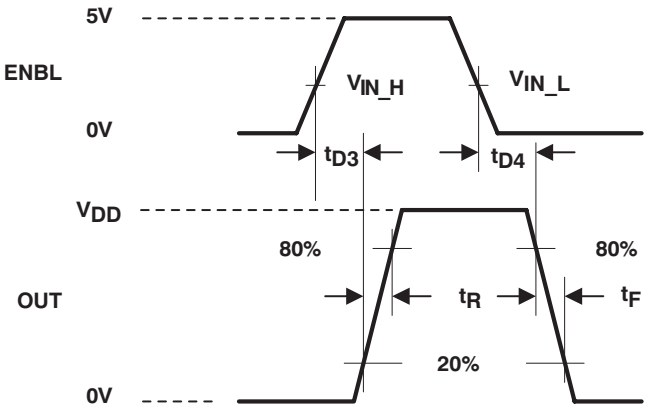
1. See data sheet for absolute maximum and minimum recommended operating conditions.
2. Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).
3. Enhanced plastic product disclaimer applies.
4. Electromigration calculation is based on operating the part at 2.5 MHz at a 50% duty cycle.

Figure 1. UCC27322 Operating Life Derating Chart



A. The 20% and 80% thresholds depict the dynamics of the Bipolar output devices that dominate the power MOSFET transition through the Miller regions of operation.

Figure 2. Switching Waveforms for (a) Inverting Driver and (b) Noninverting Driver



A. The 20% and 80% thresholds depict the dynamics of the Bipolar output devices that dominate the power MOSFET transition through the Miller regions of operation.

Figure 3. Switching Waveforms for Enable to Output

TYPICAL CHARACTERISTICS

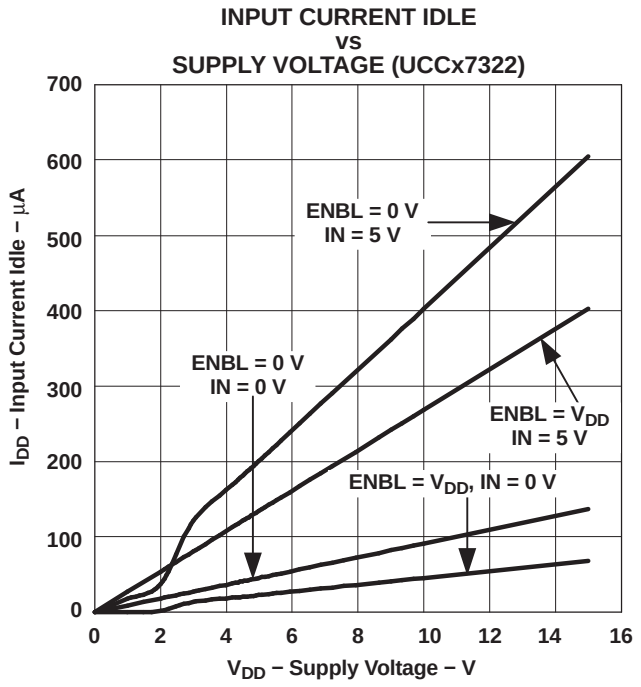


Figure 4.

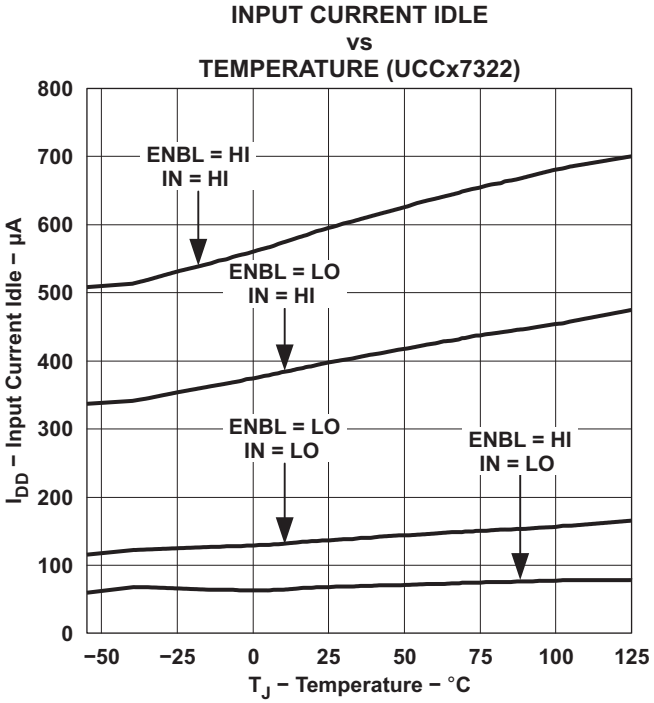


Figure 5.

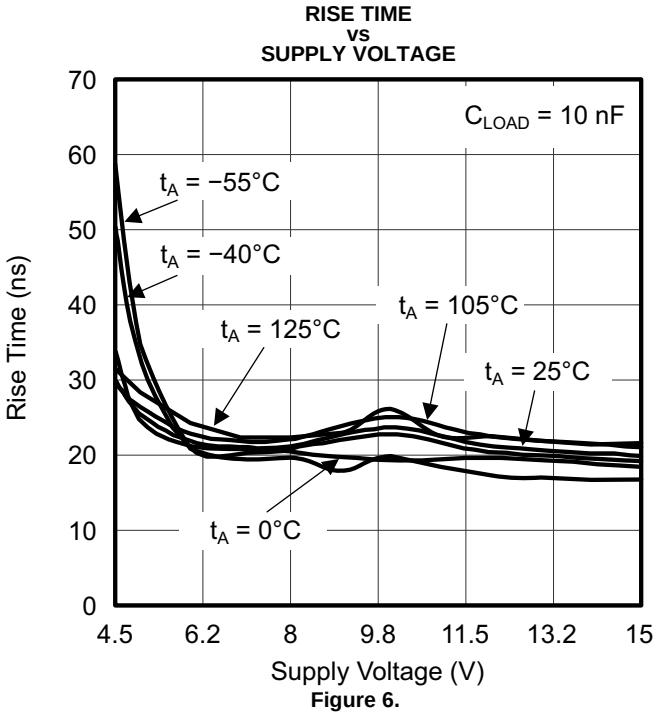


Figure 6.

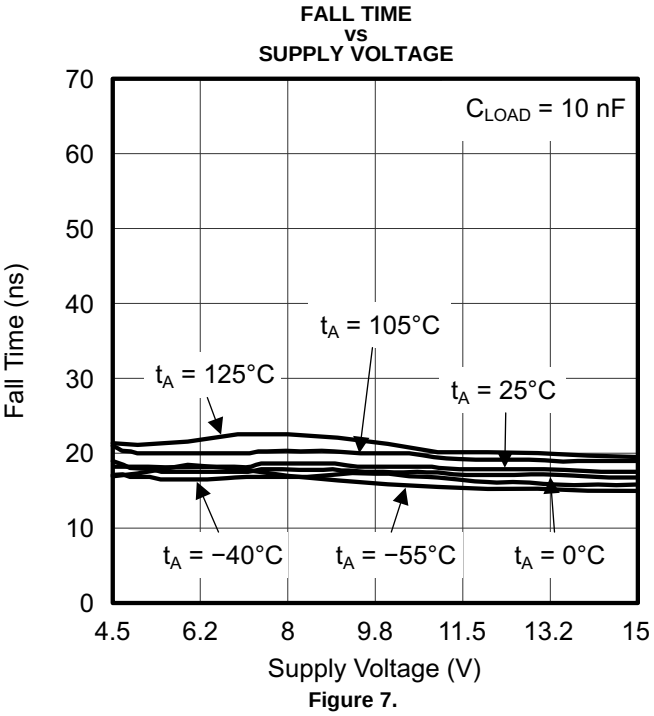


Figure 7.

TYPICAL CHARACTERISTICS (continued)

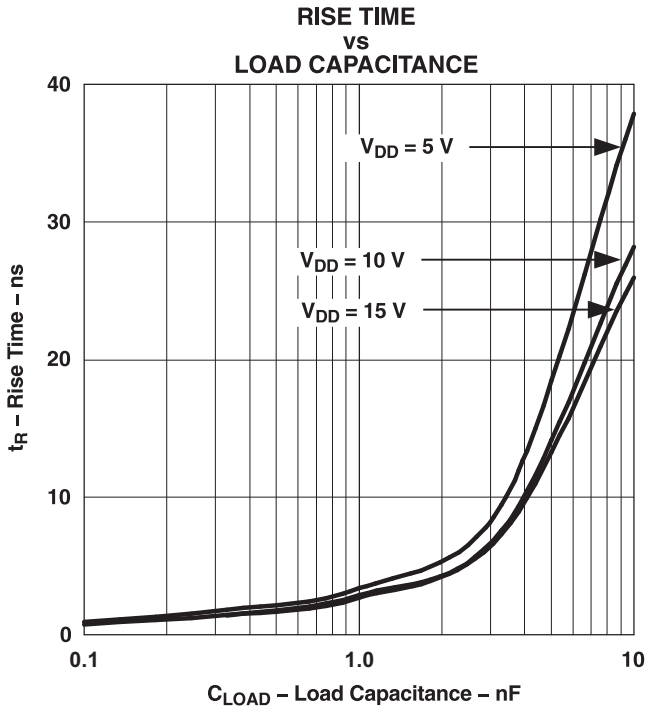


Figure 8.

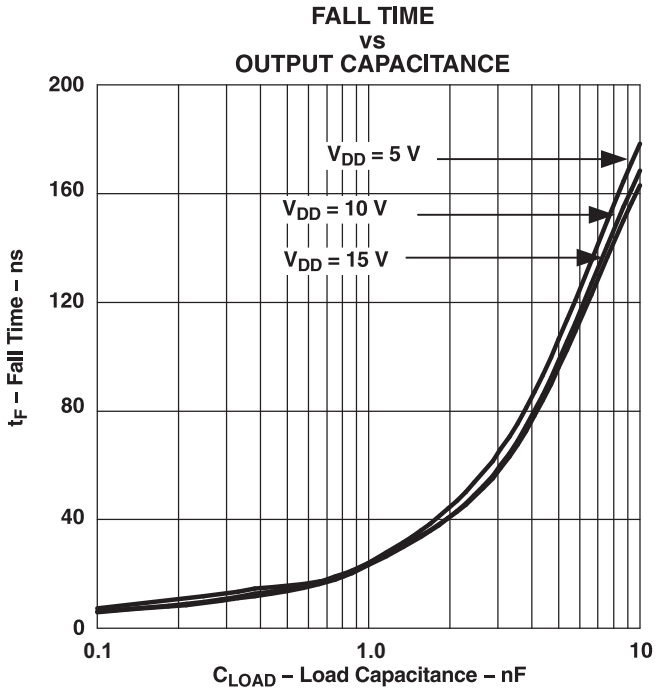


Figure 9.

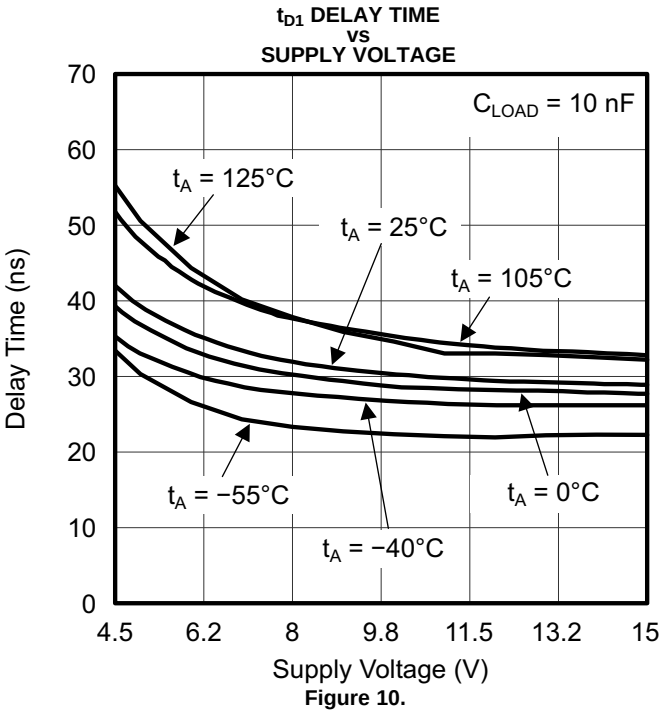


Figure 10.

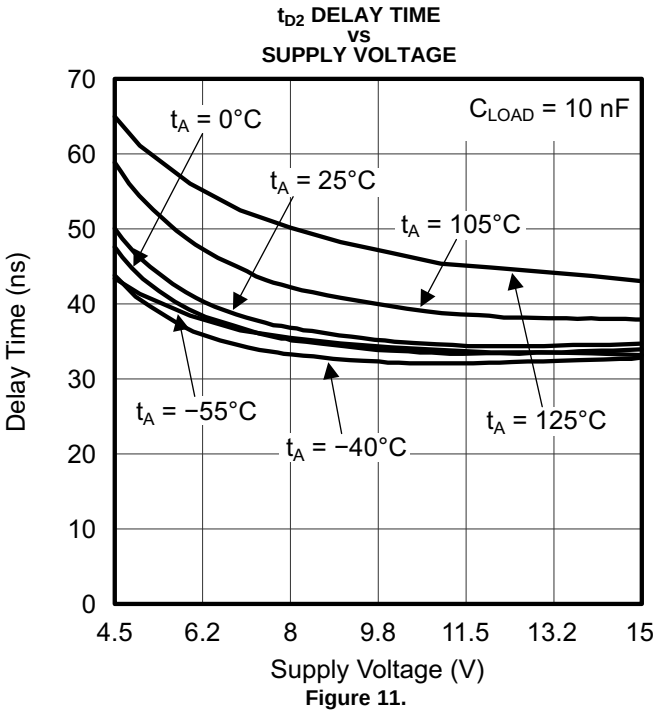


Figure 11.

TYPICAL CHARACTERISTICS (continued)

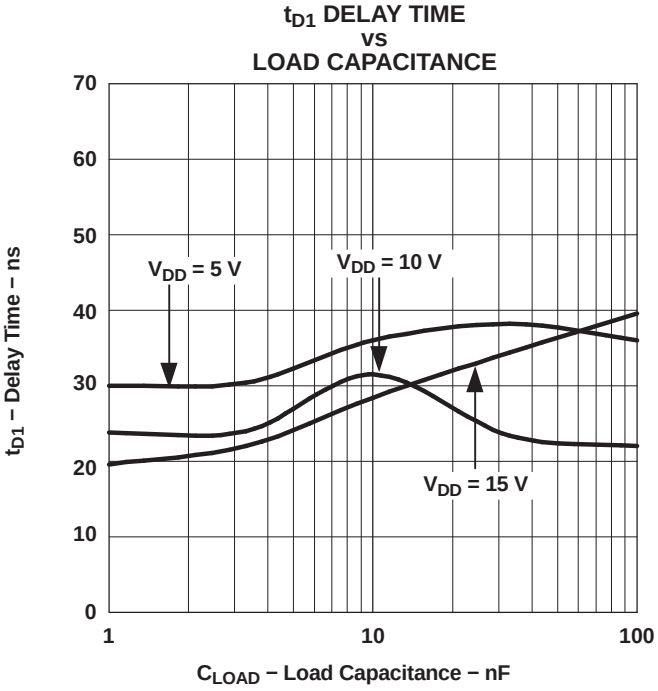


Figure 12.

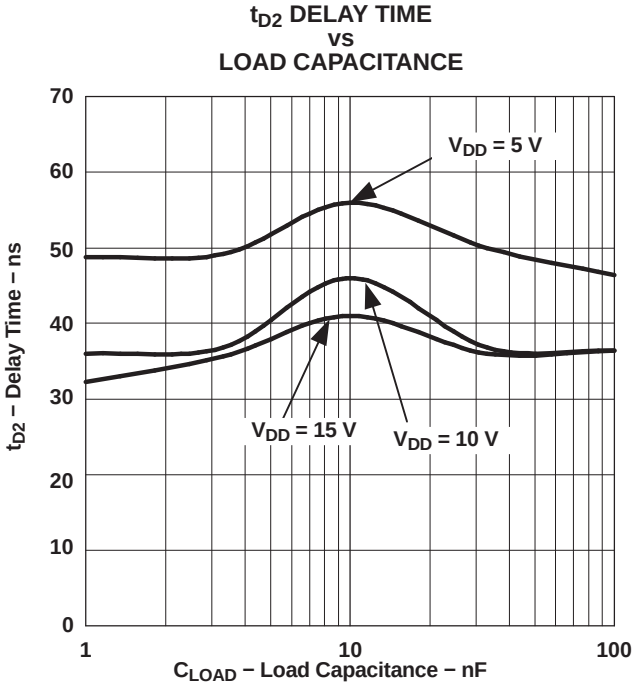


Figure 13.

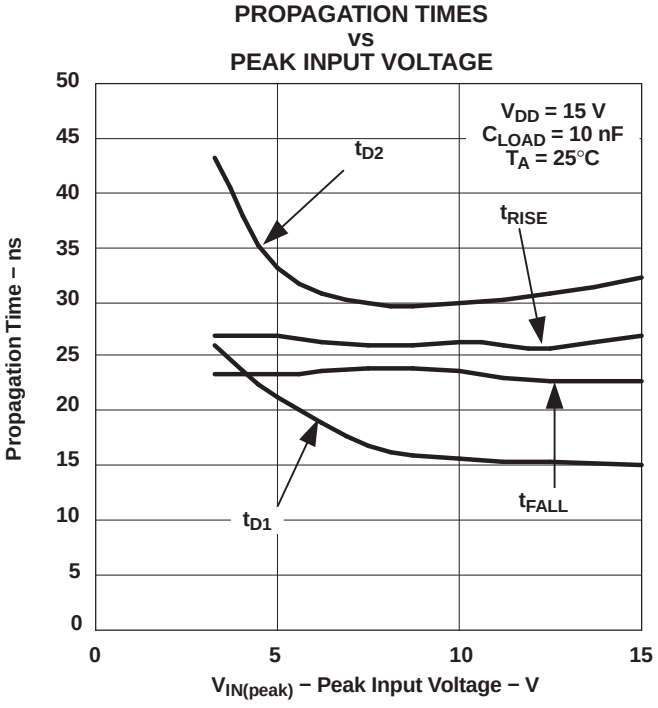


Figure 14.

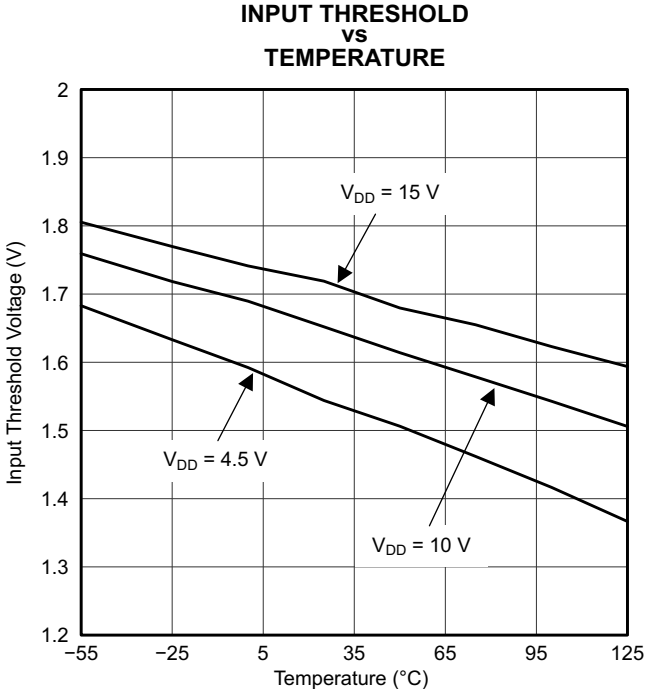


Figure 15.

TYPICAL CHARACTERISTICS (continued)

ENABLE THRESHOLD AND HYSTERESIS vs TEMPERATURE

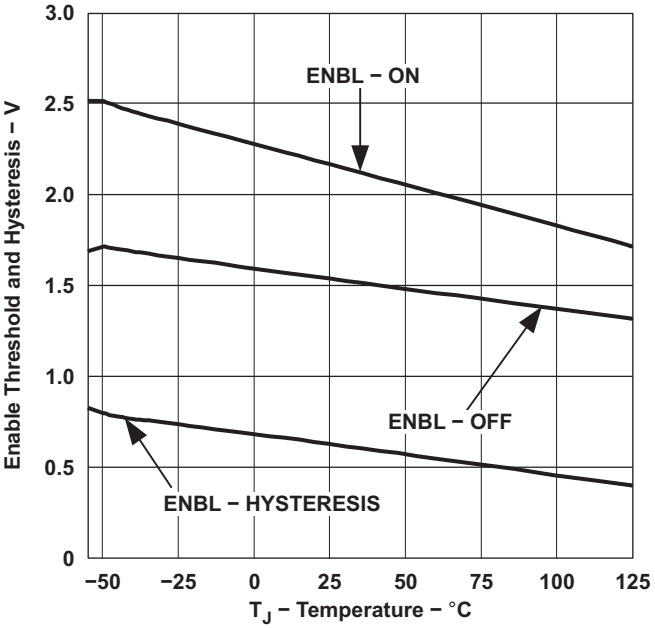


Figure 16.

ENABLE RESISTANCE vs TEMPERATURE

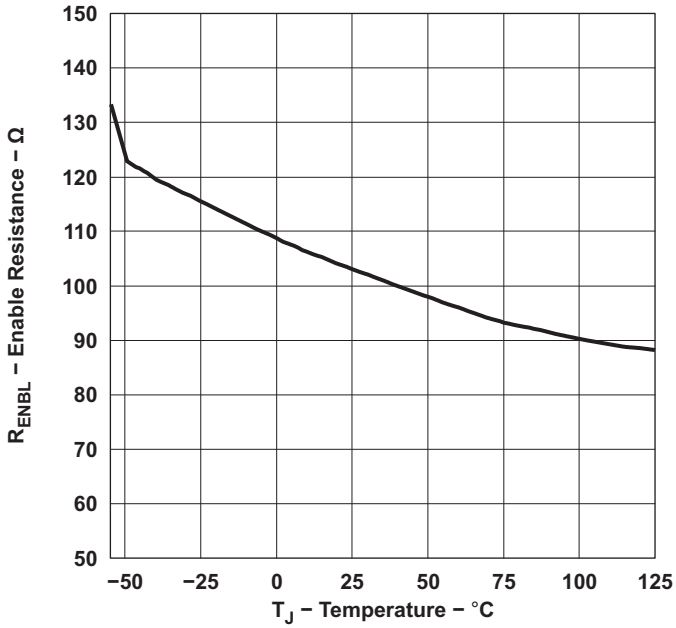


Figure 17.

OUTPUT BEHAVIOR vs VDD (UCC37322)

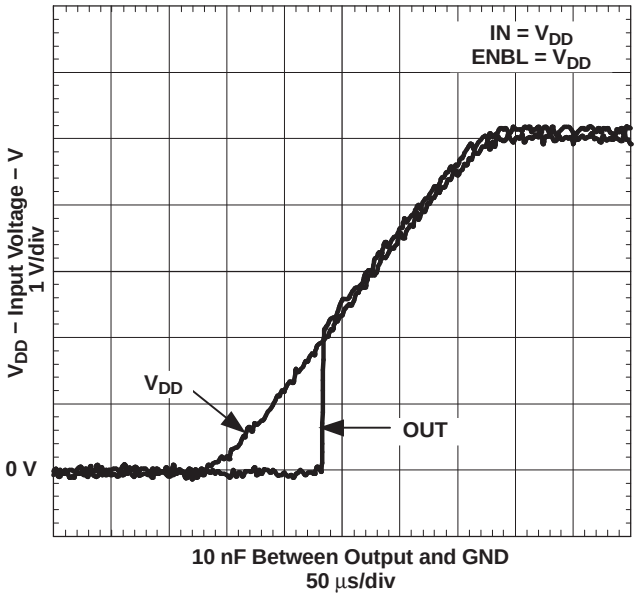


Figure 18.

OUTPUT BEHAVIOR vs VDD (UCC37322)

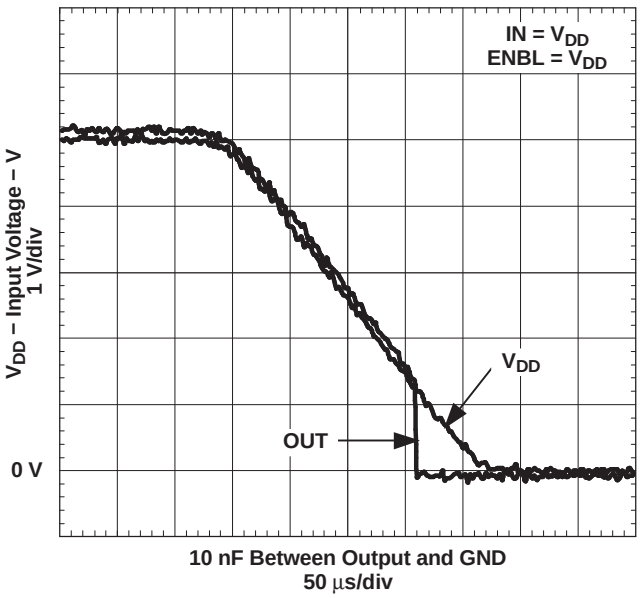


Figure 19.

TYPICAL CHARACTERISTICS (continued)

OUTPUT BEHAVIOR vs VDD (NON-INVERTING)

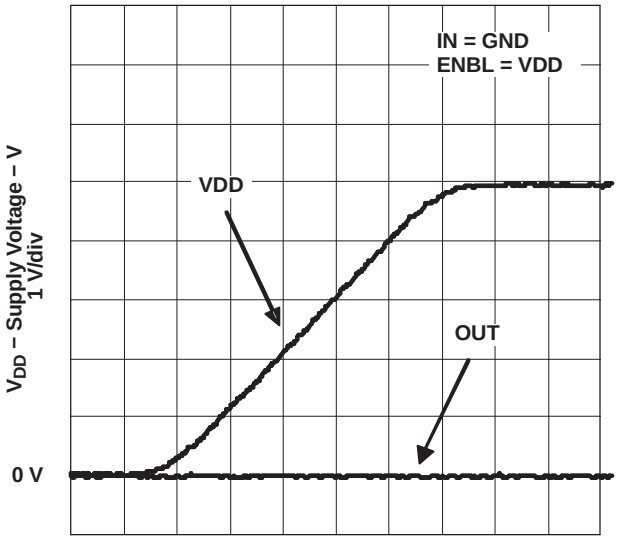


Figure 20.

OUTPUT BEHAVIOR vs VDD (NON-INVERTING)

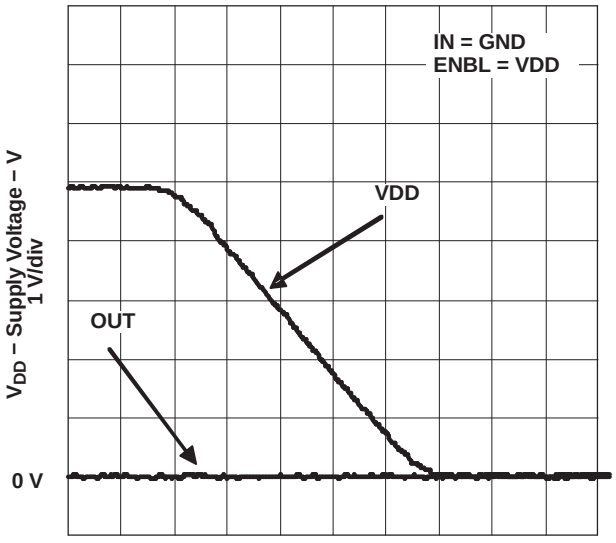


Figure 21.

APPLICATION INFORMATION

General Information

The UCC27322 driver serves as an interface between low-power controllers and power MOSFETs. It can also be used as an interface between DSPs and power MOSFETs. High-frequency power supplies often require high-speed, high-current drivers such as the UCC27322. A leading application is the need to provide a high power buffer stage between the PWM output of the control device and the gates of the primary power MOSFET or IGBT switching devices. In other cases, the device drives the power device gates through a drive transformer. Synchronous rectification supplies also have the need to simultaneously drive multiple devices which can present an extremely large load to the control circuitry.

MOSFET gate drivers are generally used when it is not feasible to have the primary PWM regulator device directly drive the switching devices for one or more reasons. The PWM device may not have the brute drive capability required for the intended switching MOSFET, limiting the switching performance in the application. In other cases there may be a desire to minimize the effect of high frequency switching noise by placing the high current driver physically close to the load. Also, newer devices that target the highest operating frequencies may not incorporate onboard gate drivers at all. Their PWM outputs are only intended to drive the high impedance input to a driver such as the UCC27322. Finally, the control device may be under thermal stress due to power dissipation, and an external driver can help by moving the heat from the controller to an external package.

Input Stage

The IN threshold has a 3.3-V logic sensitivity over the full range of V_{DD} voltages; yet, it is equally compatible with 0 V to V_{DD} signals. The inputs of UCC27322 driver is designed to withstand 500-mA reverse current without either damage to the device or logic upset. In addition, the input threshold turn-off of the UCC27322 has been slightly raised for improved noise immunity. The input stage of each driver should be driven by a signal with a short rise or fall time. This condition is satisfied in typical power supply applications, where the input signals are provided by a PWM controller or logic gates with fast transition times (<200 ns). The IN input of the driver functions as a digital gate, and it is not intended for applications where a slow changing input voltage is used to generate a switching output when the logic threshold of the input section is reached. While this may not be harmful to the driver, the output of the driver may switch repeatedly at a high frequency.

Users should not attempt to shape the input signals to the driver in an attempt to slow down (or delay) the signal at the output. If limiting the rise or fall times to the power device is desired, then an external resistance can be added between the output of the driver and the load device, which is generally a power MOSFET gate. The external resistor may also help remove power dissipation from the device package.

Output Stage

The TrueDrive output stage is capable of supplying ±9-A peak current pulses and swings to both VDD and GND and can encourage even the most stubborn MOSFETs to switch. The pull-up/pull-down circuits of the driver are constructed of bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the RDS(ON) of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor. Each output stage also provides a very low impedance to overshoot and undershoot due to the body diode of the internal MOSFET. This means that in many cases, external-schottky-clamp diodes are not required.

This unique Bipolar and MOSFET hybrid output architecture (TrueDrive) allows efficient current sourcing at low supply voltages. The UCC27322 delivers 9 A of gate drive where it is most needed during the MOSFET switching transition – at the Miller plateau region – providing improved efficiency gains.

Source/Sink Capabilities During Miller Plateau

Large power MOSFETs present a large load to the control circuitry. Proper drive is required for efficient, reliable operation. The UCC27322 driver has been optimized to provide maximum drive to a power MOSFET during the Miller plateau region of the switching transition. This interval occurs while the drain voltage is swinging between the voltage levels dictated by the power topology, requiring the charging/discharging of the drain-gate capacitance with current supplied or removed by the driver.

Two circuits are used to test the current capabilities of the UCC27322 driver. In each case, external circuitry is added to clamp the output near 5 V while the device is sinking or sourcing current. An input pulse of 250 ns is applied at a frequency of 1 kHz in the proper polarity for the respective test. In each test, there is a transient period when the current peaked up and then settled down to a steady-state value. The noted current measurements are made at a time of 200 ns after the input pulse is applied, after the initial transient.

The circuit in Figure 22 is used to verify the current sink capability when the output of the driver is clamped at approximately 5 V, a typical value of gate-source voltage during the Miller plateau region. The UCC27322 is found to sink 9 A at VDD = 15 V.

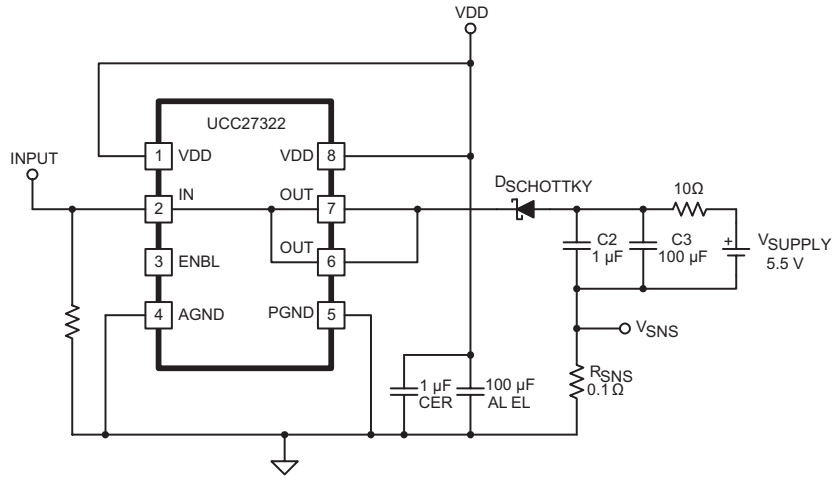


Figure 22. Sink Current Test Circuit

The circuit in Figure 23 is used to test the current source capability with the output clamped to approximately 5 V with a string of Zener diodes. The UCC27322 is found to source 9 A at VDD = 15 V.

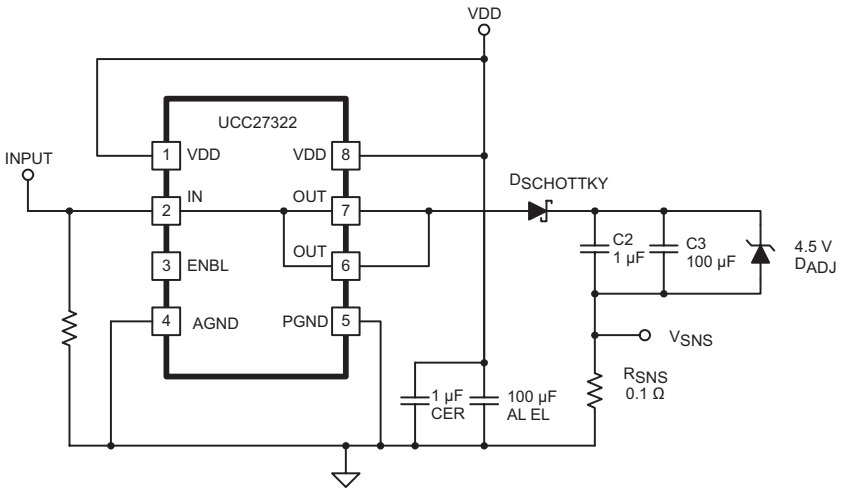


Figure 23. Source Current Test Circuit

It should be noted that the current-sink capability is slightly stronger than the current source capability at lower VDD. This is due to the differences in the structure of the bipolar-MOSFET power output section, where the current source is a P-channel MOSFET and the current sink has an N-channel MOSFET.

In a large majority of applications, it is advantageous that the turn-off capability of a driver is stronger than the turn-on capability. This helps to ensure that the MOSFET is held off during common power-supply transients that may turn the device back on.

Operational Circuit Layout

It can be a significant challenge to avoid the overshoot/undershoot and ringing issues that can arise from circuit layout. The low impedance of these drivers and their high di/dt can induce ringing between parasitic inductances and capacitances in the circuit. Utmost care must be used in the circuit layout.

In general, position the driver physically as close to its load as possible. Place a 1-µF bypass capacitor as close to the output side of the driver as possible, connecting it to pins 1 and 8. Connect a single trace between the two VDD pins (pin 1 and pin 8); connect a single trace between PGND and AGND (pin 5 and pin 4). If a ground plane is used, it may be connected to AGND; do not extend the plane beneath the output side of the package (pins 5 - 8). Connect the load to both OUT pins (pins 7 and 6) with a single trace on the adjacent layer to the component layer; route the return current path for the output on the component side, directly over the output path.

Extreme conditions may require decoupling the input power and ground connections from the output power and ground connections. The UCC27322 has a feature that allows the user to take these extreme measures, if necessary. There is a small amount of internal impedance of about 15 Ω between the AGND and PGND pins; there is also a small amount of impedance (~30 Ω) between the two VDD pins. In order to take advantage of this feature, connect a 1-µF bypass capacitor between VDD and PGND (pins 5 and 8) and connect a 0.1-µF bypass capacitor between VDD and AGND (pins 1 and 4). Further decoupling can be achieved by connecting between the two VDD pins with a jumper that passes through a 40-MHz ferrite bead and connect bias power only to pin 8. Even more decoupling can be achieved by connecting between AGND and PGND with a pair of anti-parallel diodes (anode connected to cathode and cathode connected to anode).

VDD

Although quiescent VDD current is very low, total supply current is higher, depending on OUT current and the programmed oscillator frequency. Total VDD current is the sum of quiescent VDD current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Q_g), average OUT current can be calculated from:

$I_{OUT} = Q_g \times f$

Where f is frequency

For the best high-speed circuit performance, two VDD bypass capacitors are recommended to prevent noise problems. The use of surface-mount components is highly recommended. A 0.1-µF ceramic capacitor should be located closest to the VDD to ground connection. In addition, a larger capacitor (such as 1-µF) with relatively low ESR should be connected in parallel, to help deliver the high current peaks to the load. The parallel combination of capacitors should present a low-impedance characteristic for the expected current levels in the driver application.

Drive Current and Power Requirements

The UCC27322 is capable of delivering 9-A of current to a MOSFET gate for a period of several hundred nanoseconds. High peak current is required to turn an N-channel device ON quickly. Then, to turn the device OFF, the driver is required to sink a similar amount of current to ground. This repeats at the operating frequency of the power device. An N-channel MOSFET is used in this discussion because it is the most common type of switching device used in high frequency power conversion equipment.

References 1 and 2 contain detailed discussions of the drive current required to drive a power MOSFET and other capacitive-input switching devices. Much information is provided in tabular form to give a range of the current required for various devices at various frequencies. The information pertinent to calculating gate drive current requirements are summarized here; the original document is available from the TI web site (www.ti.com).

When a driver is tested with a discrete capacitive load, it is a fairly simple matter to calculate the power that is required from the bias supply. The energy that must be transferred from the bias supply to charge the capacitor is given by:

$E = ½CV^2$

Where C is the load capacitor and V is the bias voltage feeding the driver

There is an equal amount of energy transferred to ground when the capacitor is discharged. This leads to a power loss given by:

$P = 2 \times ½CV^2f$

Where f is the switching frequency

This power is dissipated in the resistive elements of the circuit. Thus, with no external resistor between the driver and gate, this power is dissipated inside the driver. Half of the total power is dissipated when the capacitor is charged, and the other half is dissipated when the capacitor is discharged. An actual example using the conditions of the previous gate drive waveform should help clarify this.

With V_{DD} = 12 V, C_{LOAD} = 10 nF, and f = 300 kHz, the power loss can be calculated as:

$P = 10\ nF \times (12)^2 \times (300\ kHz) = 0.432\ W$

With a 12-V supply, this equates to a current of:

$I = P / V = 0.432\ W / 12\ V = 0.036\ A$

The switching load presented by a power MOSFET can be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain of the device between the on and off states. Most manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Q_g, one can determine the power that must be dissipated when charging a capacitor. This is done by using the equivalence Q_g = CeffV to provide the following equation for power:

$P = C \times V^2 \times f = Q_g \times V \times f$

This equation allows a power designer to calculate the bias power required to drive a specific MOSFET gate at a specific bias voltage.

ENABLE

UCC27322 provides an Enable input for improved control of the driver operation. This input also incorporates logic compatible thresholds with hysteresis. It is internally pulled up to VDD with 100-kΩ resistor for active high operation. When ENBL is high, the device is enabled and when ENBL is low, the device is disabled. The default state of the ENBL pin is to enable the device and therefore can be left open for standard operation. The output state when the device is disabled is low regardless of the input state. See the truth table below for the operation using enable logic.

ENBL input is compatible with both logic signals and slow changing analog signals. It can be directly driven or a power-up delay can be programmed with a capacitor between ENBL and AGND.

Table 2. Input/Ouput Table

	ENBL	IN	OUT
UCC27322	0	0	0
	0	1	0
	1	0	0
	1	1	1

References

1. Power Supply Seminar SEM-1400 Topic 2: *Design And Application Guide For High Speed MOSFET Gate Drive Circuits*, Laszlo Balogh (SLUP133)
2. *Practical Considerations in High Performance MOSFET, IGBT and MCT Gate Drive Circuits*, Bill Andreycak (SLUA105)
3. *PowerPad Thermally Enhanced Package* (SLMA002)
4. *PowerPAD Made Easy* (SLMA004)

Related Products

Table 3. Related Products

PRODUCT	DESCRIPTION	PACKAGES
UCC37323/4/5	Dual 4-A Low-Side Drivers	MSOP-8 PowerPAD, SOIC-8, PDIP-8
UCC27423/4/5	Dual 4-A Low-Side Drivers with Enable	MSOP-8 PowerPAD, SOIC-8, PDIP-8
TPS2811/12/13	Dual 2-A Low-Side Drivers with Internal Regulator	TSSOP-8, SOIC-8, PDIP-8
TPS2814/15	Dual 2-A Low-Side Drivers with Two Inputs per Channel	TSSOP-8, SOIC-8, PDIP-8
TPS2816/17/18/19	Single 2-A Low-Side Driver with Internal Regulator	5-Pin SOT-23
TPS2828/29	Single 2-A Low-Side Driver	5-Pin SOT-23

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27322MDEP	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	27322M	Samples
UCC27322MDREP	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	27322M	Samples
UCC27322TDGKREP	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	QTK	Samples
V62/11601-01XE	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	QTK	Samples
V62/11601-02YE	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	27322M	Samples
V62/11601-02YE-T	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	27322M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF UCC27322-EP :

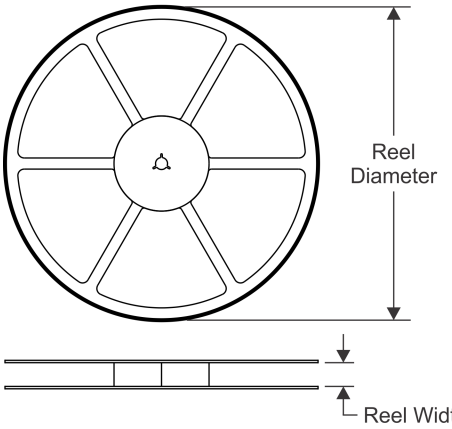
- Catalog: UCC27322
- Automotive: UCC27322-Q1

NOTE: Qualified Version Definitions:

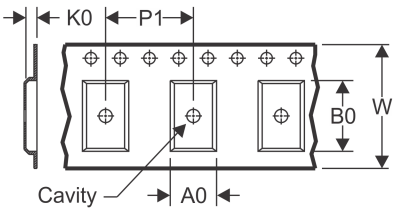
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

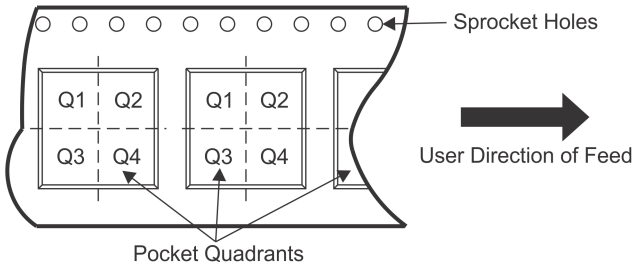


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

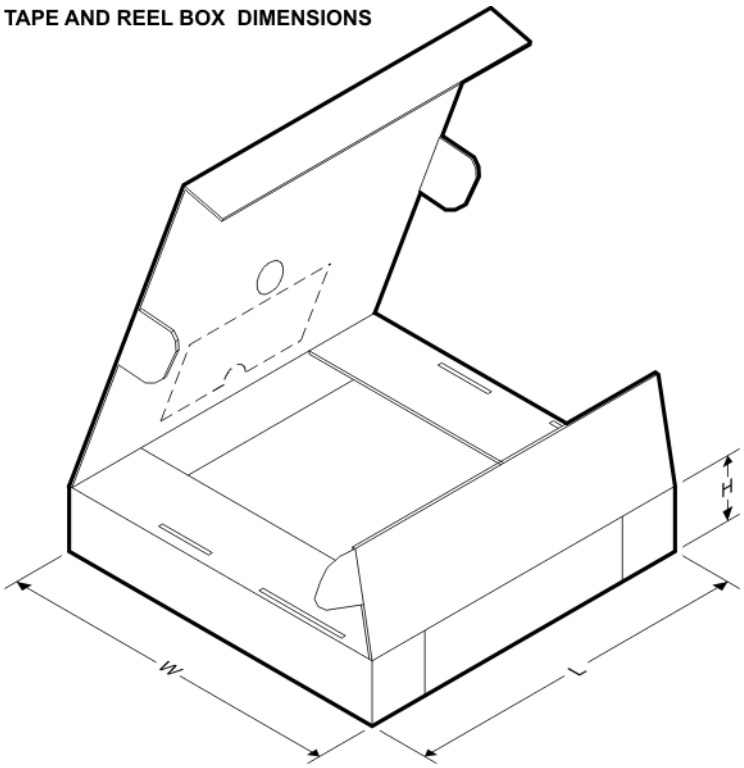
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27322MDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27322TDGKREP	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

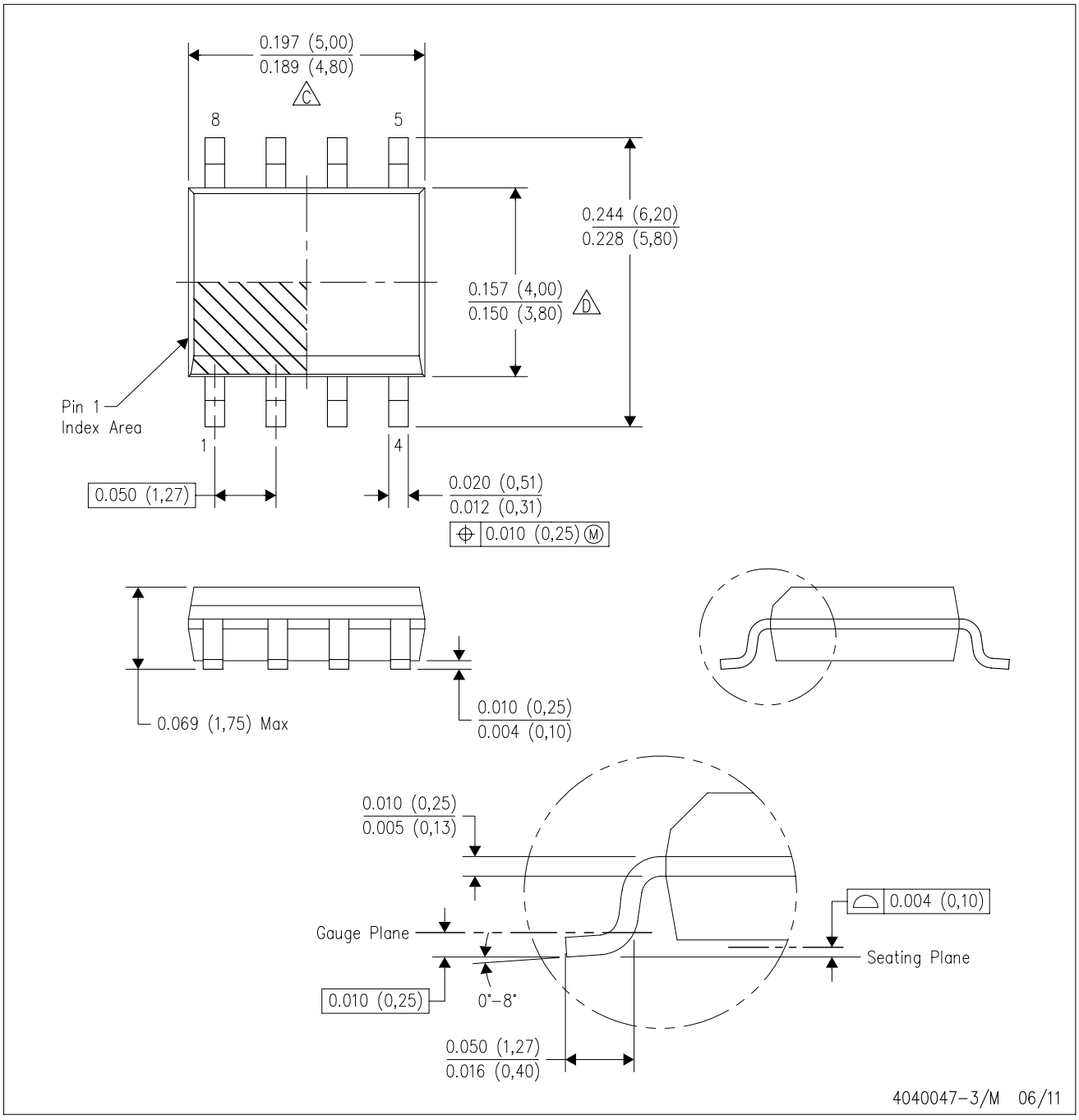
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

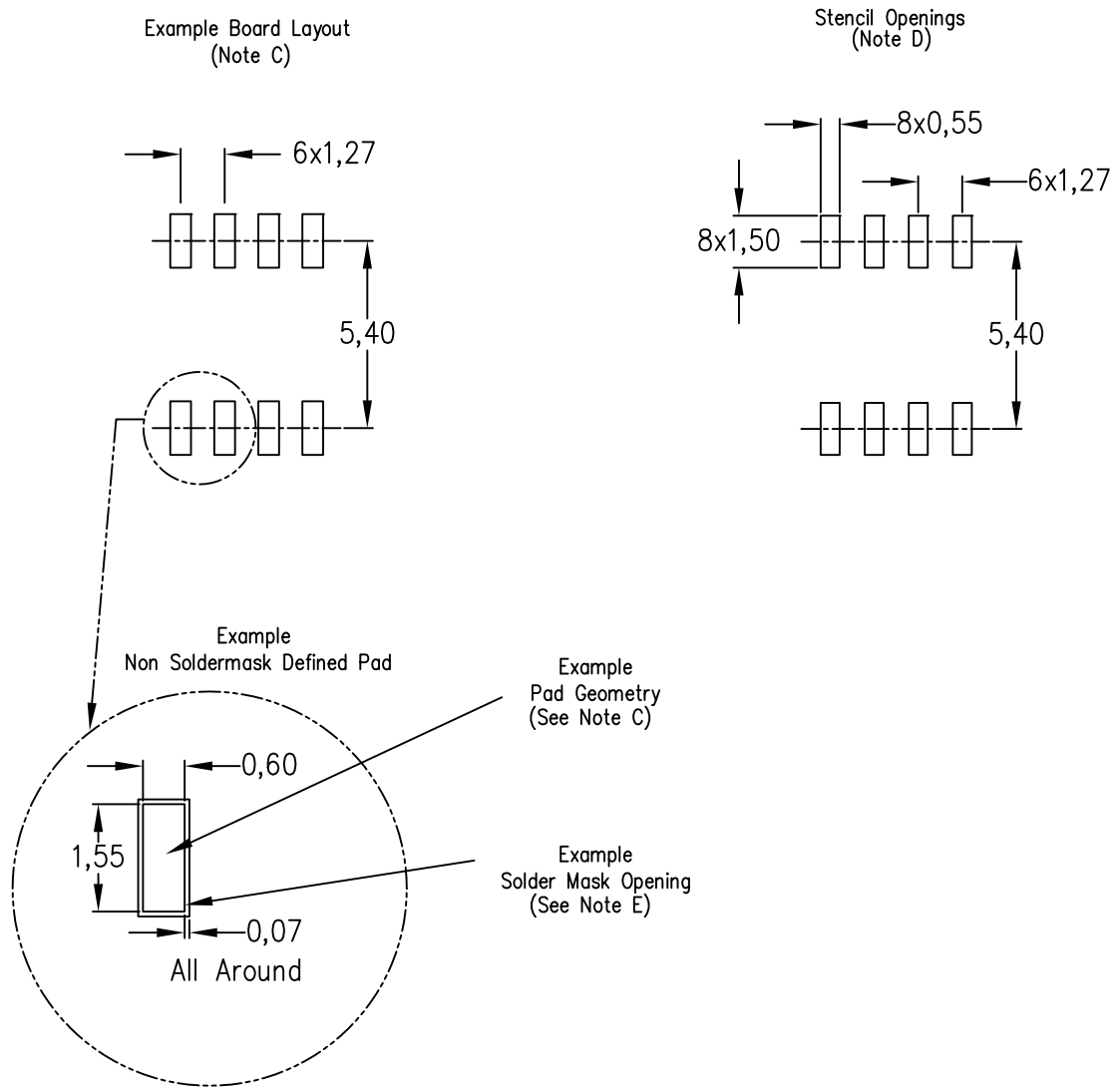
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27322MDREP	SOIC	D	8	2500	367.0	367.0	35.0
UCC27322TDGKREP	VSSOP	DGK	8	2500	367.0	367.0	38.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



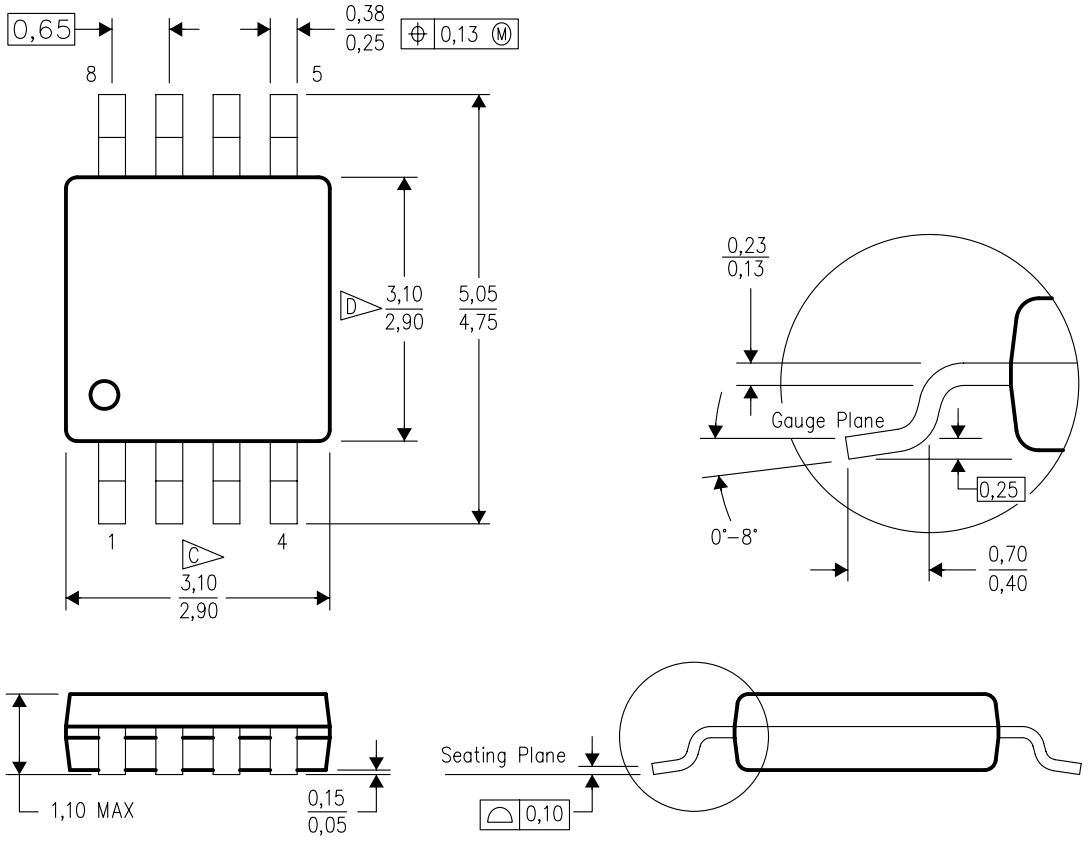
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

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