ULQ200xA-Q1 High-Voltage High-Current Darlington Transistor Arrays

1 Features

- Qualified for Automotive Applications
- ESD Protection Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- 500-mA-Rated Collector Current (Single Output)
- High-Voltage Outputs: 50 V
- Output Clamp Diodes
- Inputs Compatible With Various Types of Logic
- Relay-Driver Applications

2 Applications

- Relay Drivers
- Stepper and DC Brushed Motor Drivers
- Lamp Drivers
- Display Drivers (LED and Gas Discharge)
- Line Drivers
- Logic Buffers

3 Description

The ULQ200xA-Q1 devices are high-voltage high-current Darlington transistor arrays. Each consists of seven npn Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of a single Darlington pair is 500 mA. The Darlington pairs can be paralleled for higher current capability.

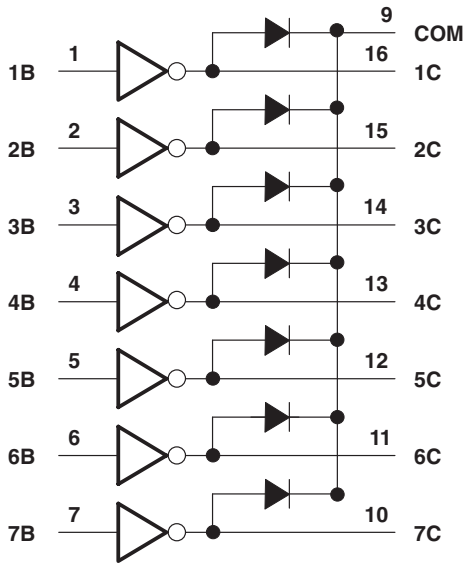
The ULQ2003A-Q1 has a 2.7-kΩ series base resistor for each Darlington pair, for operation directly with TTL or 5-V CMOS devices. The ULQ2004A-Q1 has a 10.5-kΩ series base resistor to allow operation directly from CMOS devices that use supply voltages of 6 V to 15 V. The required input current of the ULQ2004A-Q1 is below that of the ULQ2003A-Q1.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ULQ2003A-Q1	SOIC (16)	9.90 mm x 3.90 mm
	TSSOP (16)	5.00 mm x 4.40 mm
ULQ2004A-Q1	SOIC (16)	9.90 mm x 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Block Diagram



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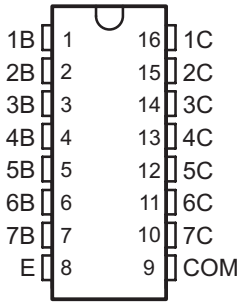
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (April 2010) to Revision E	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Pin Configuration and Functions

D or PW Package
16-Pin SOIC or TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	1B	I	Channel 1 through 7 Darlington base input
2	2B		
3	3B		
4	4B		
5	5B		
6	6B		
7	7B		
8	E	—	Common emitter shared by all channels (typically tied to ground)
9	COM	—	Common cathode node for flyback diodes (required for inductive loads)
10	7C	O	Channel 1 through 7 Darlington collector output
11	6C		
12	5C		
13	4C		
14	3C		
15	2C		
16	1C		

6 Specifications

6.1 Absolute Maximum Ratings

at 25°C free-air temperature (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CE}	Collector-emitter voltage			50	V
	Clamp diode reverse voltage(2)			50	V
V_I	Input voltage(2)			30	V
	Peak collector current	See Figure 16		500	mA
I_{OK}	Output clamp current			500	mA
	Total emitter-terminal current			–2.5	A
P_D	Continuous total power dissipation		See *Dissipation Ratings*		
T_A	Operating free-air temperature	ULQ200xAT	–40	105	°C
		ULQ200xAQ	–40	125	
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CE}	Collector-emitter voltage	0	50	V
T_J	Junction temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		ULQ2003A-Q1, ULQ2004A-Q1	ULQ2003A-Q1	UNIT
		D (SOIC)	PW (TSSOP)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73	108	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics, ULQ2003AT and ULQ2003AQ

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$V_{I(on)}$	On-state input voltage	V_{CE} = 2 V, see Figure 10	I_C = 200 mA				2.7	V
			I_C = 250 mA				2.9	
			I_C = 300 mA				3	
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_I = 250 µA, I_C = 100 mA, see Figure 9		ULQ2003AT		0.9	1.2	V
				ULQ2003AQ		1	1.3	
		I_I = 350 µA, I_C = 200 mA, see Figure 9		ULQ2003AT		1	1.4	
				ULQ2003AQ		1	1.5	
		I_I = 500 µA, I_C = 350 mA, see Figure 9		ULQ2003AT		1.2	1.7	
				ULQ2003AQ		1.2	1.8	
I_{CEX}	Collector cutoff current	V_{CE} = 50 V, I_I = 0, see Figure 3	T_A = 25°C				100	µA
			T_A = 105°C, ULQ2003AT				165	
V_F	Clamp forward voltage	I_F = 350 mA, see Figure 8				1.7	2.2	V
$I_{I(off)}$	Off-state input current	V_{CE} = 50 V, I_C = 500 µA, see Figure 5			30	65		µA
I_I	Input current	V_I = 3.85 V, see Figure 6				0.93	1.35	mA
I_R	Clamp reverse current	V_R = 50 V, T_A = 25°C, see Figure 7					100	µA
C_i	Input capacitance	V_I = 0, f = 1 MHz				15	25	pF

6.6 Electrical Characteristics, ULQ2004AT

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{I(on)}$	On-state input voltage	V_{CE} = 2 V, see Figure 10	I_C = 125 mA			5	V
			I_C = 200 mA			6	
			I_C = 275 mA			7	
			I_C = 350 mA			8	
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_I = 250 µA, I_C = 100 mA, see Figure 9			0.9	1.1	V
		I_I = 350 µA, I_C = 200 mA, see Figure 9			1	1.3	
		I_I = 500 µA, I_C = 350 mA, see Figure 9			1.2	1.6	
I_{CEX}	Collector cutoff current	V_{CE} = 50 V, I_I = 0, See Figure 3	T_A = 25°C			50	µA
			T_A = 105°C				
		V_{CE} = 50 V, see Figure 4	I_I = 0			100	
			V_I = 1 V			500	
V_F	Clamp forward voltage	I_F = 350 mA, see Figure 8			1.7	2.1	V
$I_{I(off)}$	Off-state input current	V_{CE} = 50 V, I_C = 500 µA, see Figure 5		50	65		µA
I_I	Input current	V_I = 5 V, see Figure 6			0.35	0.5	mA
		V_I = 12 V, , see Figure 6			1	1.45	
I_R	Clamp reverse current	V_R = 50 V, see Figure 7	T_A = 25°C			50	µA
			T_A = 105°C			100	
C_i	Input capacitance	V_I = 0, f = 1 MHz			15	25	pF

6.7 Switching Characteristics, ULQ2003A and ULQ2004A

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	See Figure 11		1	10	µs
t_{PHL}	Propagation delay time, high- to low-level output	See Figure 11		1	10	µs
V_{OH}	High-level output voltage after switching	V_S = 50 V, I_O = 300 mA, See Figure 12	V_S – 500			mV

6.8 Dissipation Ratings

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING	T_A = 105°C POWER RATING	T_A = 125°C POWER RATING
D	950 mW	7.6 mW/°C	494 mW	342 mW	190 mW

6.9 Typical Characteristics

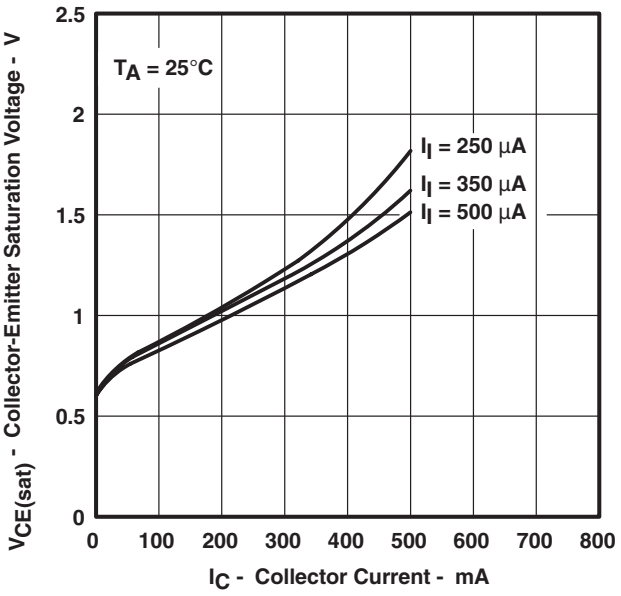


Figure 1. Collector-Emitter Saturation Voltage vs Collector Current (One Darlington)

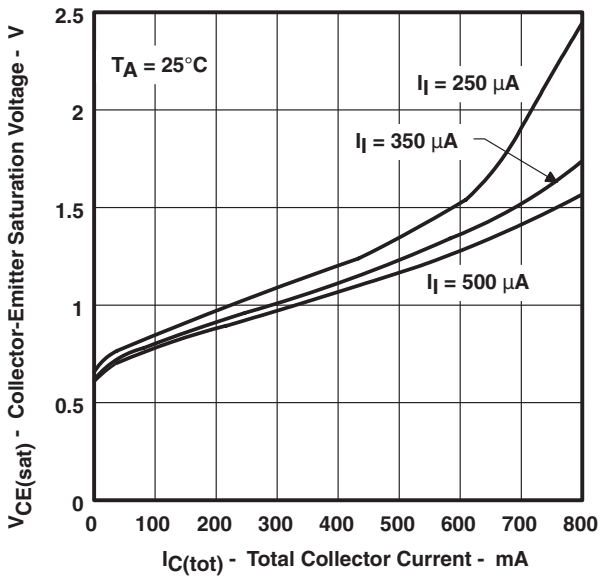


Figure 2. Collector-Emitter Saturation Voltage vs Total Collector Current (Two Darlingtons in Parallel)

7 Parameter Measurement Information

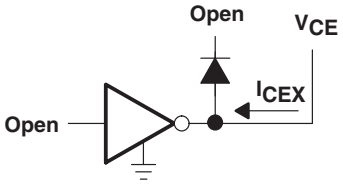


Figure 3. I_{CEX} Test Circuit

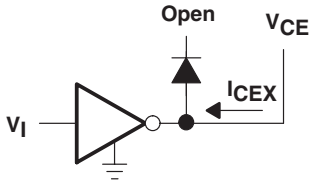


Figure 4. I_{CEX} Test Circuit

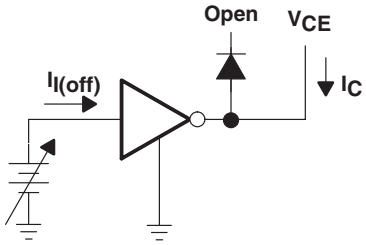
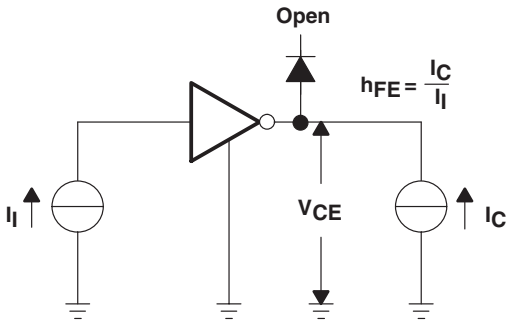


Figure 5. $I_{I(off)}$ Test Circuit



A. I_I is fixed for measuring $V_{CE(sat)}$, variable for measuring h_{FE}.

Figure 9. h_{FE}, $V_{CE(sat)}$ Test Circuit

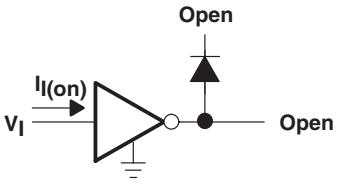


Figure 6. I_I Test Circuit

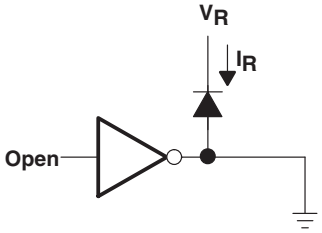


Figure 7. I_R Test Circuit

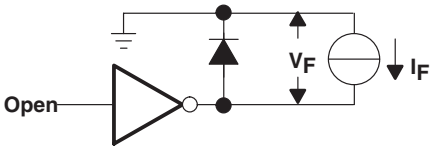


Figure 8. V_F Test Circuit

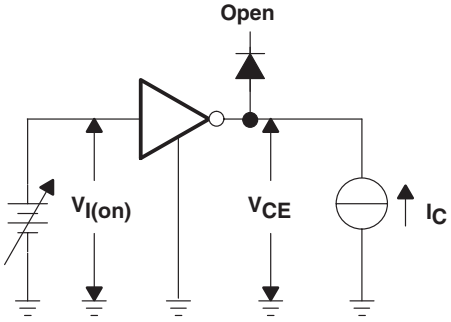


Figure 10. $V_{I(on)}$ Test Circuit

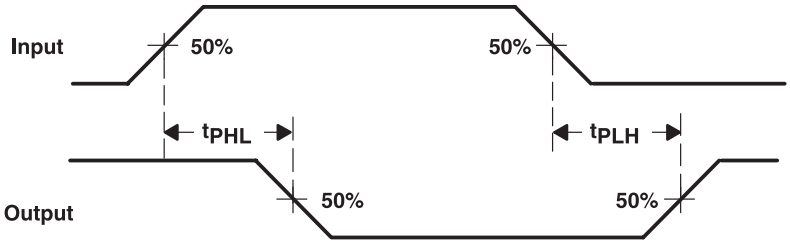
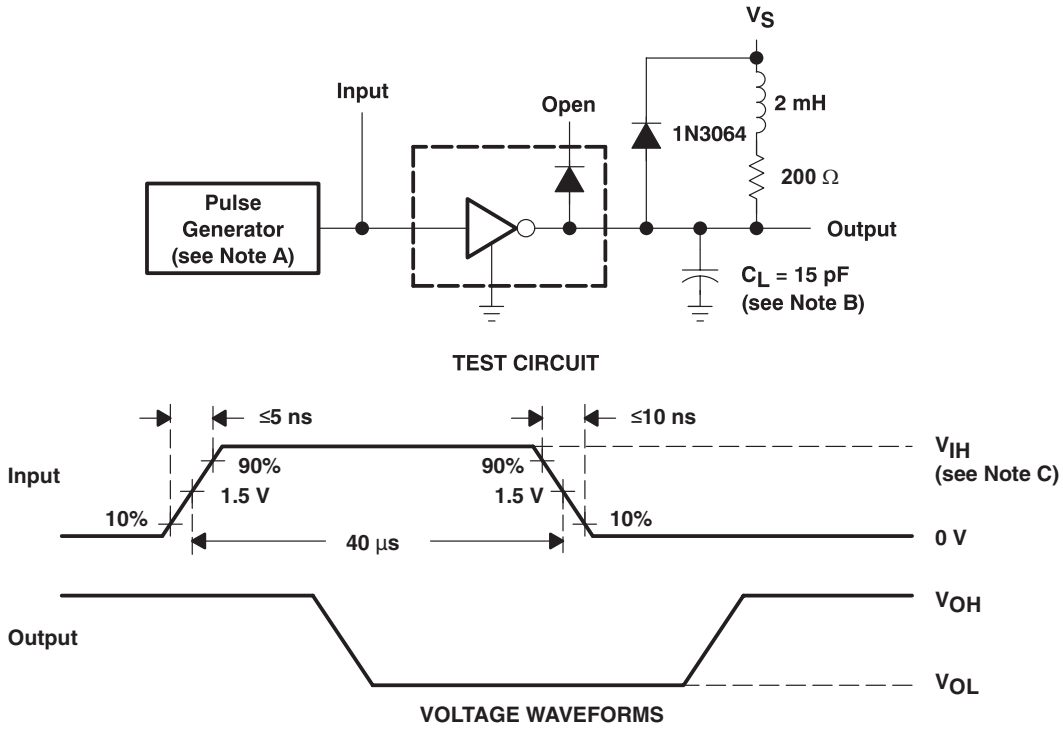


Figure 11. Propagation Delay-Time Waveforms



A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

C. For testing the ULQ2003A, V_{IH} = 3 V; for the ULQ2004A, V_{IH} = 8 V.

Figure 12. Latch-Up Test Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

This standard device has proven ubiquity and versatility across a wide range of applications. This is due to integration of 7 Darlington transistors of the device that are capable of sinking up to 500 mA and wide GPIO range capability.

The ULQ200xA-Q1 devices comprise seven high-voltage, high-current NPN Darlington transistor pairs. All units feature a common emitter and open collector outputs. To maximize their effectiveness, these units contain suppression diodes for inductive loads. The ULNQ200xA-Q1 devices have a series base resistor to each Darlington pair, thus allowing operation directly with TTL or CMOS operating at supply voltages of 5 V or 3.3 V. The ULQ2003xA-Q1 device offers solutions to a great many interface needs, including solenoids, relays, lamps, small motors, and LEDs. Applications requiring sink currents beyond the capability of a single output may be accommodated by paralleling the outputs.

This device can operate over a wide temperature range (–40°C to 105°C for ULQ200xAT or –40°C to 125°C for ULQ2003AQ).

8.2 Functional Block Diagram

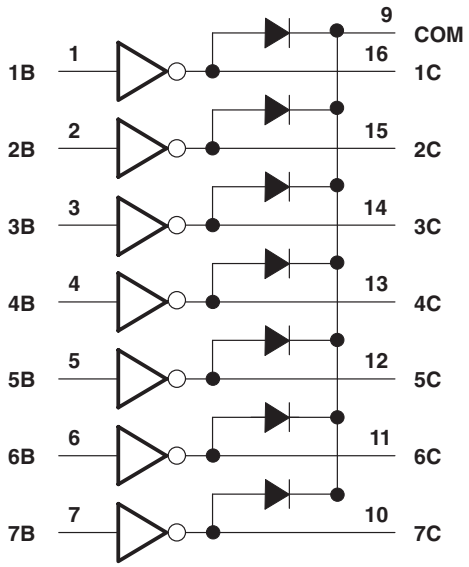
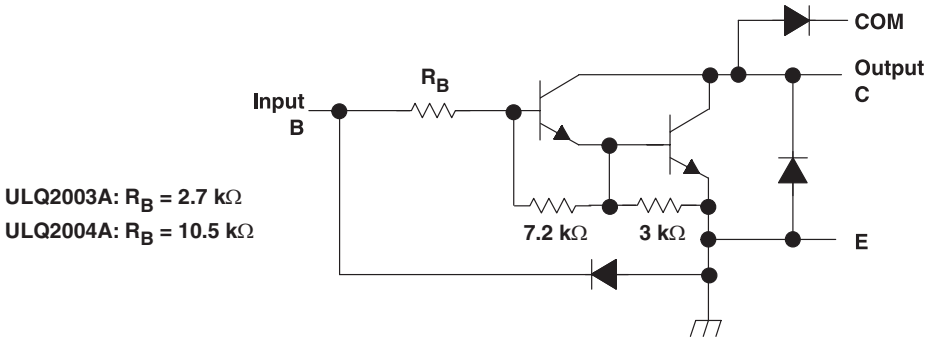


Figure 13. Logic Diagram

Functional Block Diagram (continued)



A. All resistor values shown are nominal.

B. The collector-emitter diode is a parasitic structure and should not be used to conduct current. If the collector(s) go below ground an external Schottky diode should be added to clamp negative undershoots.

Figure 14. Schematics (Each Darlington Pair)

8.3 Feature Description

Each channel of the ULQ200xA-Q1 devices consist of Darlington connected NPN transistors. This connection creates the effect of a single transistor with a very high-current gain (β2). This can be as high as 10,000 A/A at certain currents. The very high β allows for high-output current drive with a very low input current, essentially equating to operation with low GPIO voltages.

The GPIO voltage is converted to base current through the 2.7-kΩ or 10.5-kΩ resistor connected between the input and base of the predriver Darlington NPN. The 7.2-kΩ and 3-kΩ resistors connected between the base and emitter of each respective NPN act as pulldowns and suppress the amount of leakage that may occur from the input.

The diodes connected between the output and COM pin is used to suppress the kick-back voltage from an inductive load that is excited when the NPN drivers are turned off (stop sinking) and the stored energy in the coils causes a reverse current to flow into the coil supply through the kick-back diode.

In normal operation the diodes on base and collector pins to emitter will be reversed biased. If these diodes are forward biased, internal parasitic NPN transistors will draw (a nearly equal) current from other (nearby) device pins.

8.4 Device Functional Modes

8.4.1 Inductive Load Drive

When the COM pin is tied to the coil supply voltage, ULQ200xA-Q1 devices are able to drive inductive loads and suppress the kick-back voltage through the internal free-wheeling diodes.

8.4.2 Resistive Load Drive

When driving a resistive load, a pullup resistor is needed in order for the ULQ200xA-Q1 devices to sink current and for there to be a logic high level. The COM pin can be left floating for these applications.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Typically, the ULQ200xA-Q1 device drives a high-voltage or high-current (or both) peripheral from an MCU or logic device that cannot tolerate these conditions. This design is a common application of ULQ200xA-Q1 device, driving inductive loads. This includes motors, solenoids and relays. Figure 15 shows an example of driving multiple inductive loads.

9.2 Typical Application

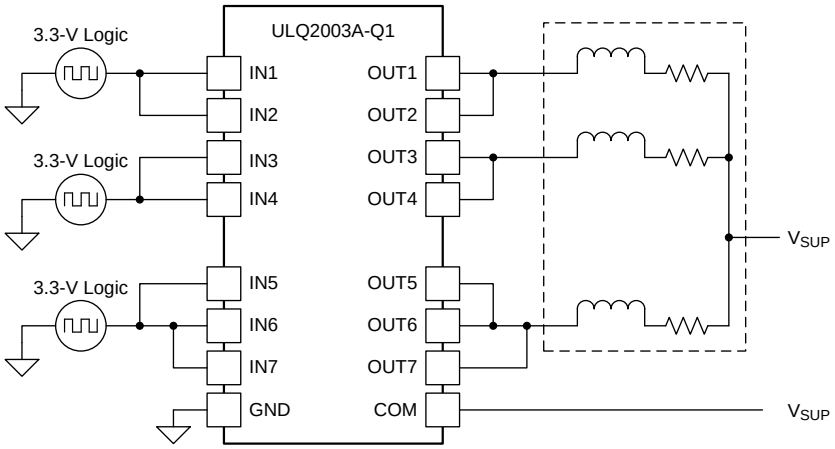


Figure 15. ULQ2003A-Q1 Device as Inductive Load Driver

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
GPIO voltage	3.3 V or 5 V
Coil supply voltage	12 V to 48 V
Number of channels	7
Output current (R_{COIL})	20 mA to 300 mA per channel
Duty cycle	100%

9.2.2 Detailed Design Procedure

When using ULQ2003A-Q1 device in a coil driving application, determine the following:

- Input voltage range
- Temperature range
- Output and drive current
- Power dissipation

9.2.2.1 Drive Current

The coil voltage (V_{SUP}), coil resistance (R_{COIL}), and low-level output voltage ($V_{CE(SAT)}$ or V_{OL}) determine the coil current.

$$I_{COIL} = (V_{SUP} – V_{CE(SAT)}) / R_{COIL} \quad (1)$$

9.2.2.2 Low-Level Output Voltage

The low-level output voltage (V_{OL}) is the same as $V_{CE(SAT)}$ and can be determined by, Figure 1 or Figure 2.

9.2.2.3 Power Dissipation and Temperature

The number of coils driven is dependent on the coil current and on-chip power dissipation. The number of coils driven can be determined by Figure 16.

For a more accurate determination of number of coils possible, use Equation 2 to calculate ULQ200xA-Q1 device on-chip power dissipation P_D:

$$P_D = \sum_{i=1}^{N} V_{OLi} \times I_{Li}$$

where

- N is the number of channels active together
- V_{OLi} is the OUT_i pin voltage for the load current I_{Li}. This is the same as $V_{CE(SAT)}$

(2)

To ensure reliability of ULQ200xA-Q1 device and the system, the on-chip power dissipation must be lower that or equal to the maximum allowable power dissipation ($PD_{(MAX)}$) dictated by Equation 3.

$$PD_{(MAX)} = \left(T_{J(MAX)} – T_A\right) \Big/ \theta_{JA}$$

where

- $T_{J(max)}$ is the target maximum junction temperature
- T_A is the operating ambient temperature
- $R_{\theta JA}$ is the package junction to ambient thermal resistance

(3)

Limit the die junction temperature of the ULQ200xA-Q1 device to less than 125°C. The IC junction temperature is directly proportional to the on-chip power dissipation.

9.2.3 Application Curve

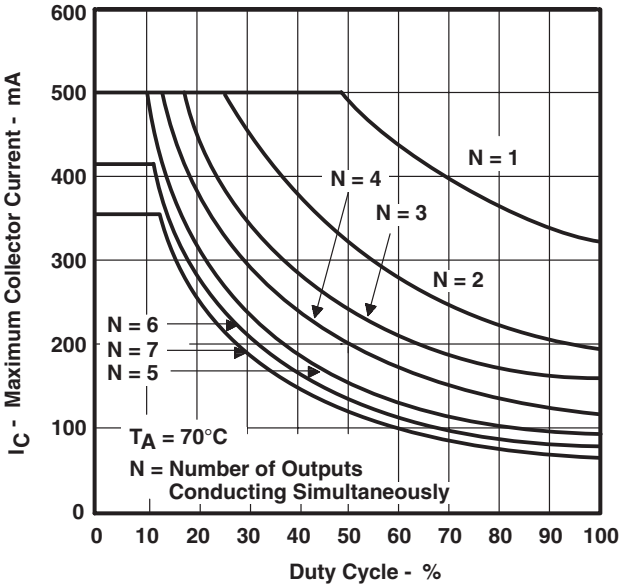


Figure 16. D Package Maximum Collector Current vs Duty Cycle

9.3 System Examples

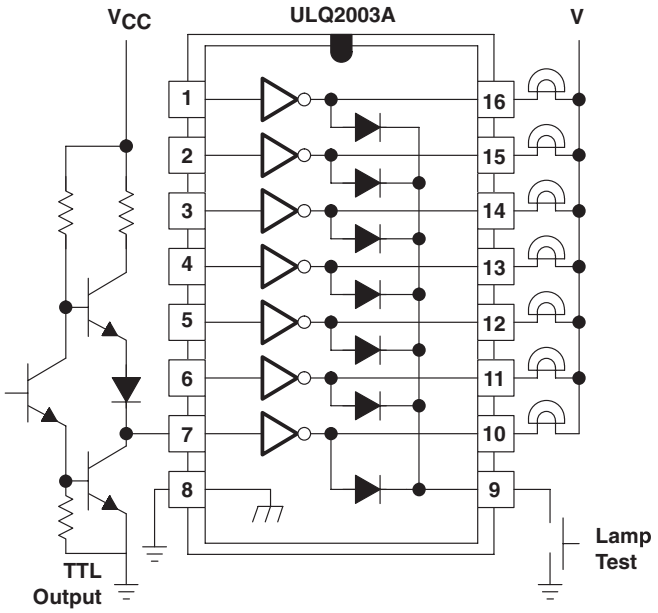


Figure 17. TTL to Load

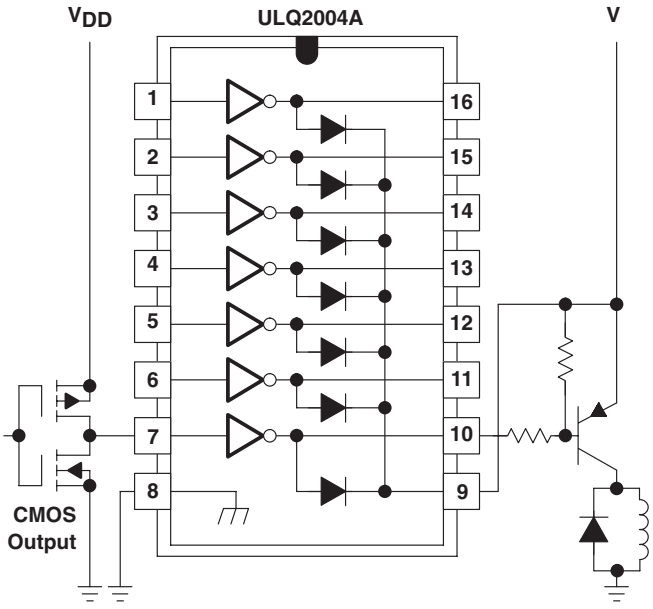


Figure 18. Buffer for Higher Current Loads

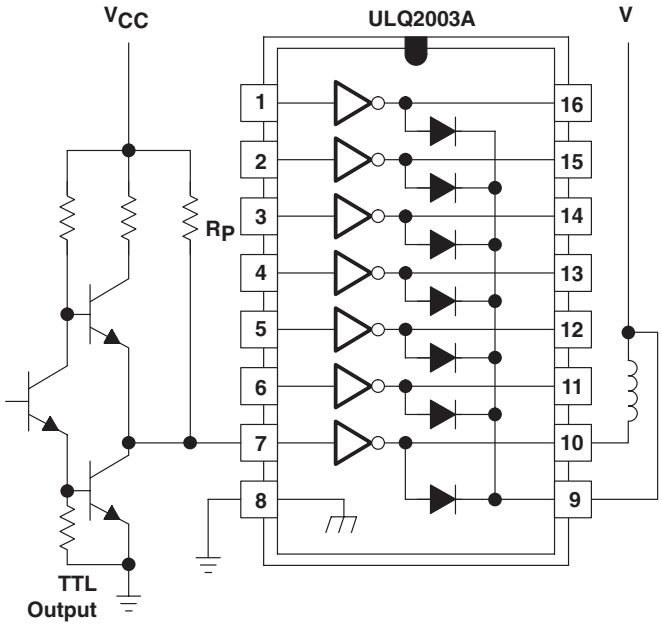


Figure 19. Use of Pullup Resistors to Increase Drive Current

10 Power Supply Recommendations

This device does not need a power supply. However, the COM pin is typically tied to the system power supply. When this is the case, it is very important to ensure that the output voltage does not heavily exceed the COM pin voltage. This discrepancy heavily forward biases the fly-back diodes and causes a large current to flow into COM, potentially damaging the on-chip metal or over-heating the device.

11 Layout

11.1 Layout Guidelines

Thin traces can be used on the input due to the low-current logic that is typically used to drive the ULQ200xA-Q1 devices. Take care to separate the input channels as much as possible, as to eliminate crosstalk. TI recommends thick traces for the output to drive whatever high currents that may be needed. Wire thickness can be determined by the current density of the trace material and desired drive current.

Because all of the channels currents return to a common emitter, it is best to size that trace width to be very wide. Some applications require up to 2.5 A.

11.2 Layout Example

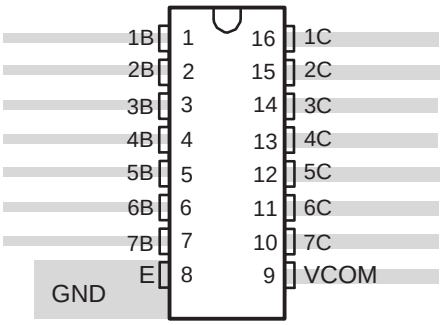


Figure 20. Package Layout

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ULQ2003A-Q1	Click here	Click here	Click here	Click here	Click here
ULQ2004A-Q1	Click here	Click here	Click here	Click here	Click here

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ULQ2003AQDRQ1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ULQ2003AQ	Samples
ULQ2003ATDG4Q1	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	ULQ2003AT	Samples
ULQ2003ATDQ1	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	ULQ2003AT	Samples
ULQ2003ATDRG4Q1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	ULQ2003AT	Samples
ULQ2003ATDRQ1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	ULQ2003AT	Samples
ULQ2003ATPWRQ1	ACTIVE	TSSOP	PW	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	U2003AT	Samples
ULQ2004ATDRG4Q1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	ULQ2004AT	Samples
ULQ2004ATDRQ1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	ULQ2004AT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF ULQ2003A-Q1, ULQ2004A-Q1 :

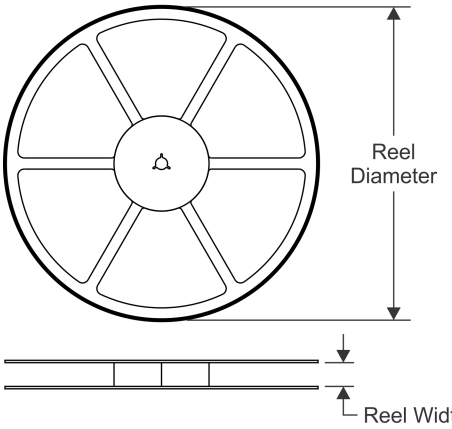
- Catalog: ULQ2003A, ULQ2004A

NOTE: Qualified Version Definitions:

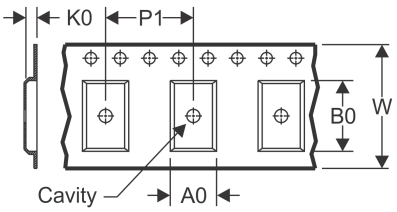
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

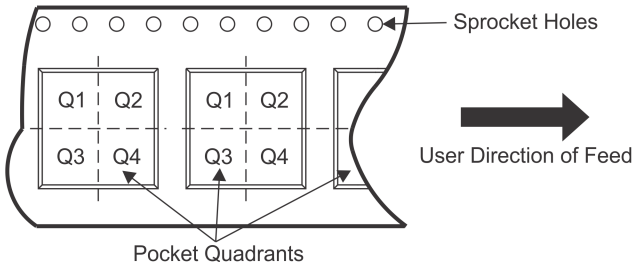


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

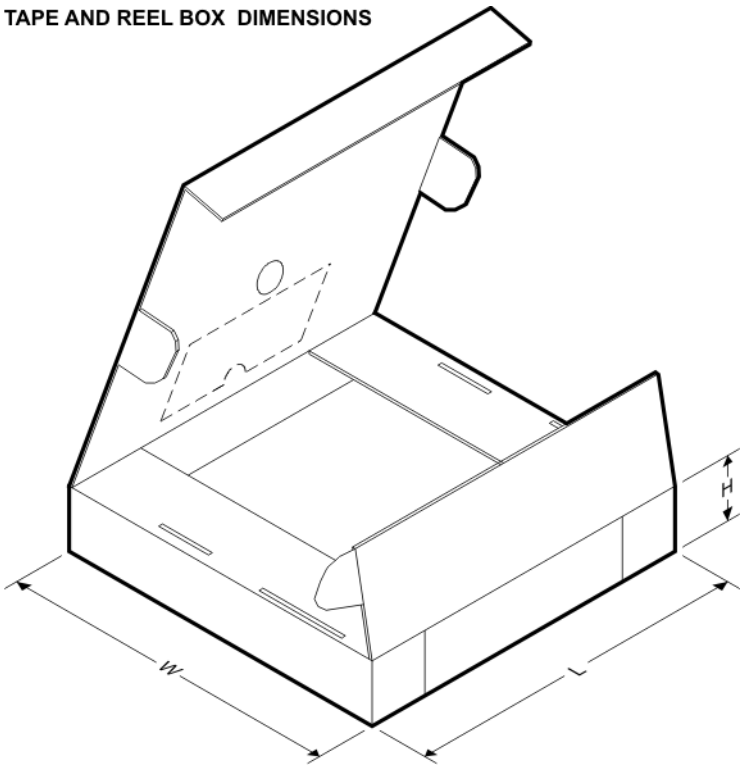
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ULQ2003ATPWRQ1	TSSOP	PW	16	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

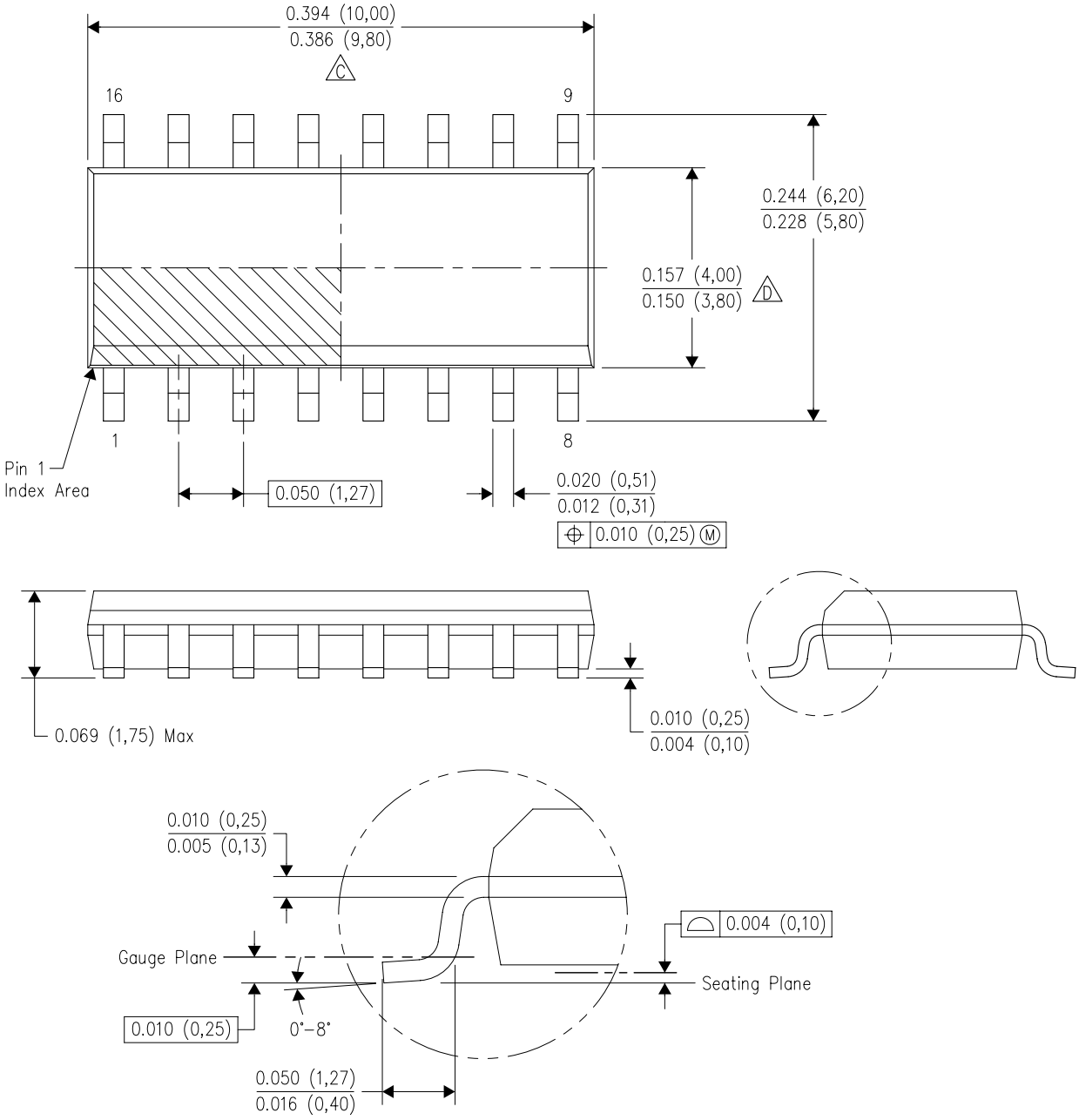
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

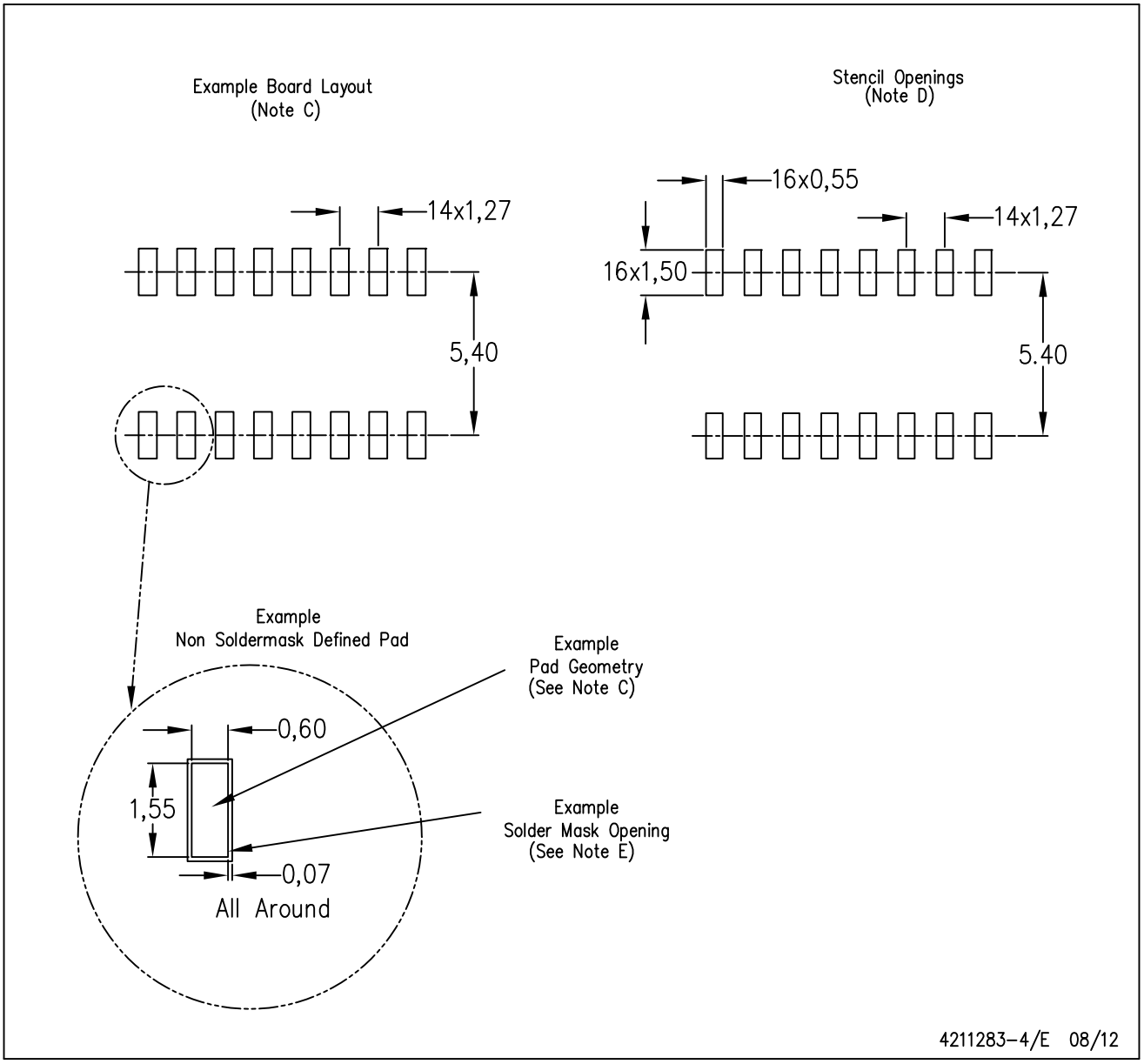
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ULQ2003ATPWRQ1	TSSOP	PW	16	2500	367.0	367.0	35.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



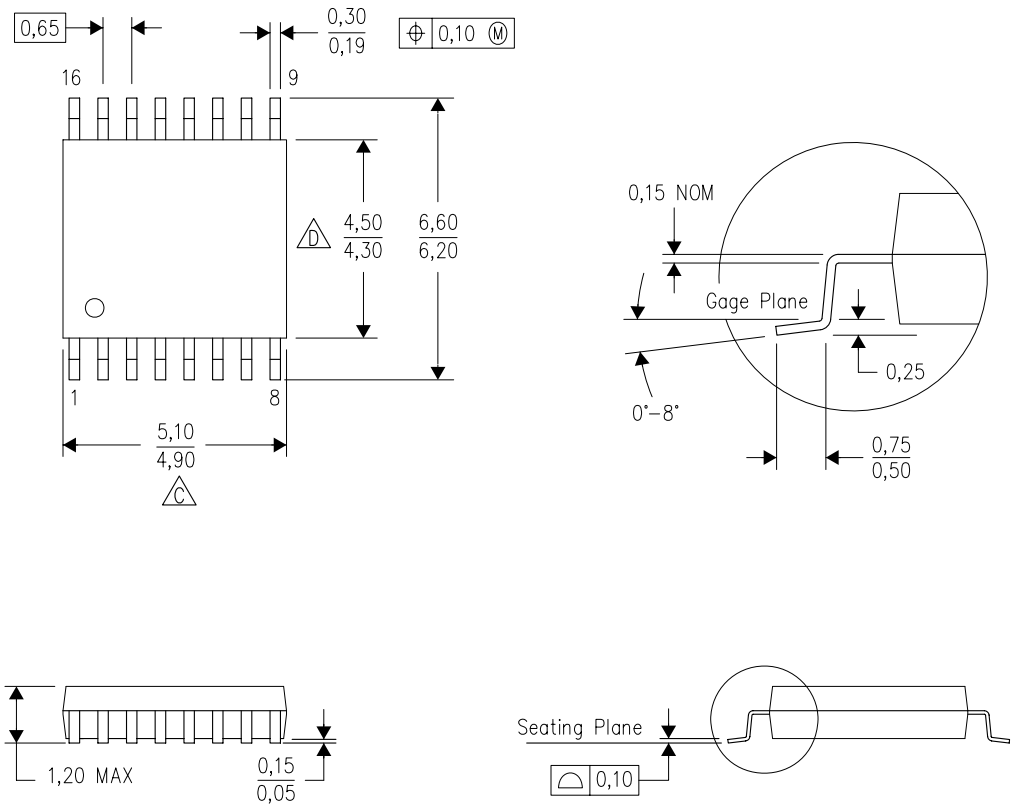
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

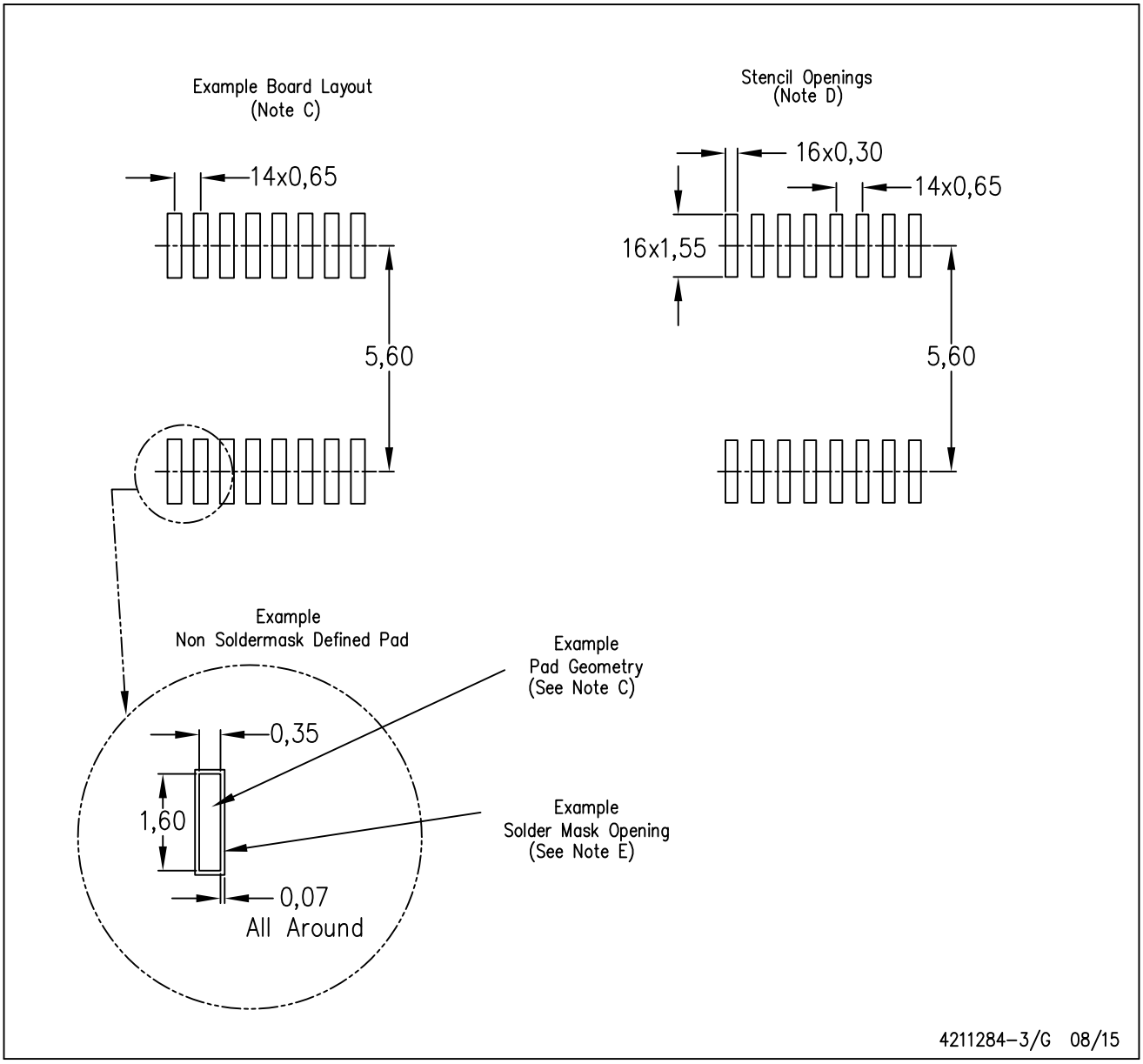
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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