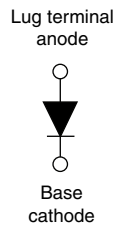


## High Performance Schottky Rectifier, 180 A


**HALF-PAK (D-67)**


### FEATURES

- 175 °C  $T_J$  operation
- Low forward voltage drop
- High frequency operation
- Guard ring for enhanced ruggedness and long term reliability
- Designed and qualified for industrial level
- UL approved file E222165
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS**  
COMPLIANT

PRIMARY CHARACTERISTICS	
$I_{F(AV)}$	180 A
$V_R$	100 V
Package	HALF-PAK (D-67)
Circuit configuration	Single

### DESCRIPTION

The VS-183NQ.. high current Schottky rectifier module series has been optimized for low reverse leakage at high temperature. The proprietary barrier technology allows for reliable operation up to 175 °C junction temperature. Typical applications are in high current switching power supplies, plating power supplies, UPS systems, converters, freewheeling diodes, welding, and reverse battery protection.

MAJOR RATINGS AND CHARACTERISTICS			
SYMBOL	CHARACTERISTICS	VALUES	UNITS
$I_{F(AV)}$	Rectangular waveform	180	A
$V_{RRM}$		100	V
$I_{FSM}$	$t_p = 5 \mu s$ sine	22 000	A
$V_F$	180 A <sub>pk</sub> , $T_J = 125 \text{ }^\circ\text{C}$	0.73	V
$T_J$	Range	-55 to +175	°C

VOLTAGE RATINGS			
PARAMETER	SYMBOL	VS-183NQ100PbF	UNITS
Maximum DC reverse voltage	$V_R$	100	V
Maximum working peak reverse voltage	$V_{RWM}$		

ABSOLUTE MAXIMUM RATINGS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum average forward current See fig. 5	$I_{F(AV)}$	50 % duty cycle at $T_C = 128 \text{ }^\circ\text{C}$ , rectangular waveform		240	A
Maximum peak one cycle non-repetitive surge current See fig. 7	$I_{FSM}$	5 $\mu s$ sine or 3 $\mu s$ rect. pulse	Following any rated load condition and with rated $V_{RRM}$ applied	22 000	
		10 ms sine or 6 ms rect. pulse		2500	
Non-repetitive avalanche energy	$E_{AS}$	$T_J = 25 \text{ }^\circ\text{C}$ , $I_{AS} = 5.5 \text{ A}$ , $L = 1 \text{ mH}$		15	mJ
Repetitive avalanche current	$I_{AR}$	Current decaying linearly to zero in 1 $\mu s$ Frequency limited by $T_J$ maximum $V_A = 1.5 \times V_R$ typical		1	A



ELECTRICAL SPECIFICATIONS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum forward voltage drop See fig. 1	$V_{FM}^{(1)}$	180 A	$T_J = 25\text{ }^\circ\text{C}$	0.91	V
		360 A		1.23	
		180 A	$T_J = 125\text{ }^\circ\text{C}$	0.73	
		360 A		0.9	
Maximum reverse leakage current See fig. 2	$I_{RM}^{(1)}$	$T_J = 25\text{ }^\circ\text{C}$	$V_R = \text{Rated } V_R$	4.5	mA
		$T_J = 125\text{ }^\circ\text{C}$		60	
Maximum junction capacitance	$C_T$	$V_R = 5 V_{DC}$ (test signal range 100 kHz to 1 MHz) $25\text{ }^\circ\text{C}$		4150	pF
Typical series inductance	$L_S$	From top of terminal hole to mounting plane		6.0	nH
Maximum voltage rate of change	dV/dt	Rated $V_R$		10 000	V/ $\mu\text{s}$

**Note**

(1) Pulse width = 500  $\mu\text{s}$

THERMAL - MECHANICAL SPECIFICATIONS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum junction and storage temperature range	$T_J, T_{Stg}$			-55 to 175	$^\circ\text{C}$
Maximum thermal resistance, junction to case	$R_{thJC}$	DC operation See fig. 4		0.28	$^\circ\text{C/W}$
Typical thermal resistance, case to heatsink	$R_{thCS}$	Mounting surface, smooth and greased		0.05	
Approximate weight				30	g
				1.06	oz.
Mounting torque	minimum	Non-lubricated threads		3 (26.5)	N · m (lbf · in)
	maximum			4 (35.4)	
Terminal torque	minimum			3.4 (30)	
	maximum			5 (44.2)	
Case style				HALF-PAK module	

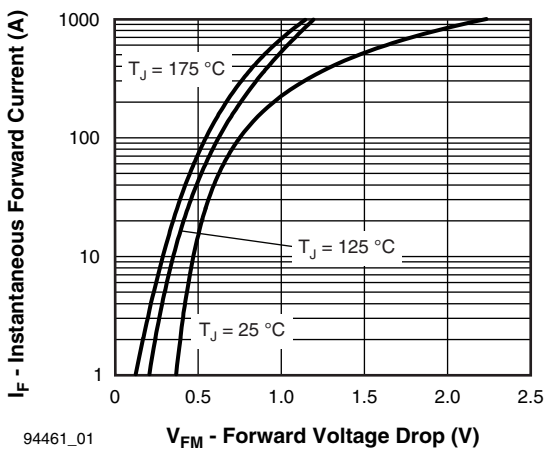


Fig. 1 - Maximum Forward Voltage Drop Characteristics

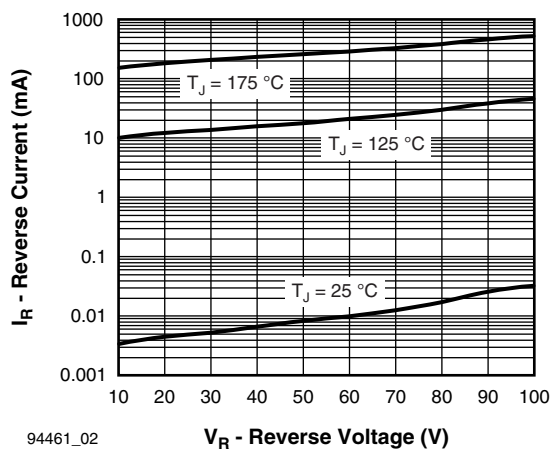
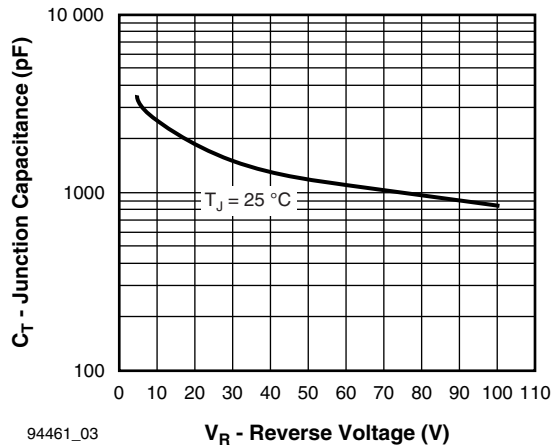
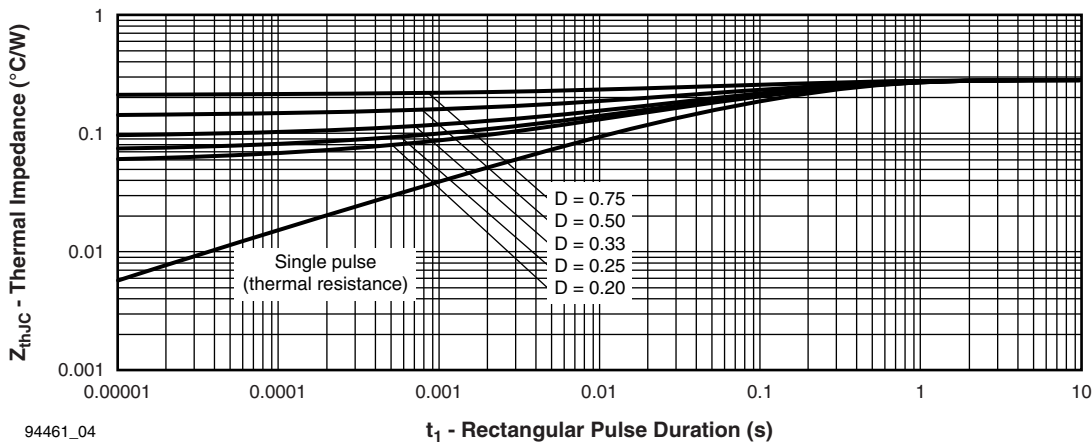


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage



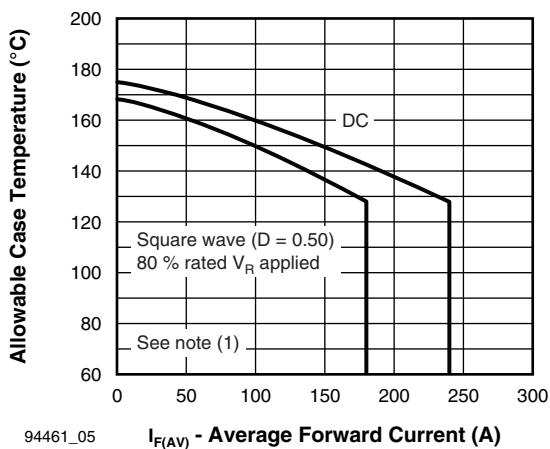
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Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage



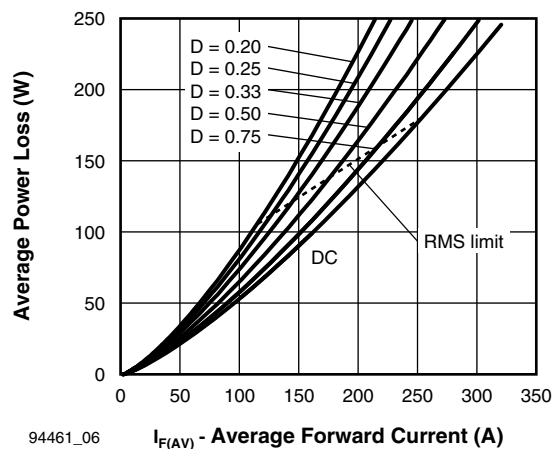
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Fig. 4 - Maximum Thermal Impedance  $Z_{thJC}$  Characteristics



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Fig. 5 - Maximum Allowable Case Temperature vs. Average Forward Current



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Fig. 6 - Forward Power Loss Characteristics

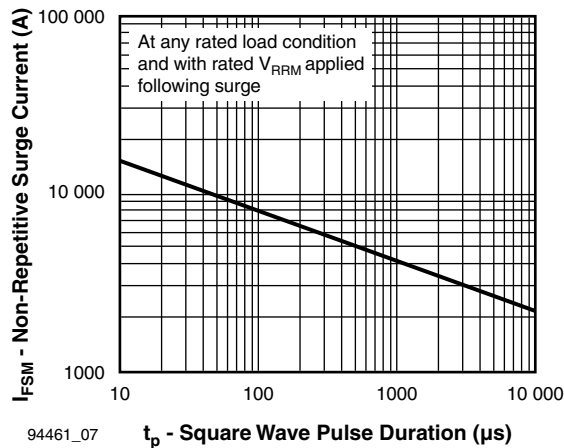


Fig. 7 - Maximum Non-Repetitive Surge Current

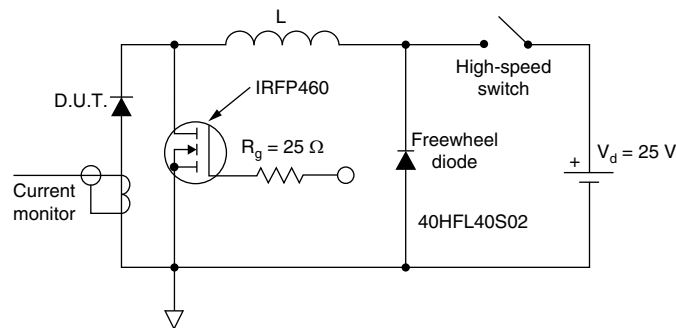


Fig. 8 - Unclamped Inductive Test Circuit

**Note**

- (1) Formula used:  $T_C = T_J - (P_d + P_{d_{REV}}) \times R_{thJC}$ ;
- $P_d$  = forward power loss =  $I_{F(AV)} \times V_{FM}$  at  $(I_{F(AV)}/D)$  (see fig. 6);
- $P_{d_{REV}}$  = inverse power loss =  $V_{R1} \times I_R (1 - D)$ ;  $I_R$  at  $V_{R1}$  = rated  $V_R$

**ORDERING INFORMATION TABLE**

Device code	<b>VS-</b>	<b>18</b>	<b>3</b>	<b>N</b>	<b>Q</b>	<b>100</b>	<b>PbF</b>
	①	②	③	④	⑤	⑥	⑦

- 1** - Vishay Semiconductors product
- 2** - Average current rating (x 10)
- 3** - Product silicon identification
- 4** - N = not isolated
- 5** - Q = Schottky rectifier diode
- 6** - Voltage rating (100 = 100 V)
- 7** - Lead (Pb)-free

LINKS TO RELATED DOCUMENTS	
Dimensions	<a href="http://www.vishay.com/doc?95020">www.vishay.com/doc?95020</a>

## D-67 HALF-PAK

**DIMENSIONS** in millimeters (inches)





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